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UNISYS

BT 3200 Series 324X/326X/328X Magnetic Tape Subsystem

Maintenance Manual

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Model Number Cross Reference Table

UNISYS Model No.	Description Model No.
3241	F617A1
3242	F617A2
3244	F617B
3243	F617E
3261	F618A1
3262	F618A2
3266	F618B
3265	F618E
3281	M2436-1
3282	M2436-2
3288	M2436-8

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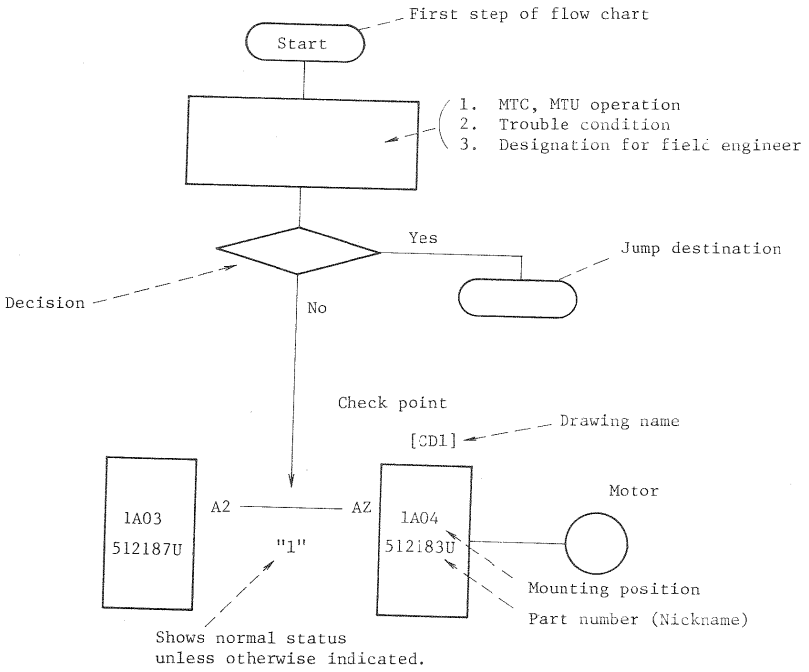
PLAN 1	Introduction, How to Use the MAP

Introduction

This Maintenance Manual describes tracing of visible trouble and tracing of trouble from sense data. It also includes checking and adjustment in OFFLINE mode and part replacement.

How to use the MAP

The symbols used in this manual are described below:



PLAN 2	How to Use the OLTE

I. The Online Test Program (OLTE) is used for the following purposes.

Trace of trouble
Checking after trouble correction
Preventive maintenance

The general flow charts of maintenance procedure, including OLTE running for these purposes, are shown in MAP50 and MAP90.
OLTE is composed of several sections and can be grouped in following four parts.
Each section in these groups may be choosed by means of maintenance purpose.
The contents and purposes of each section are detailed in the OLTE GUIDE.

A. Magnetic tape subsystem function test (JYOMT6A-G)

This group tests basic operation of the magnetic tape subsystem.
When an error is detected in these sections, trace of trouble is performed by MAP D0001 ∿ according to the sense data and the error messages.

B. Magnetic tape subsystem running test (JYOMT6H-I)

The read/write operation and data transfer functions are tested.
This group is used in the case of read/write trouble and preventive maintenance.
When an error is detected in these sections, trace of trouble is performed by MAP D0001 ∿ according to the sense data and the error messages.

C. MTC diagnosis (JYOMT6DA-DK)

Error detection and correction functions in the MTC are checked by diagnostic read/write operation.
When an error is detected in these sections, trace of trouble is performed by MAP D0001 ∿ according to the sense data and the error messages.

D. MTU prognosis

The MTU basic operation is tested by XFR mode of the set diagnose command.
At the preventive maintenance, the machine is checked by MAP TST6220 ∿ according to MTU prognose data.

E. MTC function test (JYOMT6K-M, FA-FZ, SB-SL)

This is the function tests for the MTC which aim primarily at testing the control function of the MTC on the reserve/release operation of the MTU, the functions accompanied by the cross-call constitution, and high speed functions.

II. Starting of OLTE

When the on-line test program (OLTE) has responded to the output message from the control program (OLTEC), it is loaded by control program and the execute phase is transferred.
Response format is shown below.

DEVICE/TEST/OPTION

DEVICE: Device address

This address is pre-determined at the time of system generation.

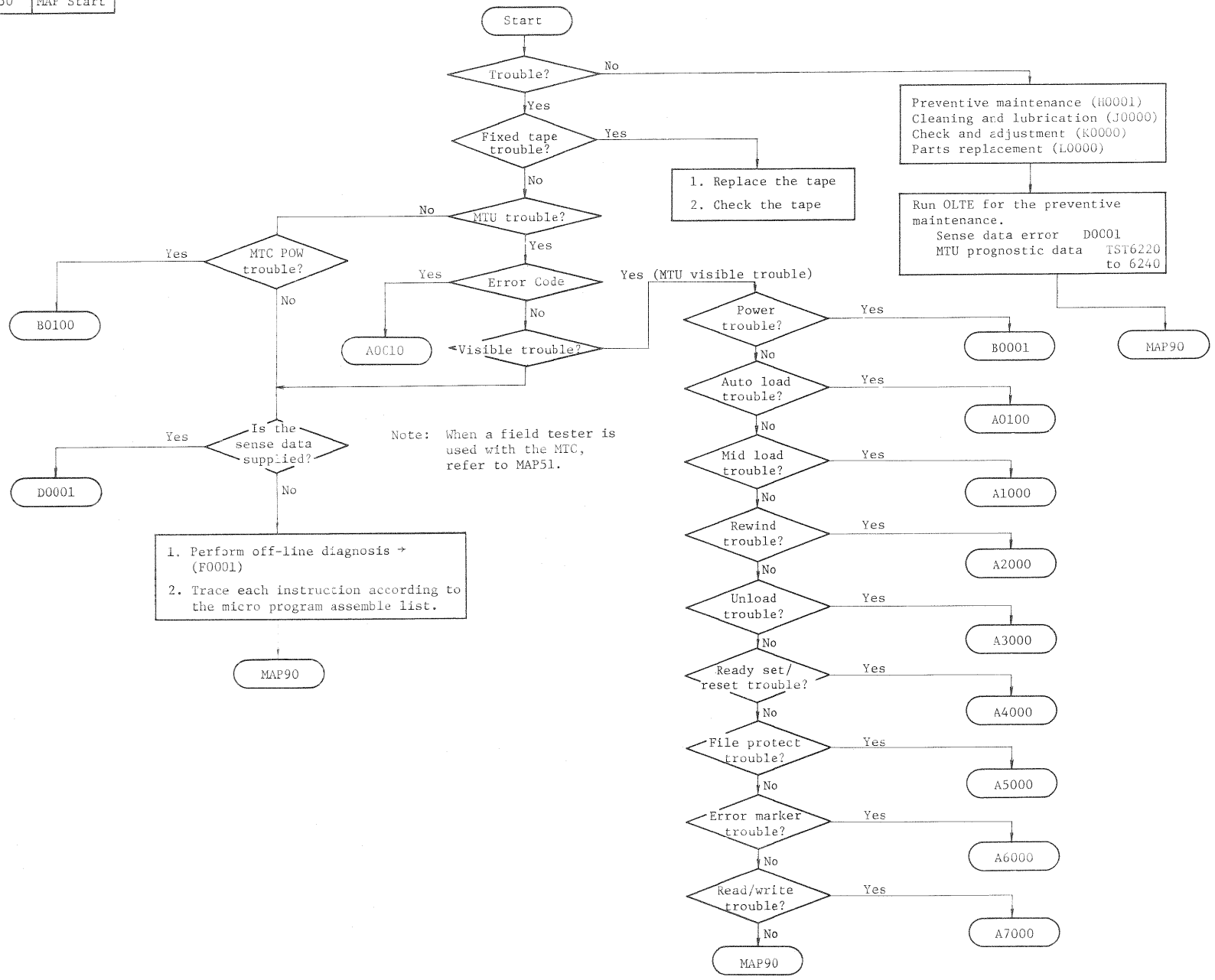
TEST: Section name

Specify the section name of the test module.

OPTION: Option and reference value

This can assign CP, FE, LP, TL, MI, EX, etc.
(Refer to the OLTE Guide in detail.)

MAP50	MAP Start



MAP51	Connection of a Field Tester to MTC

A field tester may be connected to the MTC for the maintenance purpose. When a field tester is connected to the MTC, the state of the ONL/OFL switch of the field tester connected to the MTC exerts influence on the MTC (when the MTC changes the operating mode from ONLINE to OFFLINE or vice versa, a system reset signal is issued). Accordingly, attention must be paid for the environment of the MTC to which a field tester is connected such as one that there is no job using this MT subsystem.

Either one of the following ways is desirable for the connection of a field tester and the MTC.

(1) A field tester is connected to the MTC when the power supply to the MTC is off.

(2) To connect a field tester to the MTC while the power supply to the MTC is kept on, the connection may be done with the power supply being kept on if the MTC may be put to the offline status.

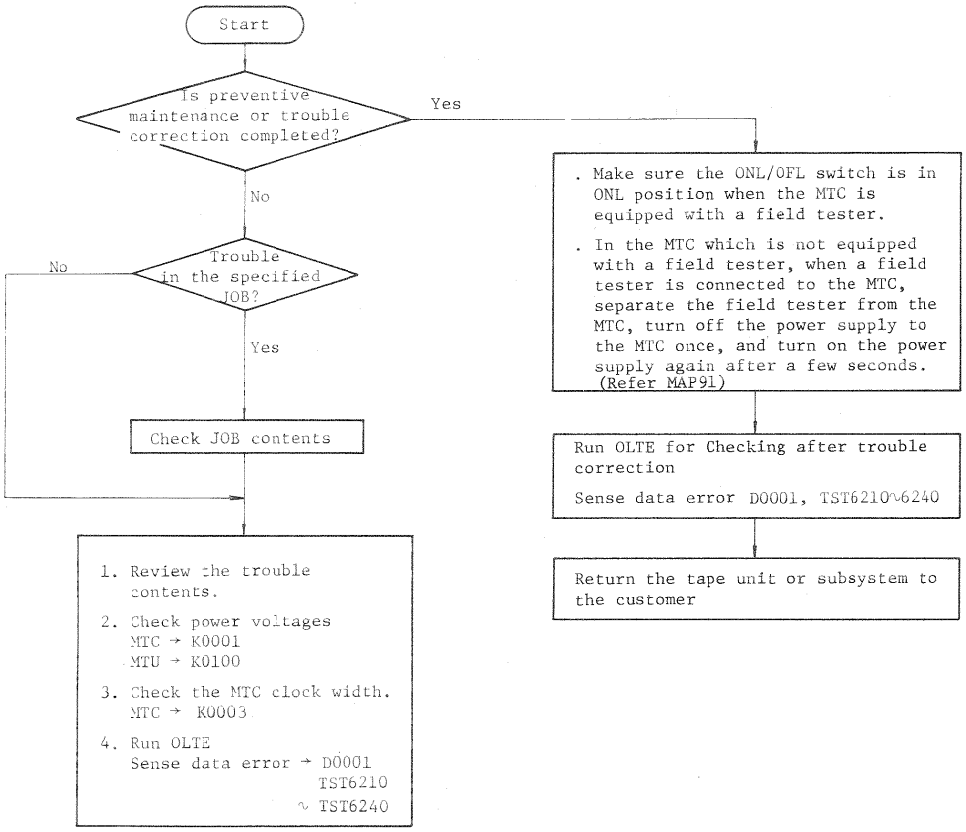
(3) To connect a field tester to the MTC while the power supply to the MTC is kept on, the following procedure is used if the MTC needs to be kept in the online status.

1) Clip BA8 card pin on 1A07 column at 0 V.

2) Connect a field tester to the MTC, in the location 1A07 Port A with the ONL/OFL switch on field tester remaining the ONL position.

3) In the case where only the display function of field tester is used, BA8 card pin on 1A07 column may be left clipped. In the case where the control function of field tester is used (CNT or SSS switch is operated), release the BA8 card pin on 1A07 column clipped at 0 V. (Refer to MAP91)

MAP90	MAP End



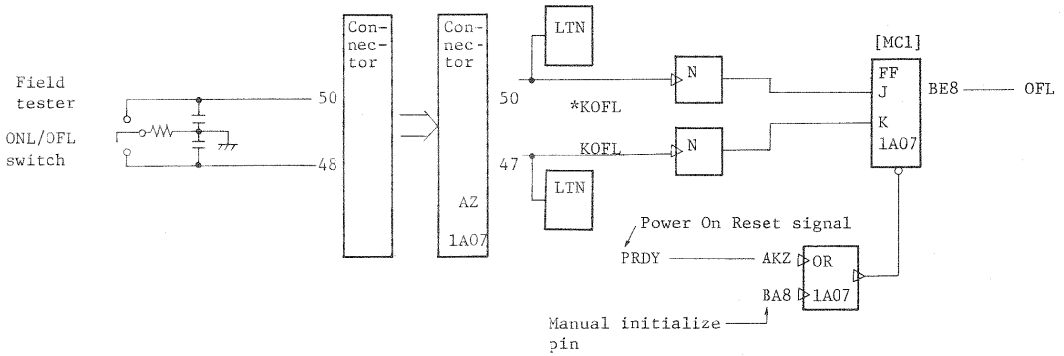
MAP91	Separation of a Field Tester from the MTC

When a field tester connected to the MTC is separated, the status of the MTC might become indefinite either ONLINE status or OFFLINE status due to the state or chattering of the ONL/OFL switch of the field tester which may occur. Accordingly, the separation of field tester should be done by one of the following ways.

(1) CE panel is separated when the power supply to the MTC is OFF.

(2) CE panel may be separated when the power supply to the MTC is ON, but after that turn off the power supply to the MTC once and after a few seconds turn on the power supply again. When the power supply is turned on again, the MTC is always initialized into the online status.

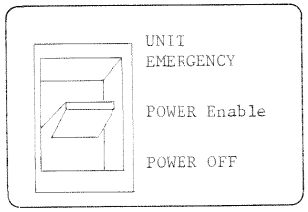
(3) When it is not desirable to turn off the power supply, the MTC can be initialized into the online status by manually clipping card pin BA8 on 1A07 column at 0 V.



MAP0120	How to Reset UEPO Switch

Because an emergency happened, UEPO SW was set to OFF; it cannot be set to Power Enable from the front.

After removing the cause of the emergency, open the rear door at buck of the unit and push the switch indicated by the arrow in Fig. 3 Rear View; the UEPO switch can be set to Power Enable.



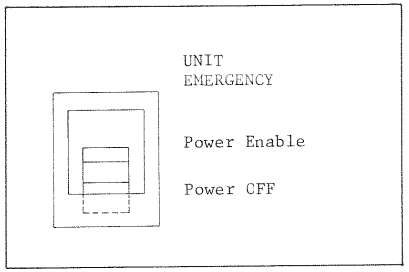


Fig. 1 Front view

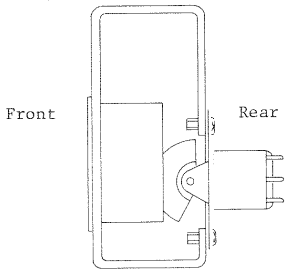


Fig. 2 Side view

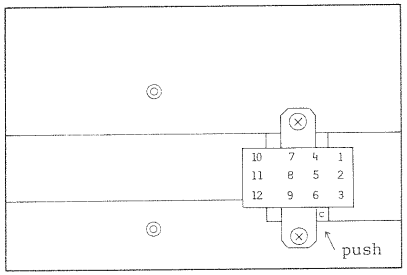
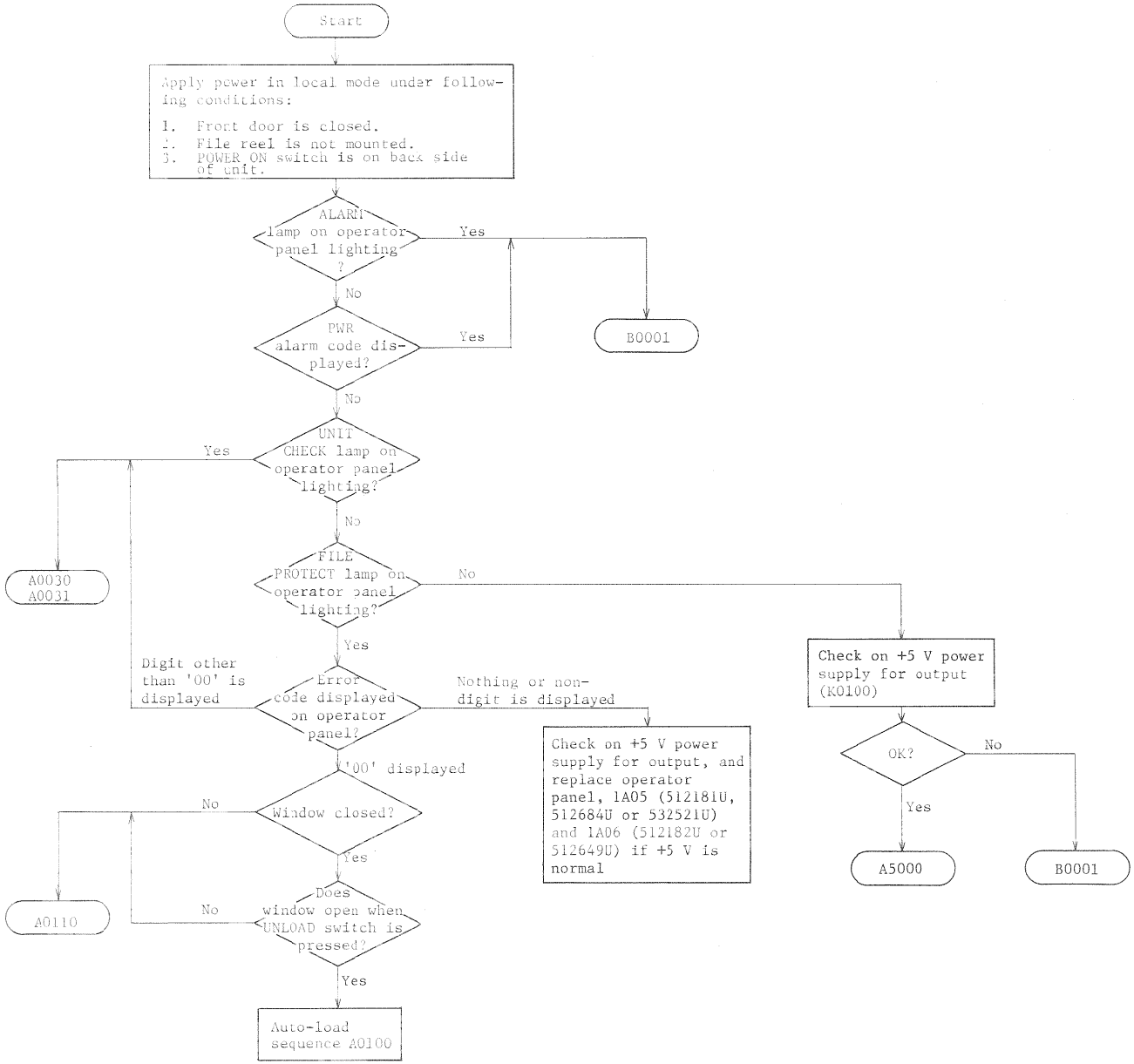


Fig. 3 Rear view

A0000 Pre-Check for Initial Operation



A0010	Error Code Assign Table (1)

1. Error codes listed in the following table each indicate the abnormal conditions occurring in arithmetic circuits, registers, timers, counters, or sense signal at the time of power on.

Error code	Content of error	Cause of error	MAP No.
00	Parity error of the ROM detected before starting execution of the microprogram. (When the Unit Check LED lights.)	Hard-ER	A0030
01	Faulty arithmetic operation of ALU (Arithmetic Logic Unit)	Hard-ER	A0030
02	Faulty execution of a subroutine of microprogram	Hard-ER	A0030
03	Faulty operation of register at file address $00 ∿ $03	Hard-ER	A0030
04	Faulty operation of register at file address $04 ∿ $07	Hard-ER	A0030
05	Faulty operation of register at file address $08 ∿ $0B	Hard-ER	A0030
06	Faulty operation of generated register at file address $0C ∿ $0F	Hard-ER	A0030
07	Faulty operation of timer 0 at file address $10	Hard-ER	A0030
08	Faulty operation of timer 1 at file address $11	Hard-ER	A0030
10	Faulty operation of the counter at file address $12	Hard-ER	A0030
11	Faulty operation of general register at file address $13	Hard-ER	A0030
12	Some of bits 0, 4, and 5 at file address $14 are wrong.	Hard-ER	A0031
13	Some of bits 0, 1, and 4 at file address $15 are wrong.	Hard-ER	A0031

Error code	Content of error	Cause of error	MAP No.
14	Faulty operation of general register at file address $18.		
15	Either bit 6 or bit 7 at file address $17 is wrong.	Hard-ER	A0031
16	Faulty operation of the register at file address $18	Hard-ER	A0030
17	Some of bits 0 to 5 in file address $19 are wrong.	Hard-ER	A0031
18	Some of bits 0 to 5 in file address $1A are wrong.	Hard-ER	A0031
19	Some of bits 3, 4, and 5 in file address $13 is wrong.	Hard-ER	A0031
20	Bit 0 in file address $1C is wrong.	Hard-ER	A0031
21	Some of bits 1, 2, 5, 6, and 7 in file address $1D are wrong.	Hard-ER	A0031
22	One of read data detecting signals TMSR0∿7 in file address $1E is erroneously set at '1'	Hard-ER	A0031
23	One of read data detecting signals TMSR0∿7 in file address $1E is erroneously set at '0'	Hard-ER	A0031
24	One of bits 0, 1, 2, 3, 4, 6, and 7 in file address $1F is erroneously set at '1' or bit 5 is erroneously set at '0'	Hard-ER	A0031
25	One of bits 2, 3, and 4 in file address $1F is erroneously set at '0' or bit 5 is erroneously set at '1'	Hard-ER	A0031

A0011	Error Code Assign Table (2)

2. Abnormality of internal components

Error code	Content of error	Cause of error	MAP No.
28	A parity error was detected in ROM during the execution of an instruction	Hard-ER	A0030
29	A parity error occurred in register LSI in file address $00 to $0B.	Hard-ER	A0030

3. Abnormality in the servo off status

Error code	Content of error	Cause of error	MAP No.
30	Current flows even after resetting the error marker drive.	Hard-ER	A0043 A6000
31	The window does not close within a prescribed time.	OP-Miss Hard-ER	A0110
32	Reel Hub Lock signal was erroneously detected.	Hard-ER	A0041
35	Door open was detected during unloading.	OP-Miss Hard-ER	A0420
36	File Column In Signal is not set to OFF state during unloading.	Hard-ER	A3020
37	Machine Column In signal is not set to OFF state during unloading.	Hard-ER	A3020
38	Tape Present signal is not set to OFF state when the tape is wound up by both reels for a contain prescribed time during unloading.	Hard-ER	A3030
39	Failure of forced unload		

4. Abnormality during auto loading

Error code	Content of error	Cause of error	MAP No.
40	Door open was detected during auto loading.	OP-Miss Hard-ER	A0420
41	Cartridge does not open.	Hard-ER	A0120
42	The low tape cannot be detected within a prescribed number of rotations of the machine reel.	Hard-ER	A0300
43	Auto hub is not locked.	Hard-ER	A0320
44	Load/rewind or Unload key pressed while door had opened.		
45	The window is not closed.	Hard-ER	A0110
46	File Column In signal was erroneously detected.	Hard-ER	A0310
47	Machine Column In signal was erroneously detected.	Hard-ER	A0310
48	Tape Present signal is detected even after the tape is wound up for load retry.	Hard-ER	A3030
49	The tape has not passed the BOT/EOT sensor (Tape Present signal is not detected.)	Hard-ER	A0350
50	Reel Loaded signal was erroneously detected.	Hard-ER	A0360
51	Reel Loaded signal is not detected.	Hard-ER	A0360
52	The length from the starting tip of tape to the BOT marker is too short.	OP-Miss	A0380
53	BOT marker cannot be detected within a certain prescribed distance.	OP-Miss Hard-ER	A0400
54	Machine Column In signal is not detected.	Hard-ER	A0310
55	File Column In signal is not detected.	Hard-ER	A0310
56	Loop alarm was detected after machine reel column in.	Hard-ER	A0430
57	Loop alarm was detected after file reel column in.	Hard-ER	A0430

A0012	Error Code Assign Table(3)

5. Abnormality in the servo on status

Error code	Content of error	Cause of error	MAP No.
60	Loop alarm in file reel column is detected when the capstan speed down (HSCF) is on.	Hard-ER	
61	Loop alarm in file reel column is detected when the capstan speed down (HSCF) is off.	Hard-ER	A0170 A2000
62	Loop alarm in machine reel column is detected when the capstan speed down (HSCM) is on.	Hard-ER	A0170
63	Loop alarm in machine reel column is detected when the capstan speed down (HSCM) is off.	Hard-ER	A0170 A2000
64	Reel hub lock was released.	Hard-ER	A0320
65	Door open was detected.	Hard-ER	A0420
66	Left tape-loop alarm detected in servo-on state (HSCF = 1)		
68	Window open detected while tape running	Hard-ER	A0460
69	Failure of auto-cleaner while tape running	Hard-ER	A0470

6. Abnormality in the capstan system

Error code	Content of error	Cause of error	MAP No.
70	Tacho pulse cannot be detected when capstan motor is started.	Hard-ER	A0550
71	The phase of capstan tacho pulse A/B is wrong.	Hard-ER	A0550
72	Capstan repeats turning during position control. (Direction Detecting signal OD remains set at '1'.)	Hard-ER	A0500
73	Capstan does not turn back and forth during position control. (Direction Detecting signal OD remains set at '0'.)	Hard-ER	A0500
74	A range of stop position of capstan is too long (longer than ±36 QTP).	Hard-ER	A0450
75	The stop position of capstan is not stable even when servo lock is applied after capstan stops.	Hard-ER	A0450

A0013	Error Code Assign Table (4)

7. Abnormality in the read/write system

Error code	Content of error	Cause of error	MAP No.
80	Write voltage was turned to on during the read status, or write voltage is not turned to off within a prescribed time.	Hard-ER	A0330
81	Write voltage was turned to off during the write status, or write voltage is not turned to on within a prescribed time.	Hard-ER	A0330
82	Erase current was turned to on during the read status, or erase current is not turned to off within a prescribed time.	Hard-ER	A0330
83	Erase current was turned to off during the erase status, or the erase current is not turned to on within a prescribed time.	Hard-ER	A0330
84	An error occurred in the +12 V power supply.	Hard-ER	A0330
85	Write voltage could not be turned to on within a certain distance during write operation in the streaming mode.	Hard-ER	A0340
86	The file protect was turned to on during write erase operation.	OP-Miss Hard-ER	A5000
87	The file protect was turned to on during the DSE (Data Security Erase) operation.	OP-Miss Hard-ER	A5000
88	An error occurred in level setting for FE mode.	Hard-ER	A0044

8. Other abnormality

Error code	Content of error	Cause of error
99	Error occurs frequently in tape medium (Error is to be displayed after unloading is completed. However, the Unit Check LED is off.)	Tape medium Hard-ER

9. Abnormality during troubleshooting

Error code	Content of error	Cause of error	MAP No.
0	Capstan Tacho Pulse A is erroneously set at '0', or it remains at '0' for one cycle during high speed rotation.	Hard-ER	A0550
1	Capstan Tacho Pulse A is erroneously set at '1', or it remains at '1' for one cycle during high speed rotation.	Hard-ER	A0550
2	Capstan Tacho Pulse B is erroneously set at '0'.	Hard-ER	A0550
3	Capstan Tacho Pulse B is erroneously set at '1'.	Hard-ER	A0550
4	Duty of Capstan Tacho Pulse A is less than 40%.	Hard-ER	A0550
	Faulty operation of the error marker drive system system	Hard-ER	A6000
5	Duty of Capstan Tacho Pulse A is greater than 60%.	Hard-ER	A0550
	Faulty operation of the cartridge opener drive system	Hard-ER	A0120
6	Duty of Capstan Tacho Pulse B is less than 40%.	Hard-ER	A0550
	Faulty operation of the window drive system	Hard-ER	A0110
7	Duty of Capstan Tacho Pulse B is greater than 60%.	Hard-ER	A0550
8	The phase difference between Capstan Tacho Pulse A and B is less than 16%.	Hard-ER	A0550
9	The phase difference between Capstan Tacho Pulse A and B is greater than 34%.	Hard-ER	A0550

A0020	PCB Location

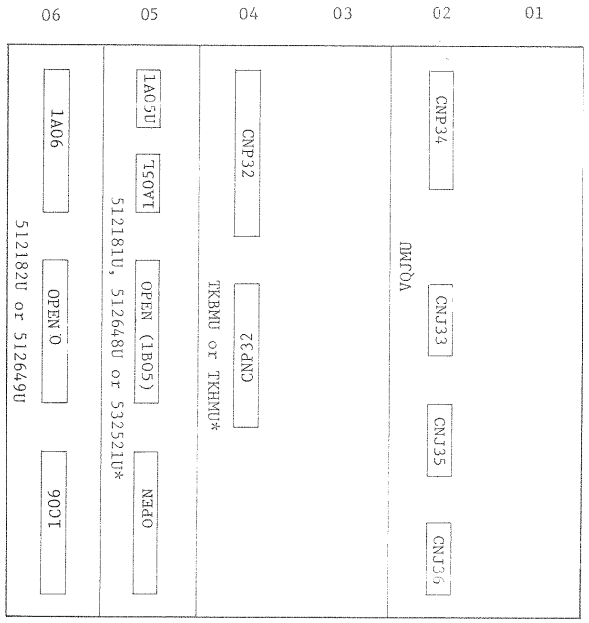
PCA location table

Location	Identifications	Designation
1A01		
1A02	B16B-7220-0020A#U	VQJMU
1A03		
1A04	B16B-7190-0020A#U or B16B-7190-0100A#U*	TKBMU or TKHMU*
1A05	C16B-5121-0810#U, C16B-5126-0480#U or C16B-5325-0210#U*	512181U, 512648U or 532521U*
1A06	C16B-5121-0820#U or C16B-5126-0490#U	512182U or 512649U

Note: The PCA marked * is used in 200 ips model.

Attentions at PCA replacement

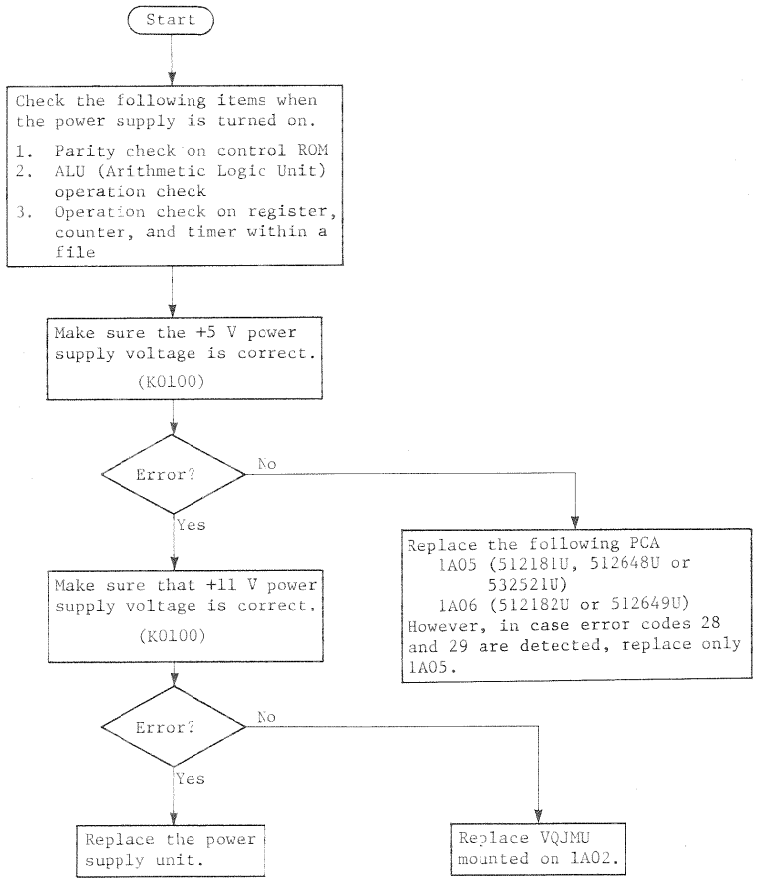
1. Turn off the power supply before the replacement.
2. When replacing the PCA at Cate Section, you must use the Extraction tool
   Extraction tool: P/N C960-0300-T001
3. Attend to bending of PCA contact at installation.
   When using Card Extender too, attend to bending in same as above.
   Card Extender: P/N C960-0030-T029
4. After replacement, connect the connector to the same position as before the replacement.



Install side view

A0030	Abnormality at the Time of Power On (1)

Error Code 00 ∿ 11, 16, 28, 29



A0031	Abnormality at the Time of Power On (2)

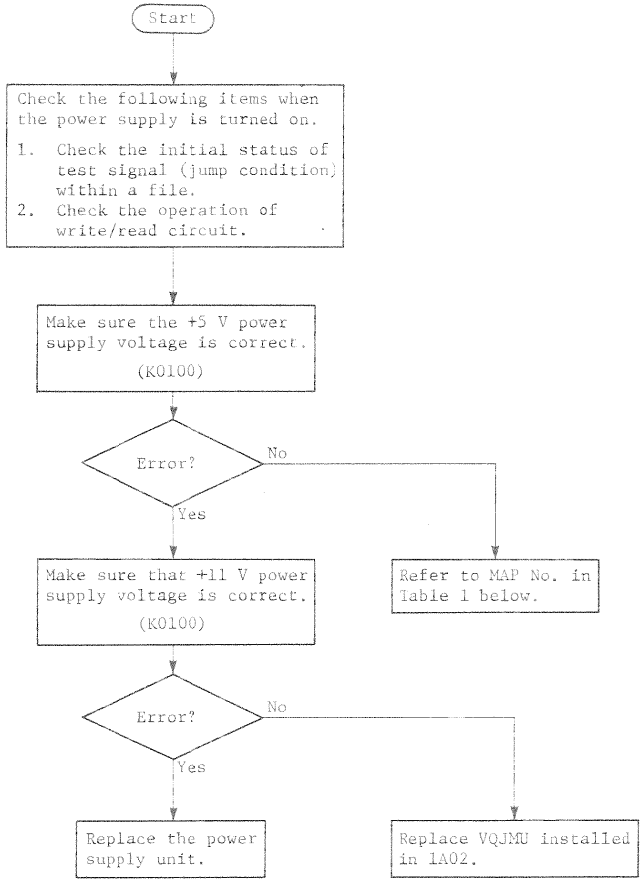
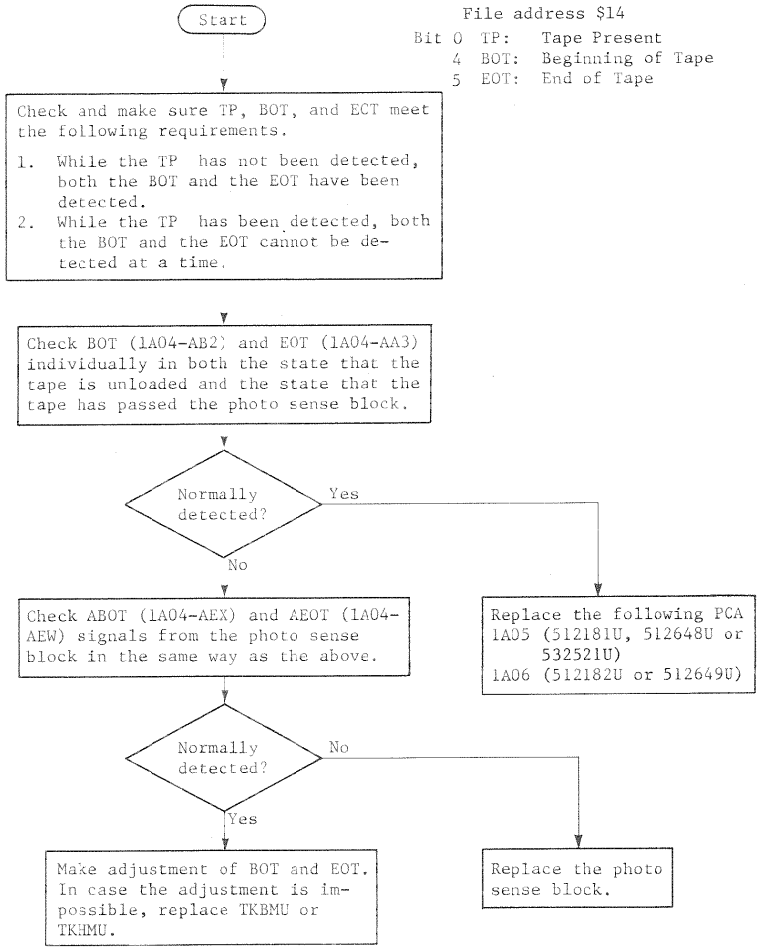
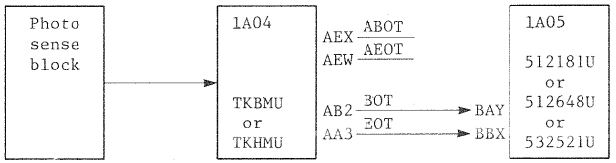


Table 1

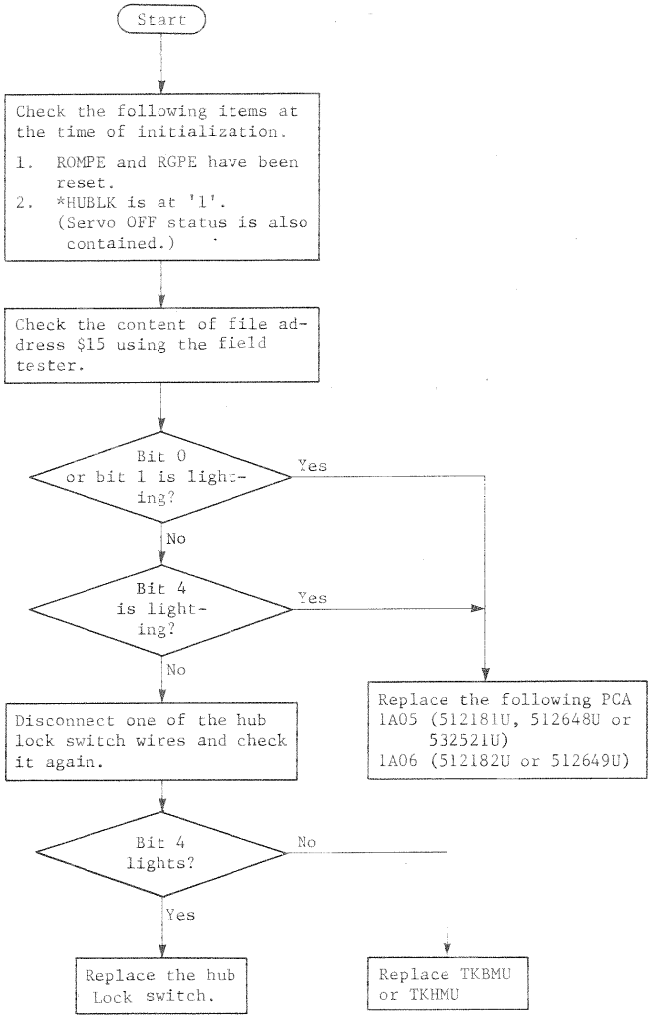
Error code	File address	Point of failure	Reference MAP No.
12	$14	There is inconsistency between three signals TP (Tape Present), BOT (Beginning of Tape), and EOT (End of Tape).	A0040
13	$15	Either ROMPE (ROM Parity Error) signal, RGPE (Register Parity Error) signal, or HUBLK (Hub Lock) signal is set.	A0041
15	$17	Either TSFL (Test Flag) signal or TST (Test Start) signal is set.	Replace the following PCA 1A05 (5121810) 1A06 (5121820)
17	$19	Either ONL (Online), INTRP (Interruption), UCHLD (Unit Check Hold), TUCHK (Tape Unit Check), GAPCT (Gap Control), or TWA (Tape Warning Area) signal is set.	
18	$1A	Either RTLAL (Right Tape Loop Alarm), LTLAL (Left Tape Loop Alarm), HUBAL (Hub Lock Alarm), ECER (Erase Circuit Error), WCER (Write Circuit Error), or WRIST (Write/Read PCA Installed) is wrong.	A0042
19	$1B	Either CLINF (Column In File), CLINM (Column In Machine), or EMMVD (Error Marker Moved) signal has been detected.	A0043
20	$1C	Failure in STEP6 (Step 6 ALL) - PE level setting operation	A0044
21	$1D	Either WVON (Write Voltage ON), ECON (Erase Current ON), AGCOK (SAGC OK), or VEL0.1 (Velocity Mode 0.1) signal is wrong.	A0045
22	$1E	One of TMSR0∿7 (Time Sensor 0∿7) is erroneously set at '1'.	A0046
23		One of TMSR0∿7 (Time Sensor 0∿7) is erroneously set at '0'.	
24	$1F	Either GOB (Go Tag), STS (Status Tag), TMSR8 (Time Sensor 8), DNOIS (Detected Noise), DBOB (Detected Beginning of Block), DTM (Detected Tape Mark), or 0 (Logical '0') signal is erroneously set at '1', or DIBG (Detected Inter Block Gap) signal is erroneously set at '0'.	A0046
25		Either TMSR8, DNOIS, or DBOB signal is erroneously set at '0', or DIBG signal is erroneously set at '1'.	

A0040	Abnormality on BOT and EOT





A0041	Abnormality on File Address $15

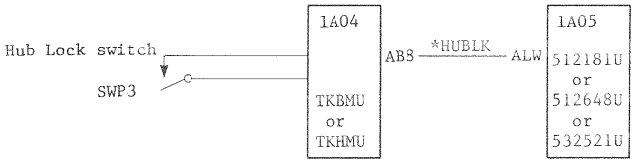


File address $15

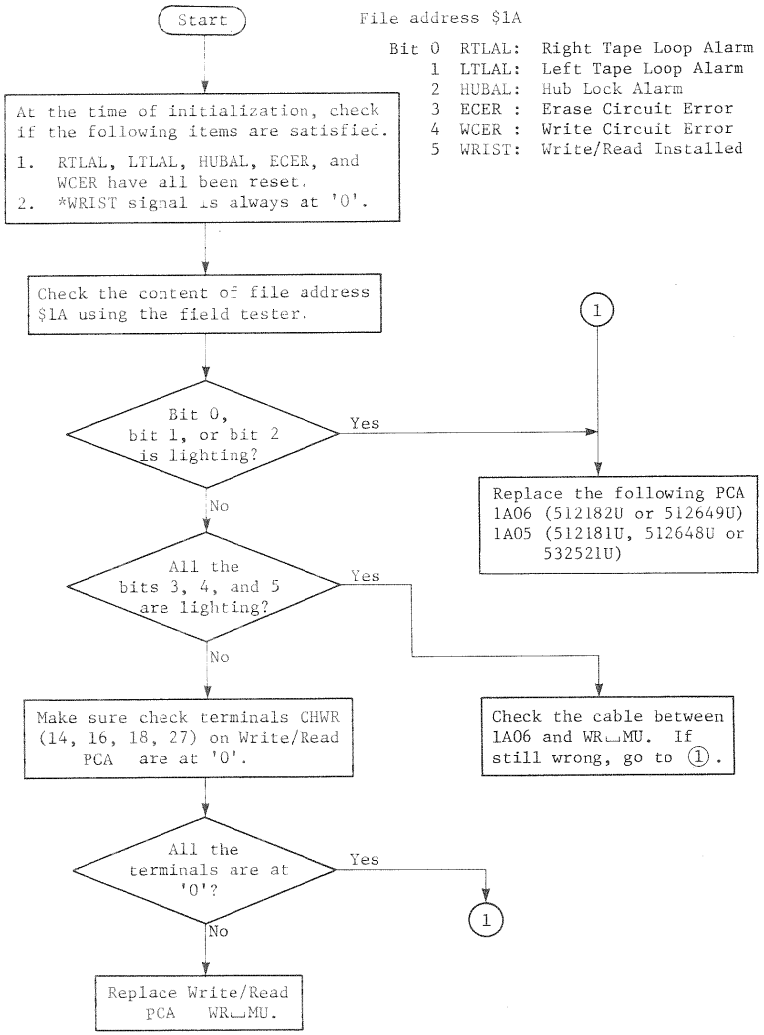
Bit 0 ROMPE: ROM Parity Error

1 RGPE : Register Parity Error

4 *HUBLK: Hub Lock



A0042	Abnormality on File Address $1A (Error Code = 18)



File address $1A

Bit 0	RTLAL:	Right Tape Loop Alarm
1	LTLAL:	Left Tape Loop Alarm
2	HUBAL:	Hub Lock Alarm
3	ECER :	Erase Circuit Error
4	WCER :	Write Circuit Error
5	WRIST:	Write/Read Installed

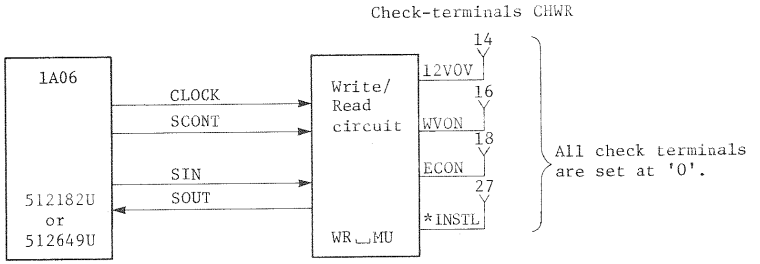


Fig. 1

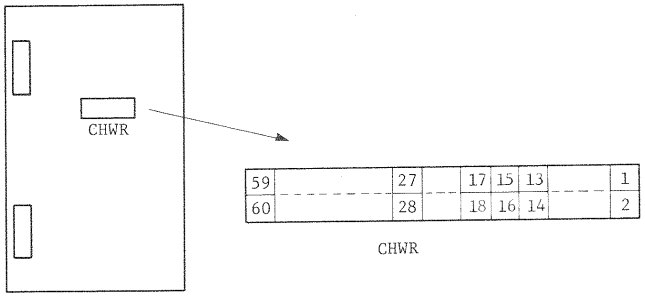


Fig. 2 Write/Read printed-circuit assembly (WR␣MU)

A0043	Abnormality on File Address $1B

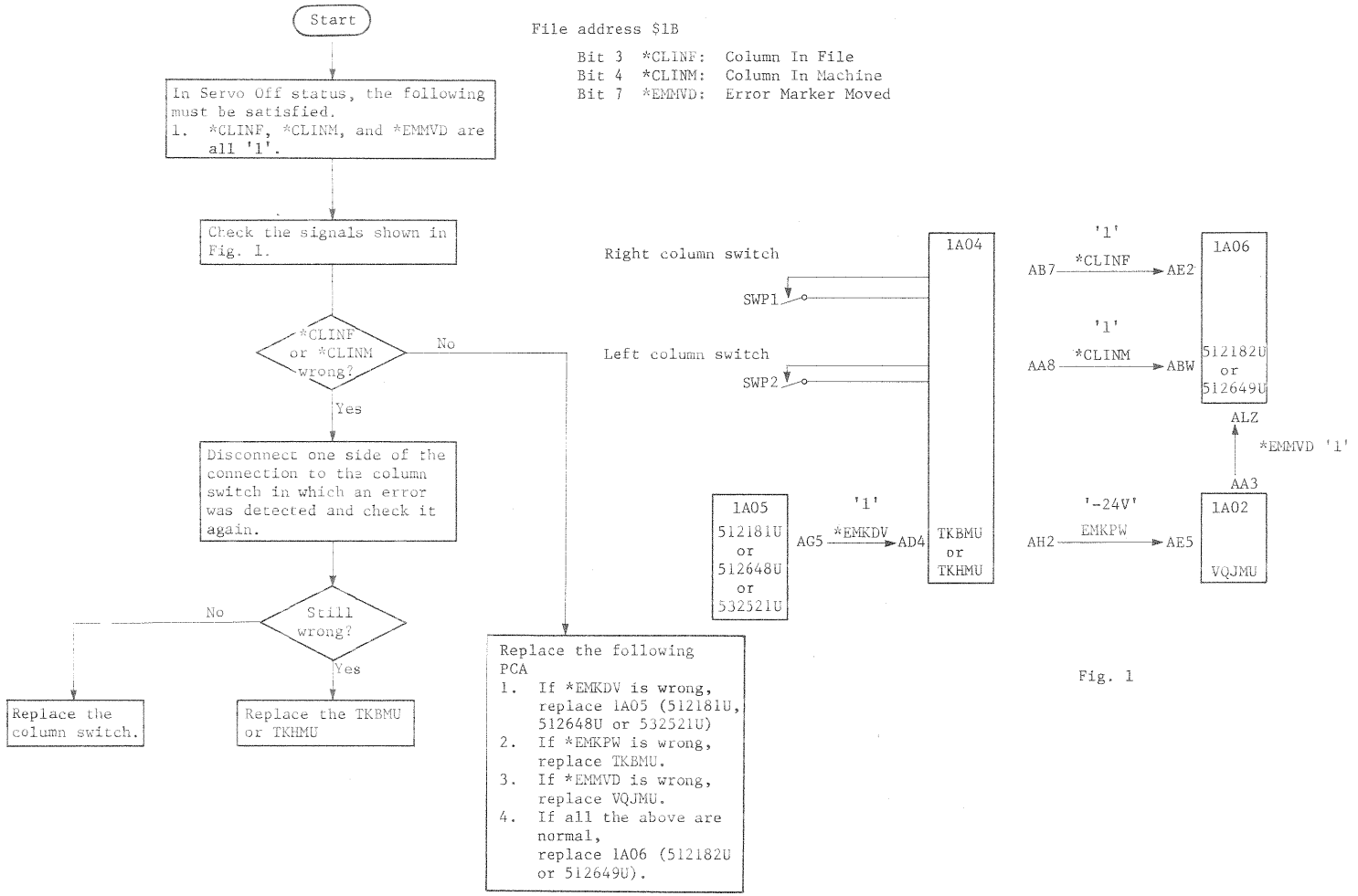
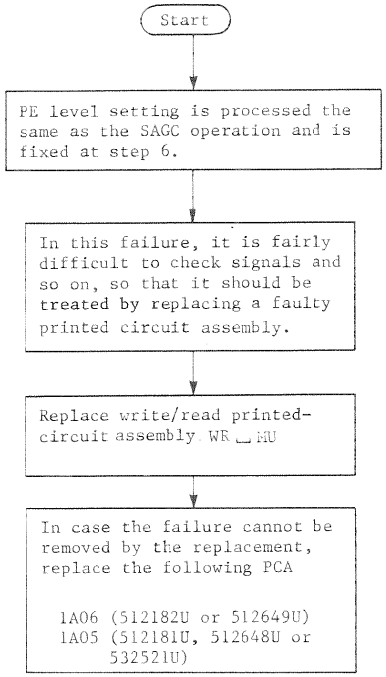


Fig. 1

A0044	Faulty PE Level Setting



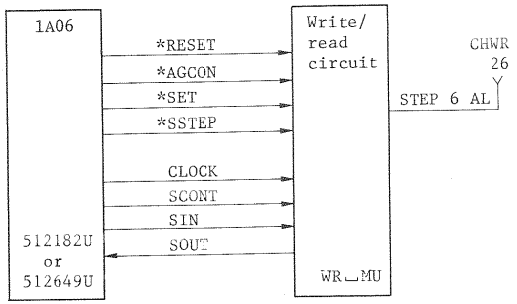
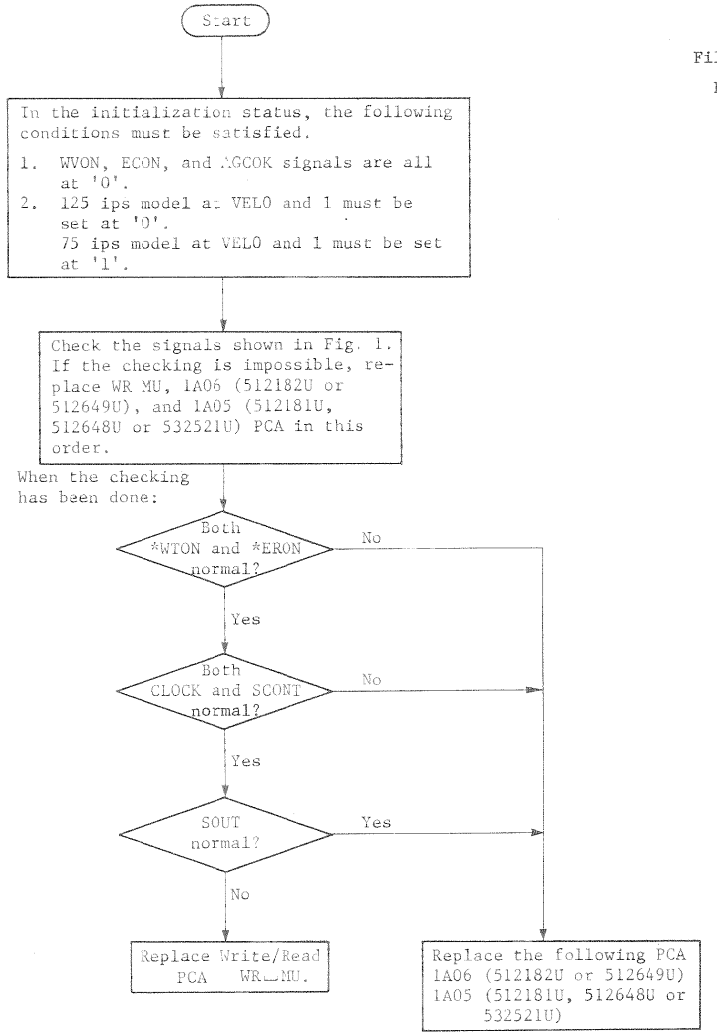


Fig. 1

A0045	Abnormality on File Address $1D (Error Code = 21)



File address $1D

Bit 1 WVON : Write Voltage ON
2 ECON : Erase Current ON
5 AGCOK: SAGC OK
6 VEL0 : Velocity Model 0
7 VEL1 : Velocity Model 1

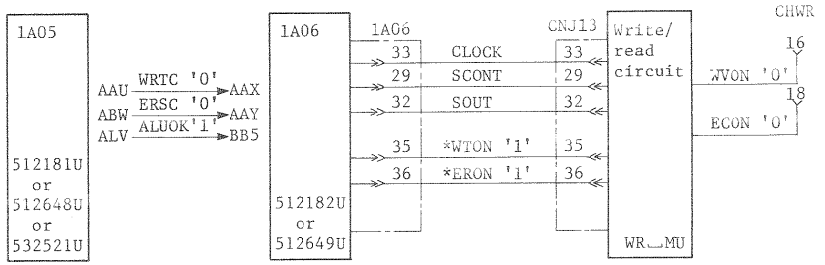


Fig. 1

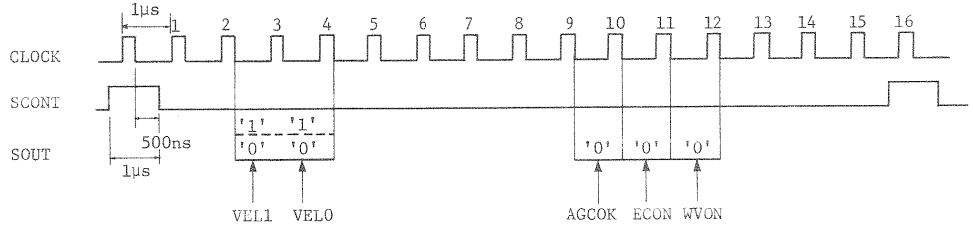
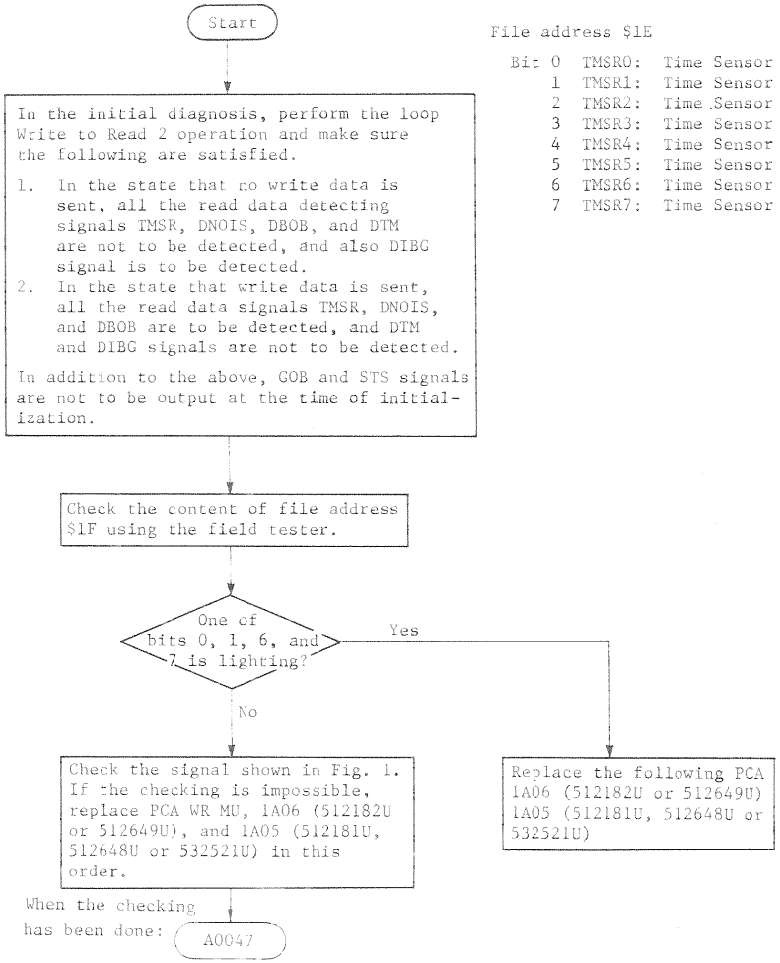


Fig. 2

A0046	Abnormality on File Address $1E and $1F (Error Codes = 22 to 25)



File address $1E

Bit	0	TMSR0:	Time Sensor 0
	1	TMSR1:	Time Sensor 1
	2	TMSR2:	Time Sensor 2
	3	TMSR3:	Time Sensor 3
	4	TMSR4:	Time Sensor 4
	5	TMSR5:	Time Sensor 5
	6	TMSR6:	Time Sensor 6
	7	TMSR7:	Time Sensor 7

File address $1F

Bit	0	GOB :	Go Tag
	1	STS :	Status Tag
	2	TMSR8:	Time Sensor 8
	3	DNOIS:	Detected Noise
	4	DBOB :	Detected Beginning of Block
	5	DIBG :	Detected Inter Block Gap
	6	DTM :	Detected Tape Mark
	7	0 :	Logical '0'

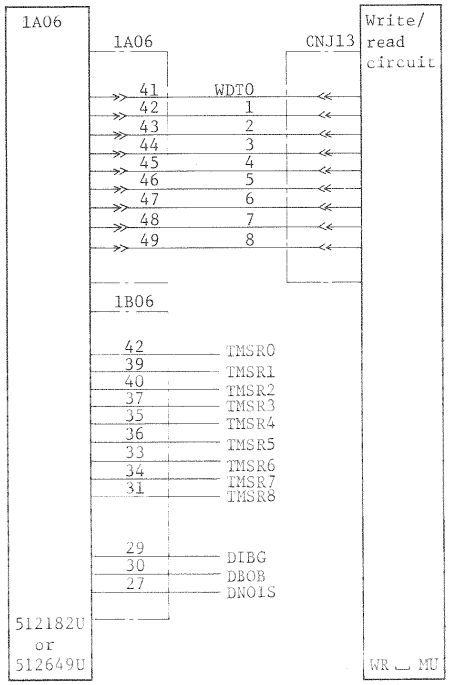
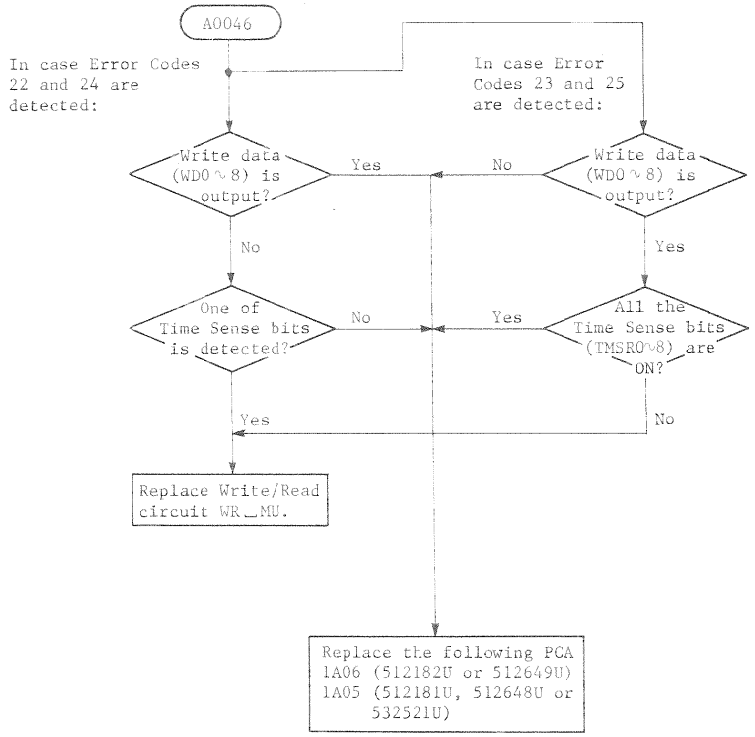


Fig. 1

A0047	Abnormality on File Addresses $1E and $1F



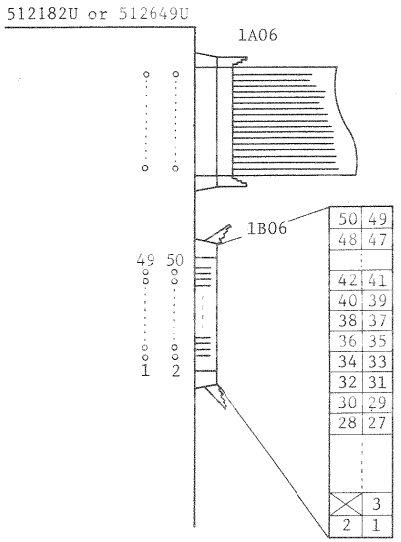
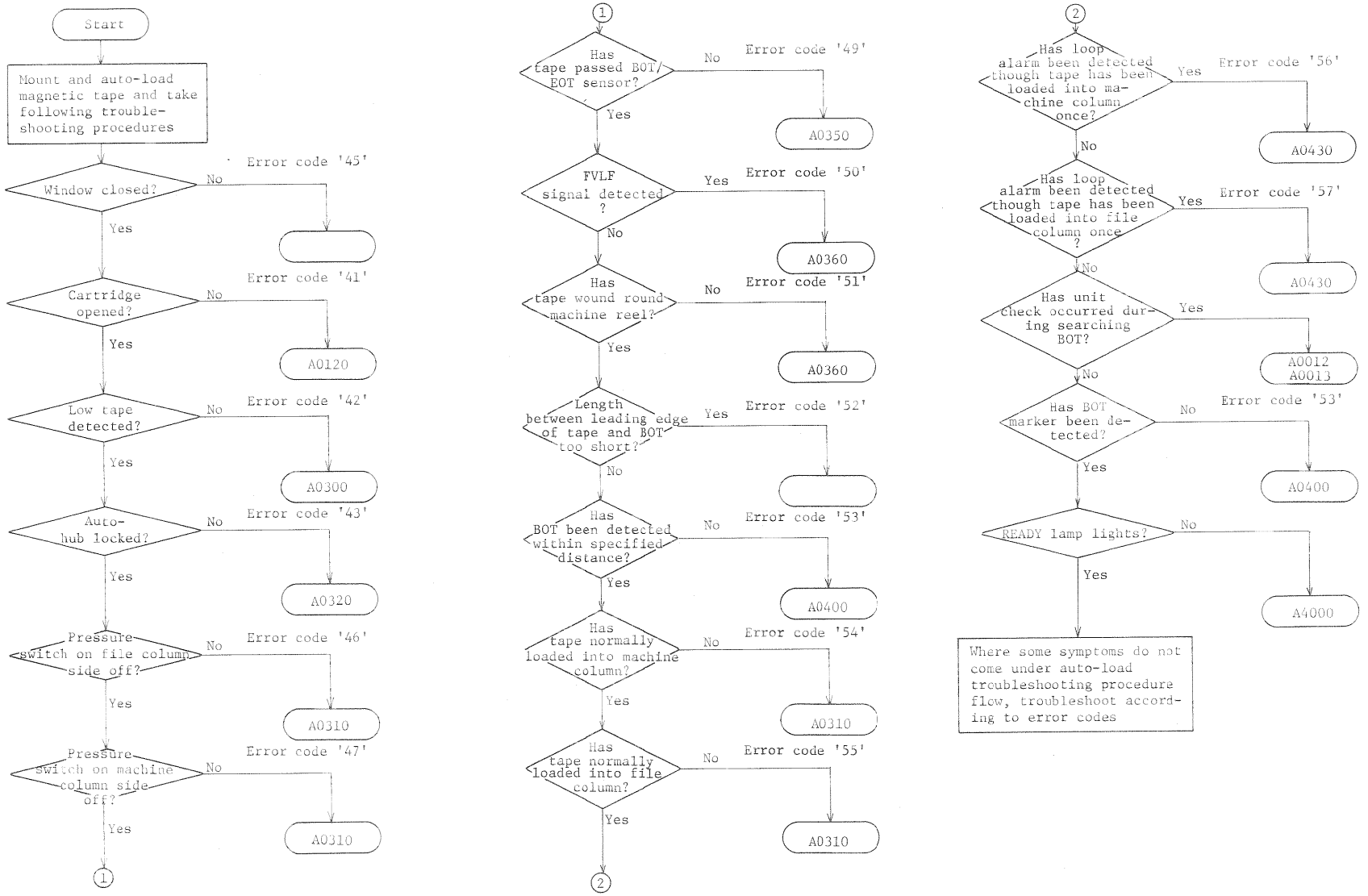
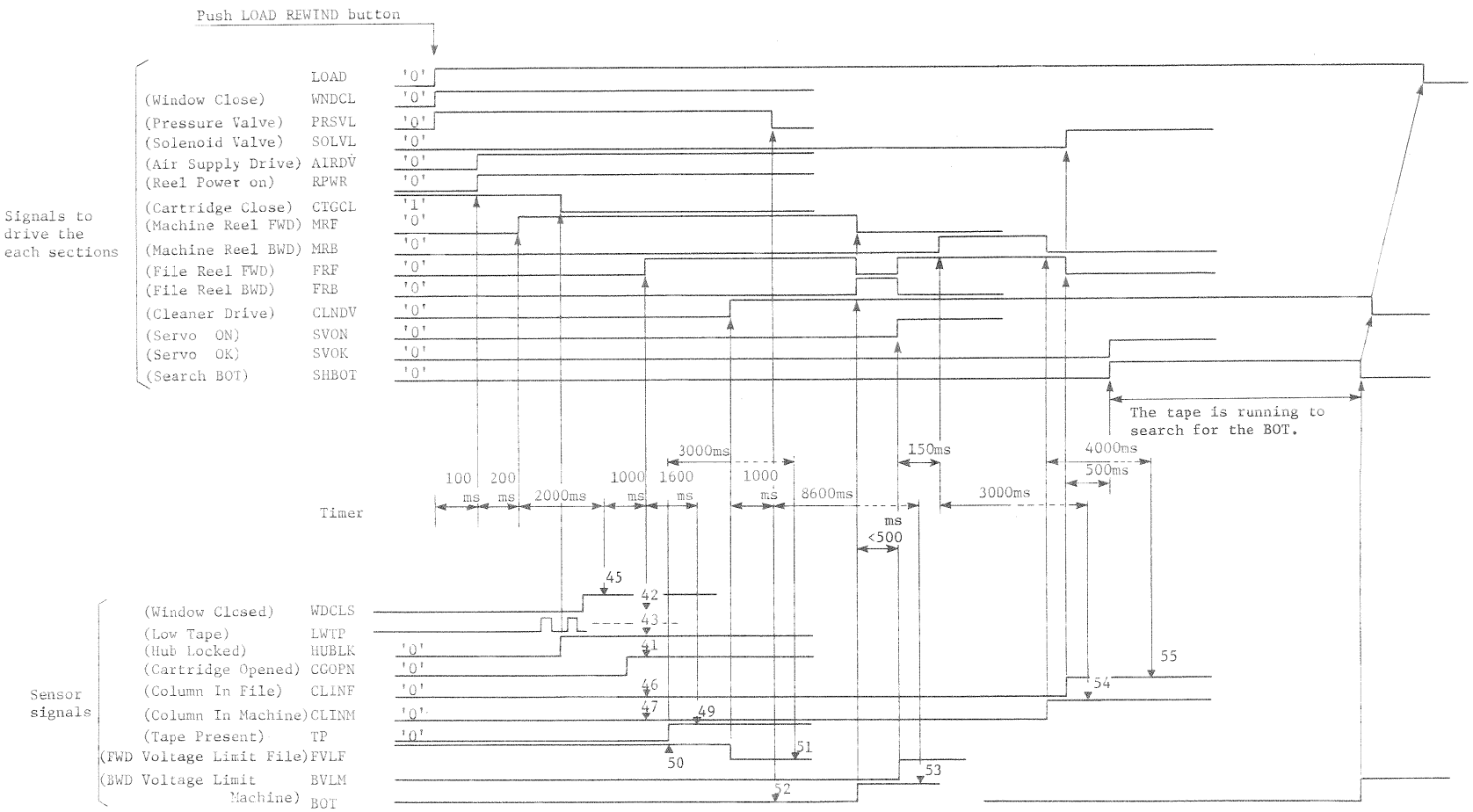


Fig. 2

A0100	Auto Load Troubleshooting



A0101	Auto Load Timing Chart



Note: The marks '▼' indicate the timings when the program checks the logical level of each sensor during auto loading. The hexadecimal number in upper of the mark '▼' means Error code which is set to ER register.

A0110	The Window does not Open/Close.

Start

Symptom: Window open/close failure is due to drive system, microprograms, or mechanism

PWR alarm due to overcurrent (code 4) detected?

Yes

Remove cover on inside of front door and check/replace following:

1. Check on actuators of window open and window close switches (SW1 and SW2) for folding/bending.
2. Check on micro switches for operation when opened/closed.
3. Replace TVAMU.
4. Replace window motor.

No

Remove cover on inside of front door and check that no failure occurs in drive motor, belts, pulley, and open and close switches

Check with field tester on bit 3 of file address $04 for signal (WNDCL), with front door closed, by taking following steps:

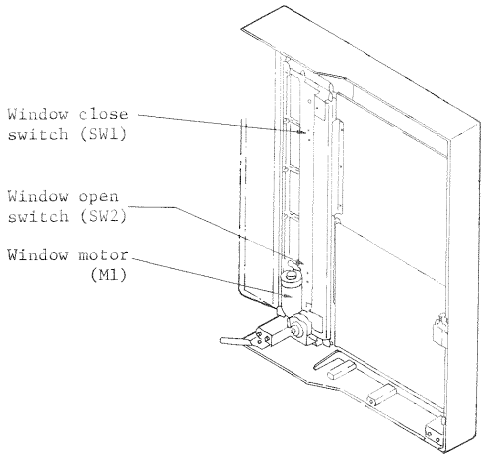
1. Press RESET switch:
   ... WNDCL='1' (LED lights.)
2. Press UNLOAD switch:
   ... WNDCL='0' (LED goes out.)

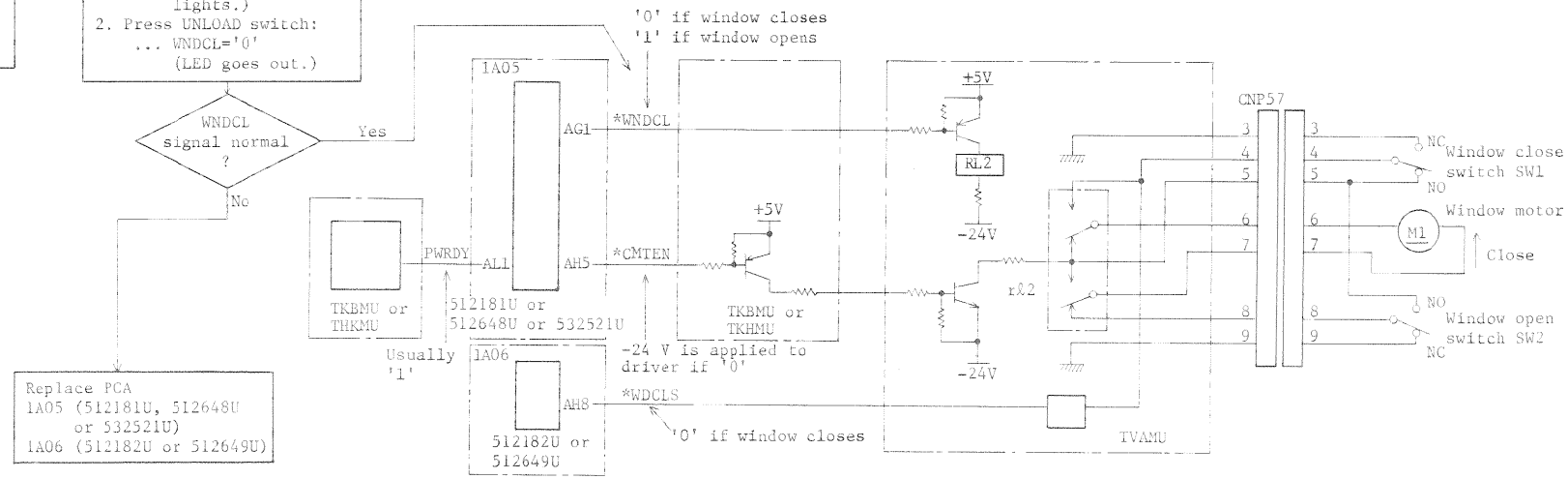
WNDCL signal normal ?

Yes

No

Replace PCA
1A05 (512181U, 512648U or 532521U)
1A06 (512182U or 512649U)





A0120	Cartridge does not Open/Close.

Start

Symptom:

If magnetic tape with cartridge is mounted, micro switch in cartridge sensor (Fig. 1) operates; if command code $B1 is set by field tester, cartridge opens/closes

Perform following:

1. Check on cartridge sensor for detect signal
2. Check that CARTRIDGE OPEN/CLOSE switch is correctly operating

Check with field tester on bit 2 of file address $04 for signal (CTGCL), with front door closed, by taking following steps:

1. Issue command does $B1 from field tester in order to set SSS switch to on:
   ... CTGCL='0' (LED goes out.)
2. Set SSS switch to on once more:
   ... CTGCL='1' (LED lights.)

CTGCL signal normal ?

Yes

No

Replace PCA 1A05 (512181U, 512648U or 532521U) and 1A06 (512182U or 511649U)

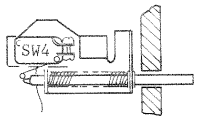


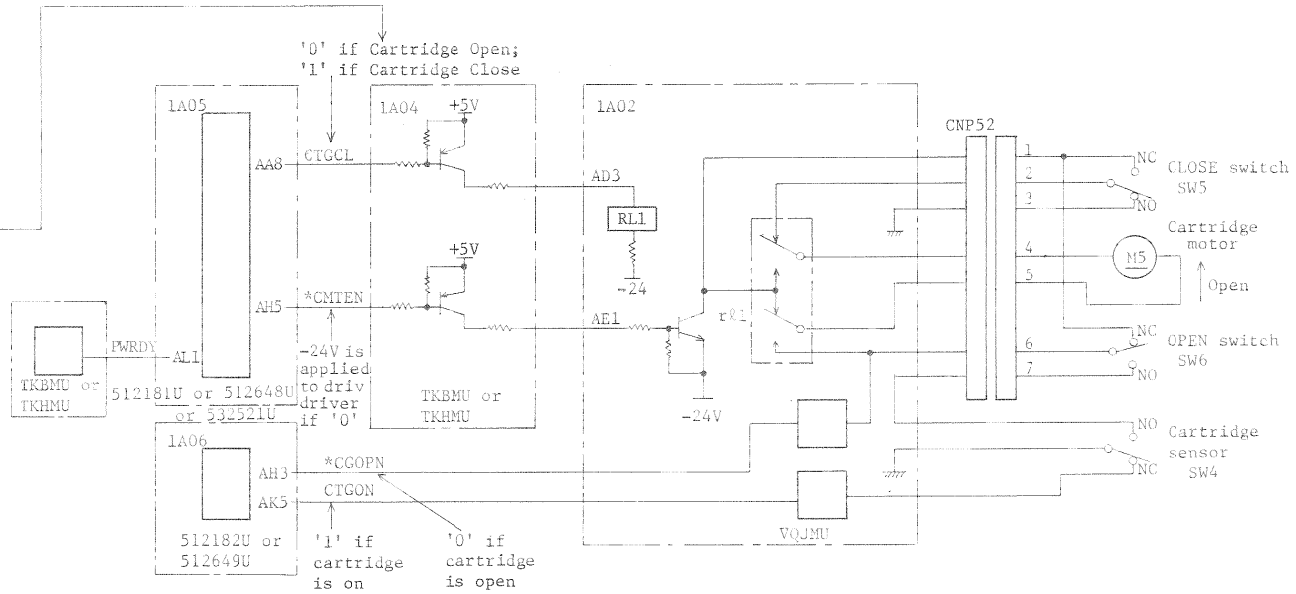
Fig. 1 Cartridge sensor

Cartridge close switch (this side)

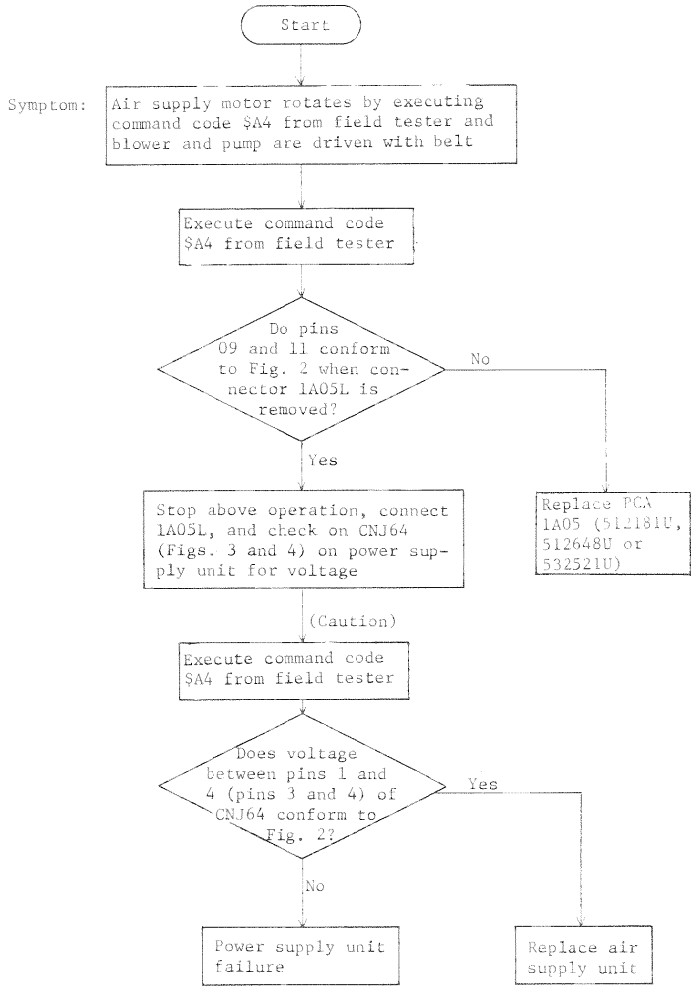
Cartridge open switch (other side)

Cartridge sensor

Fig. 2 Cartridge opener
(Viewed with the plate removed.)



A0130	Air Supply Motor does not Rotate.



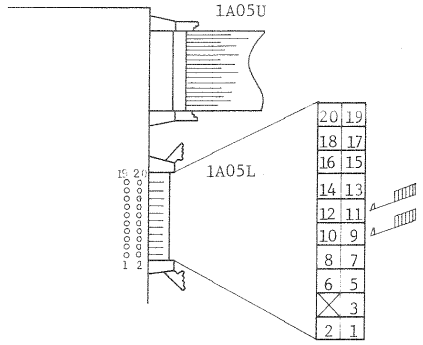


Fig. 1 Logic PCA at 1A05

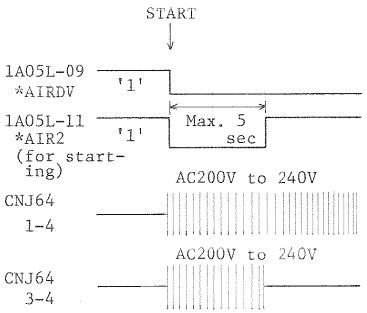


Fig. 2 Timing chart

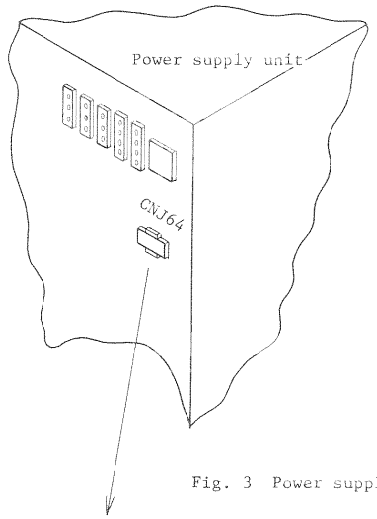


Fig. 3 Power supply unit

CNJ64

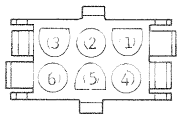


Fig. 4

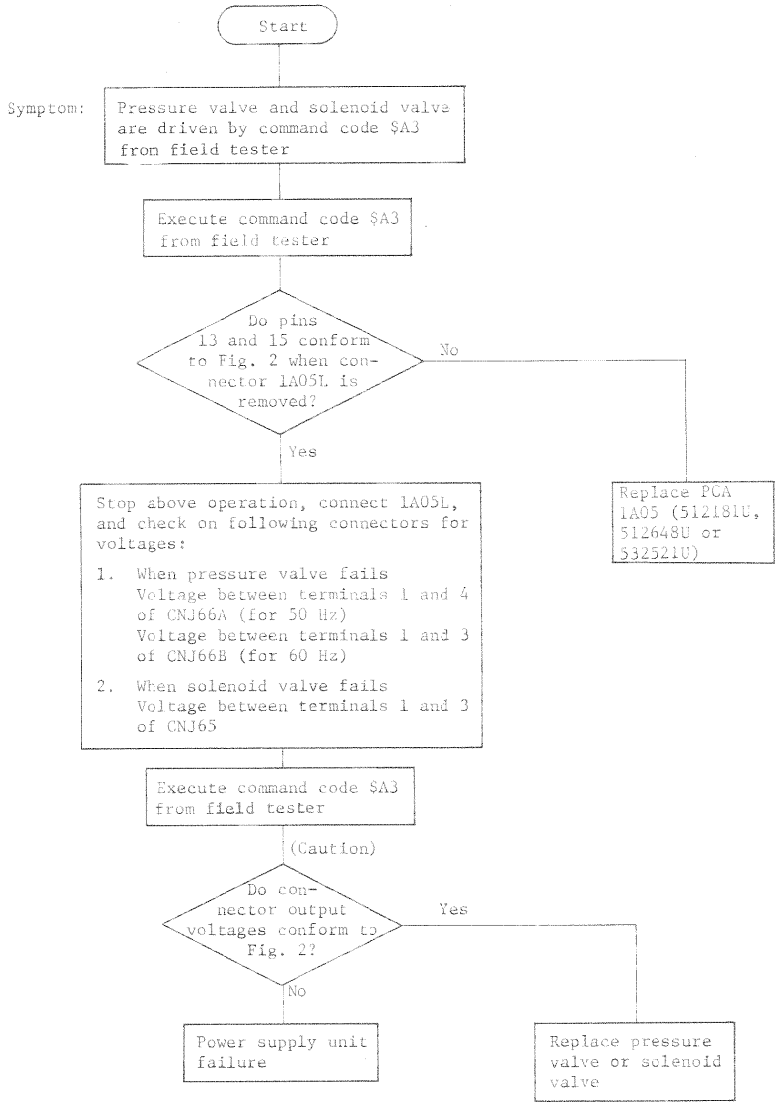
CAUTION

Special attention must be paid to checking in this area because dangerous voltage exists in the connector CNJ64.

Measurement points (connector pin number)

CNJ64 1-4 and 3-4

A0131	Pressure and Solenoid Valves do not Work



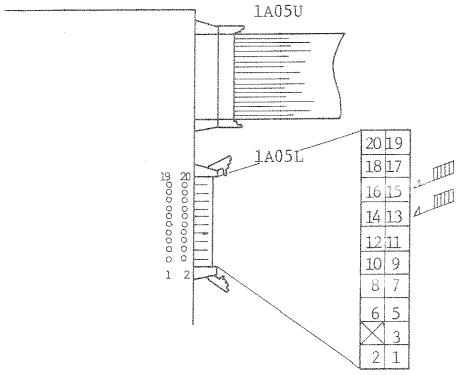


Fig. 1 Logic PCA at 1A05

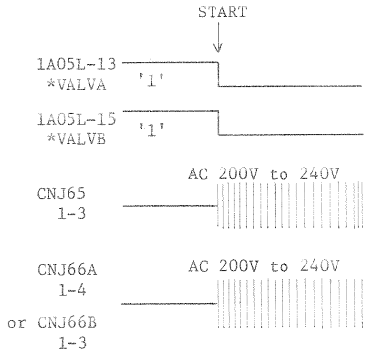


Fig. 2

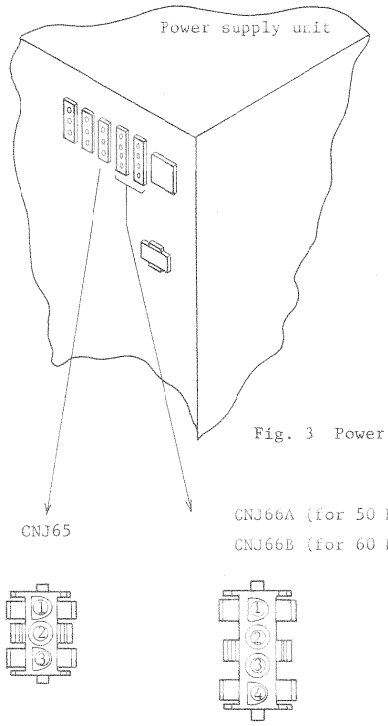


Fig. 3 Power supply unit

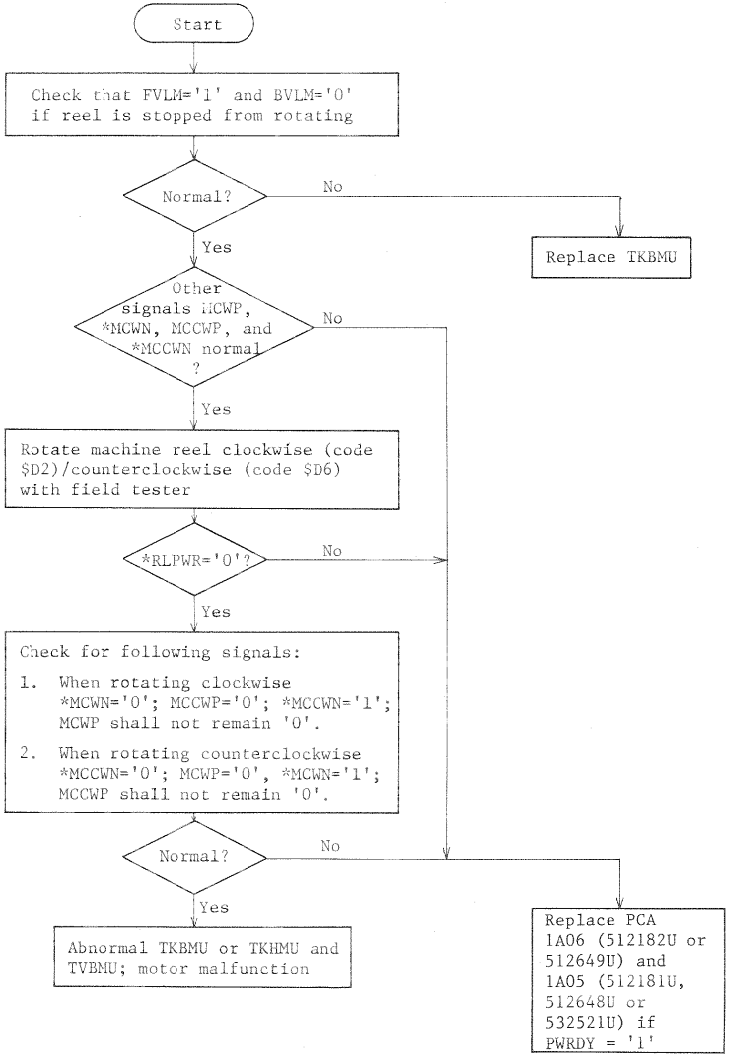
Fig. 4

CAUTION

Special attention must be paid to checking in this area because dangerous voltage exists in the connector CNJ65 and CNJ66A/B.
Measurement point (Connector pin number)

A0140	Machine Reel Motor Trouble

Symptom: The machine reel does not rotate during unloading/loading tape.



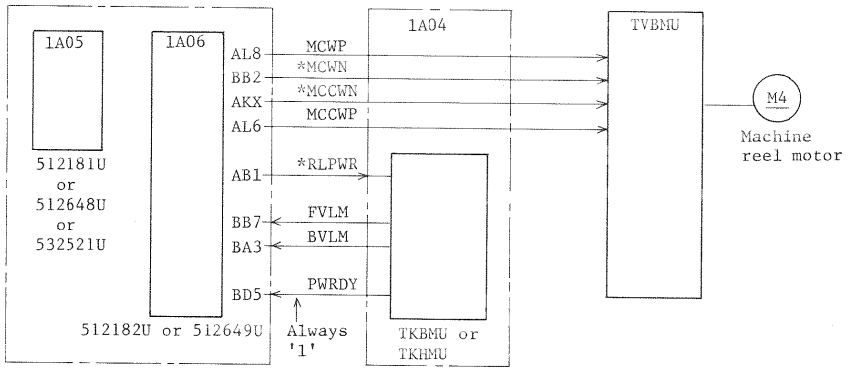


Fig. 1

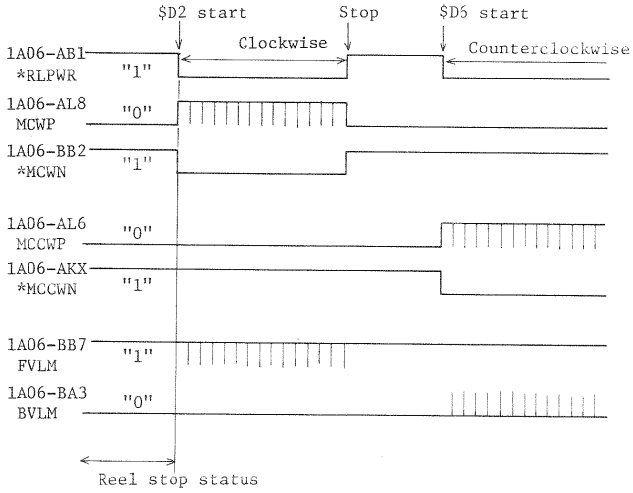
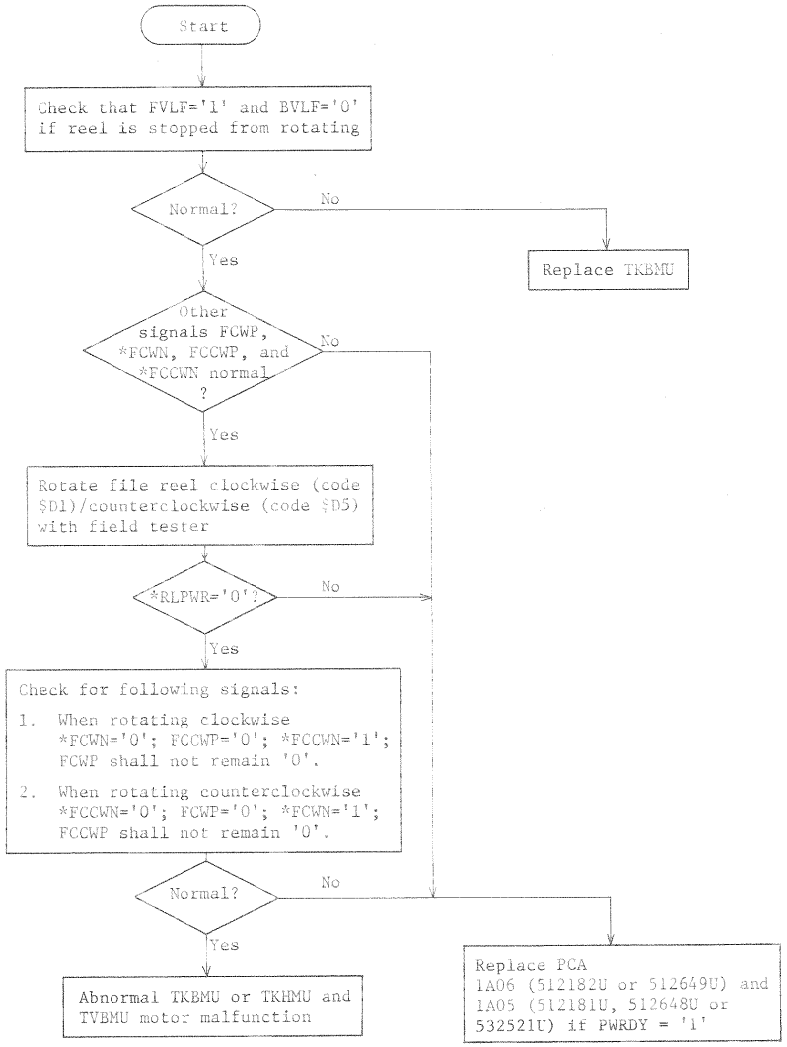


Fig. 2

A0141	File Reel Motor Trouble

Symptom: The file reel does not rotate during loading/unloading tape.



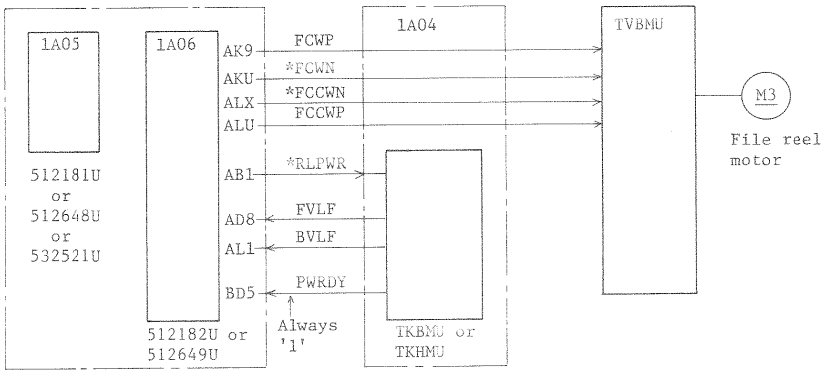


Fig. 1

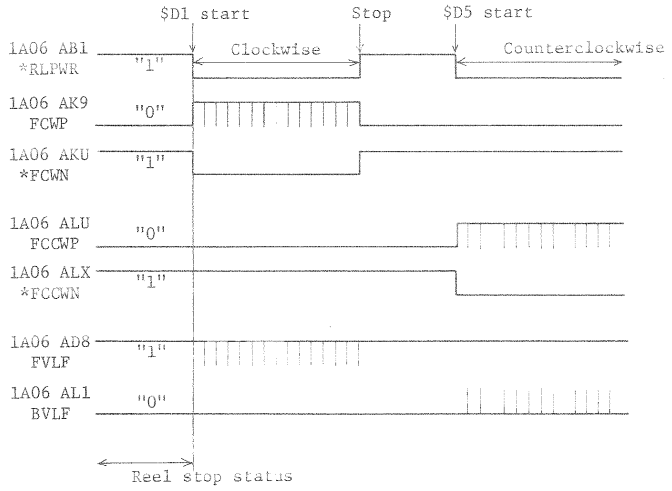
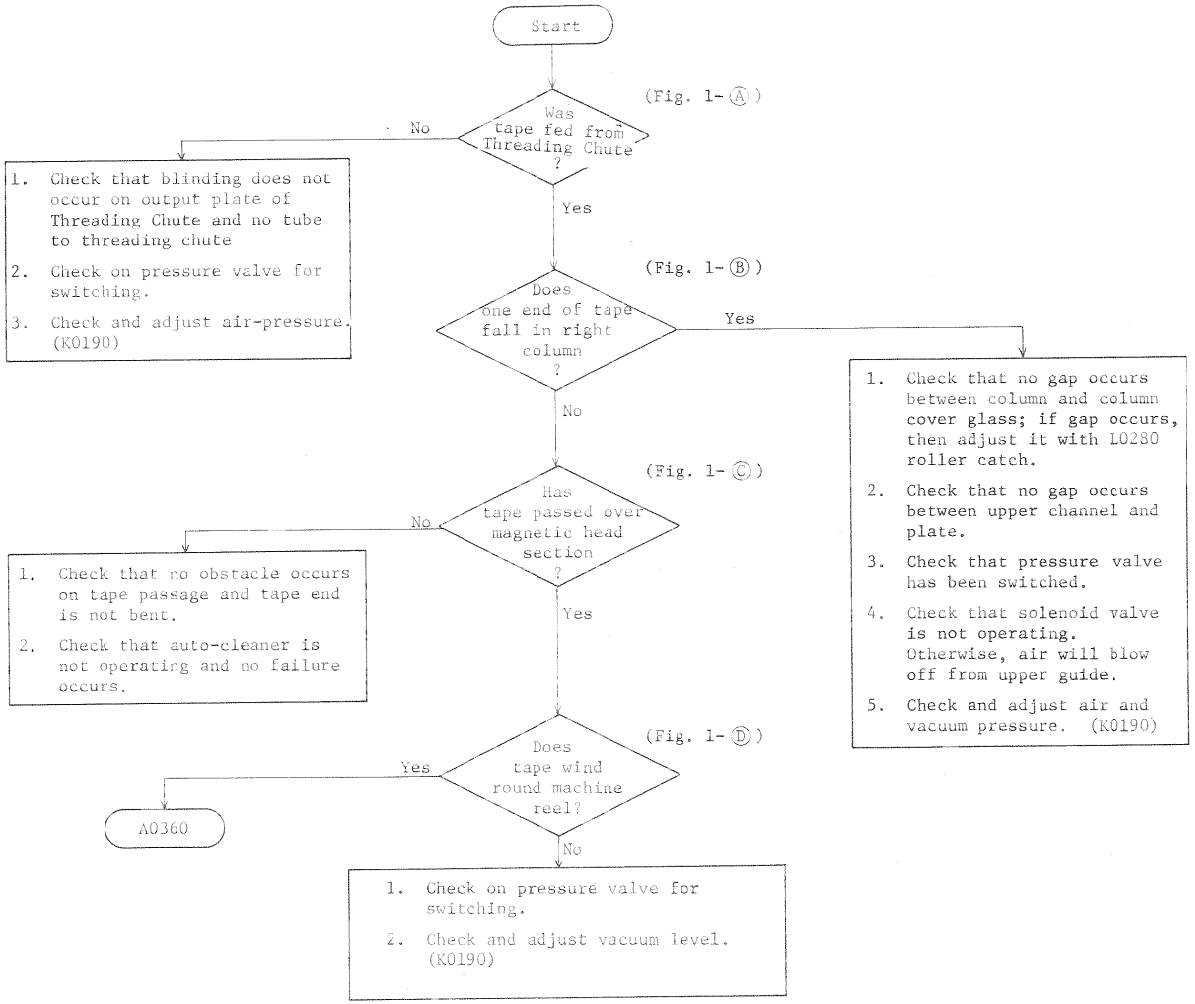


Fig. 2

A0150	Tape is not wound to the Machine Reel

Symptom: Tape does not wind round machine reel even though it has been loaded from file reel; tape running trouble has occurred.



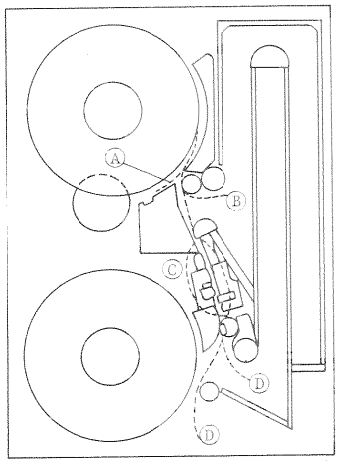
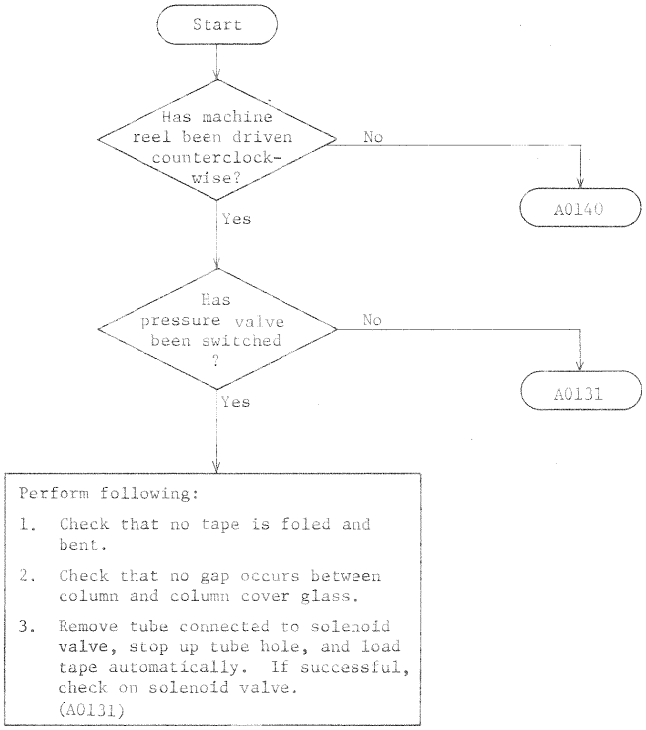
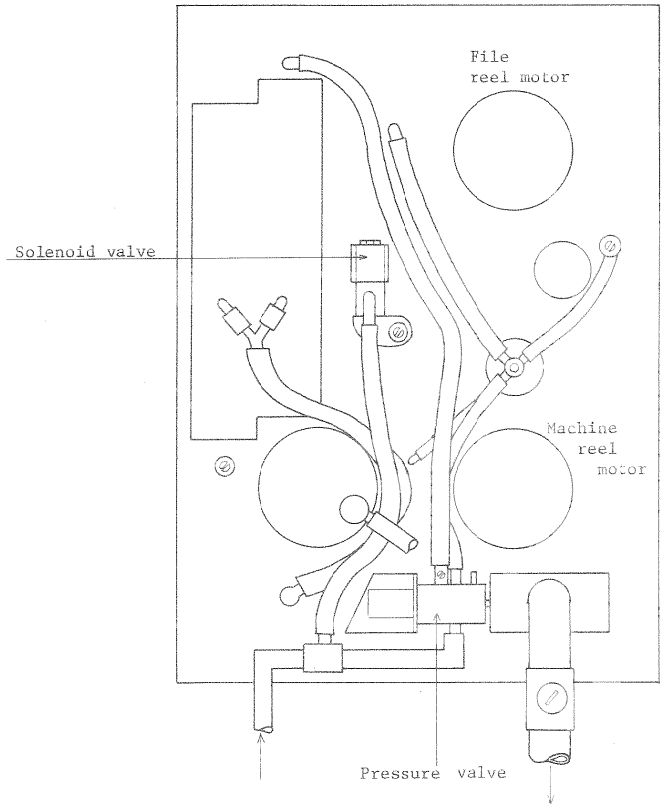


Fig. 1

A0160	Column-In Fail

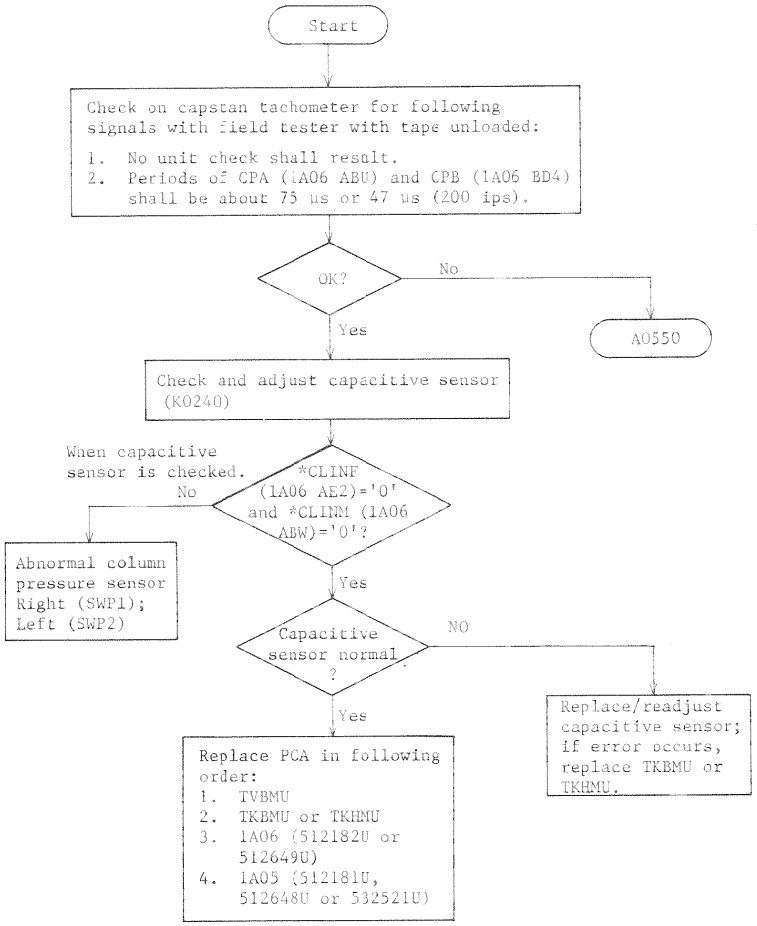
Symptom: Machine reel is driven counterclockwise and tape is loaded into both columns if tape has wound round machine reel and BOT detected during automatic loading.



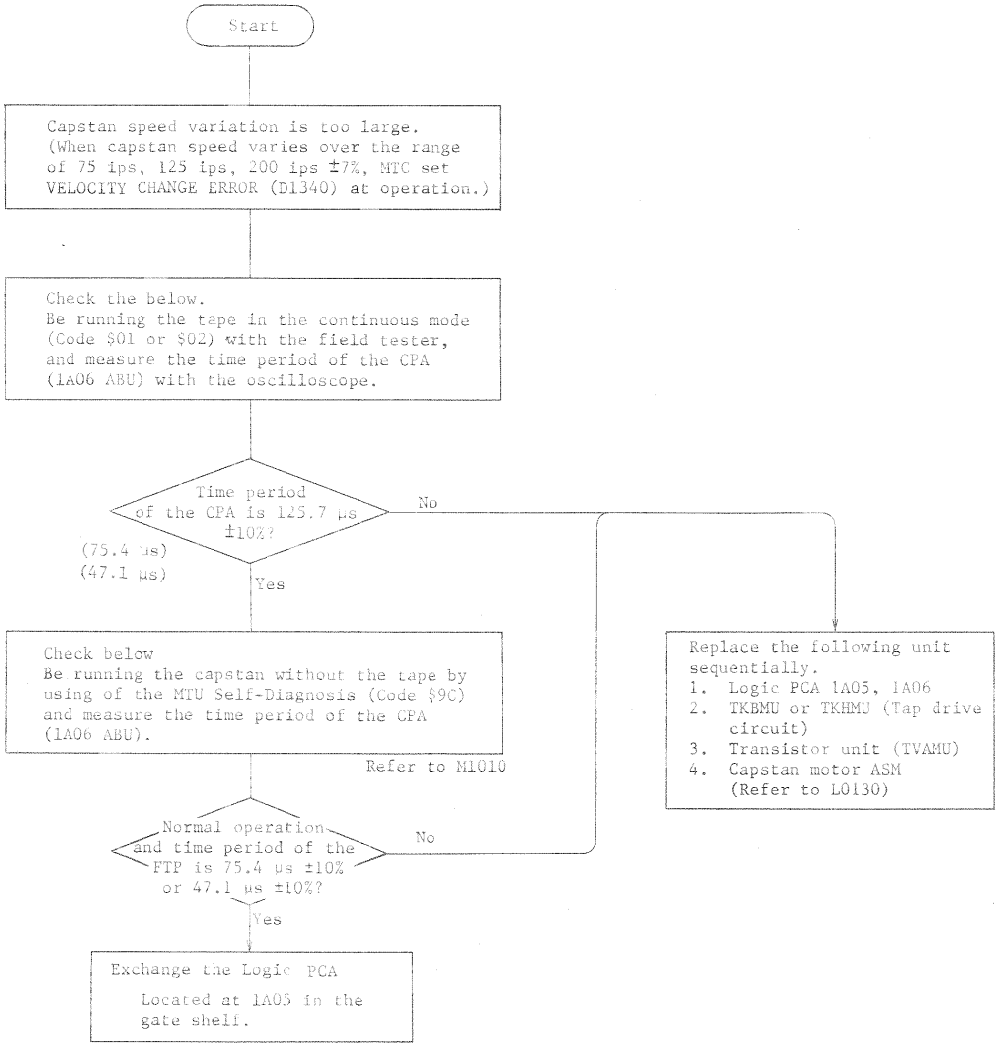


A0170	Tape Loop Vibration in Column is Considerable Size.

Symptom: A unit check results if tape loop in the column passes the warning detection hole with the servo set on.



A0180	The Tape does not Run in Standard Speed



A0300 Error Code = 42

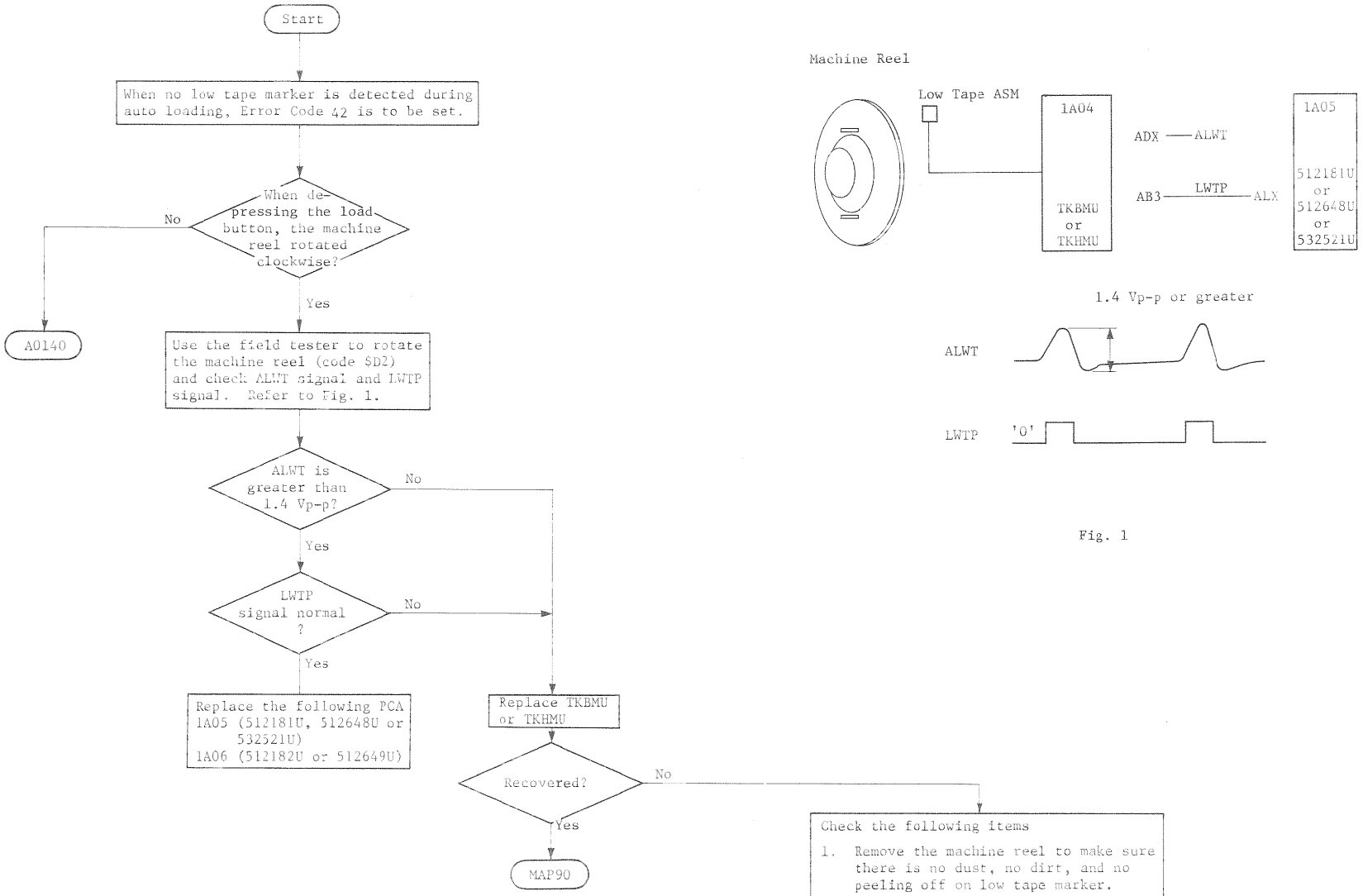
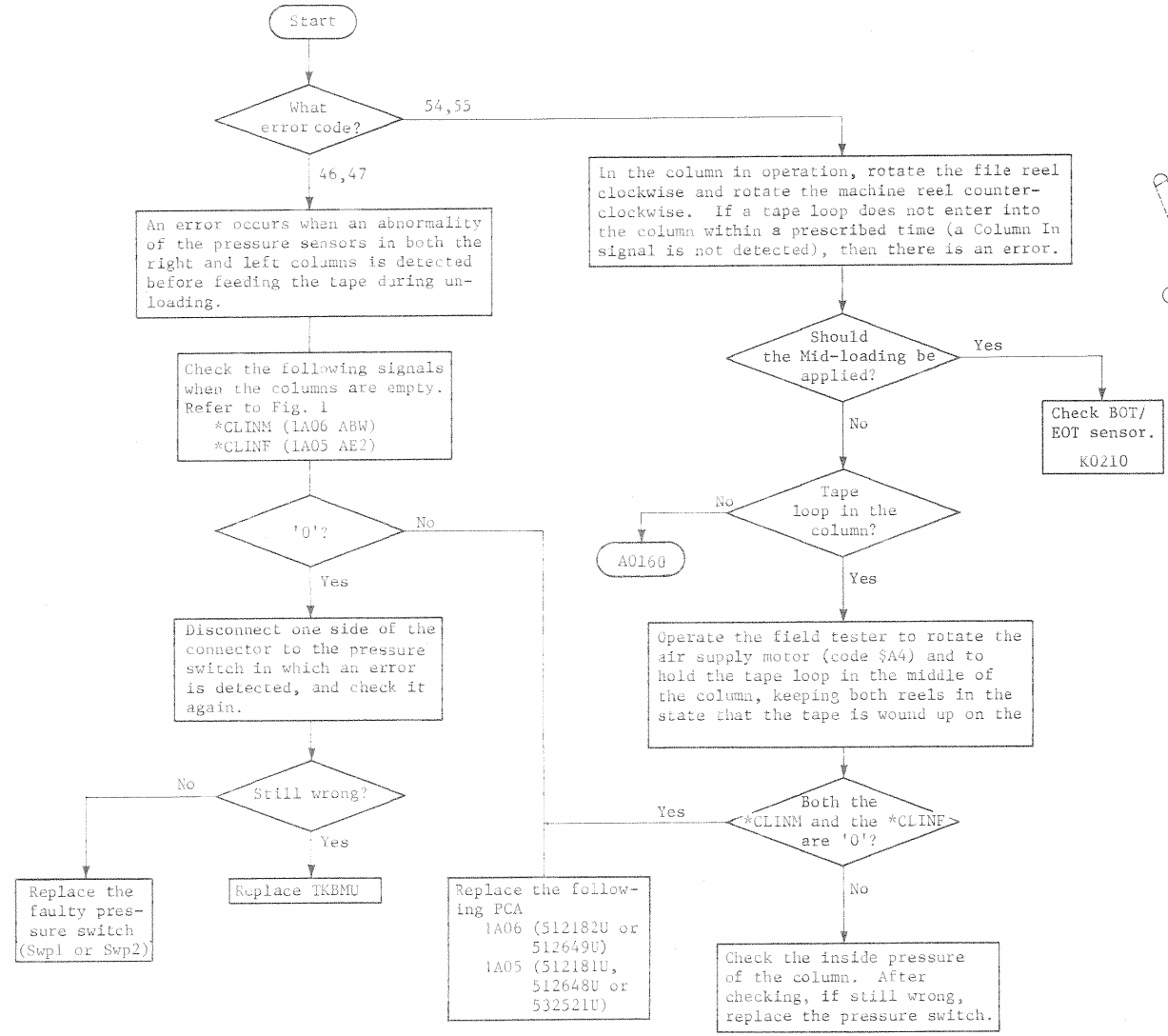


Fig. 1

A0310	Error Code = 46·47, 54·55



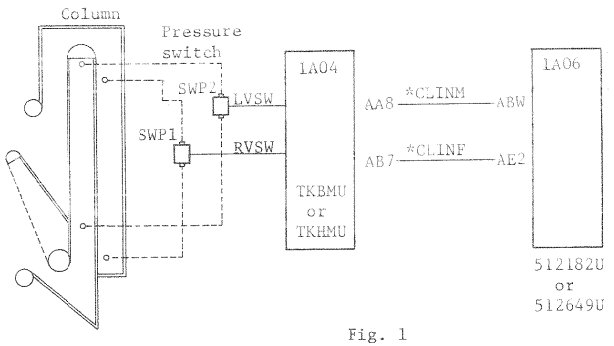


Fig. 1

A0320	Error Code = 43, 64

Start

Check if the auto hub is locked before the tape is fed during auto loading and when the MTU is in the Servo On status.

Make shortcircuit of both terminals of the hub lock detecting switch SWP3.

*HUBLK signal is '0' ?

No

Yes

Use the field tester to rotate the air supply motor and make sure the Auto Hub ASM is in the locked status.

Auto hub is locked ?

Yes

No

Check the following items and make adjustment.
1. Make sure there is no failure in the belt hooked on the motor and pump of air supply unit.
2. Check if the rear frame in the rear part of reel motor is mounted firmly. (There is no air leakage.)
3. Remove 6 mounting screws for the rear frame and check if there is any damage in the diaphram.
4. Check and adjust the blow-out air pressure. (K0190)

Replace pressure switch SWP3.

Connect 1A05 ALW to 0V terminal while keeping the state of checking bit 4 (*HUBLK) in file address $15 using the maintenance panel

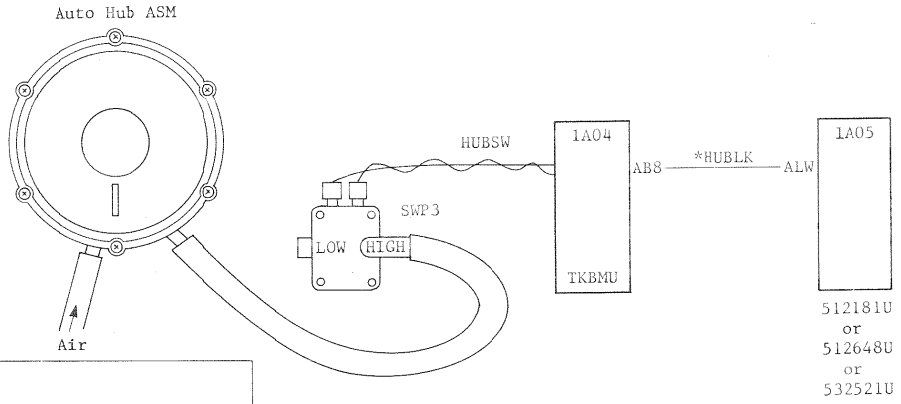
Bit 4 lamp is lighting?

Yes

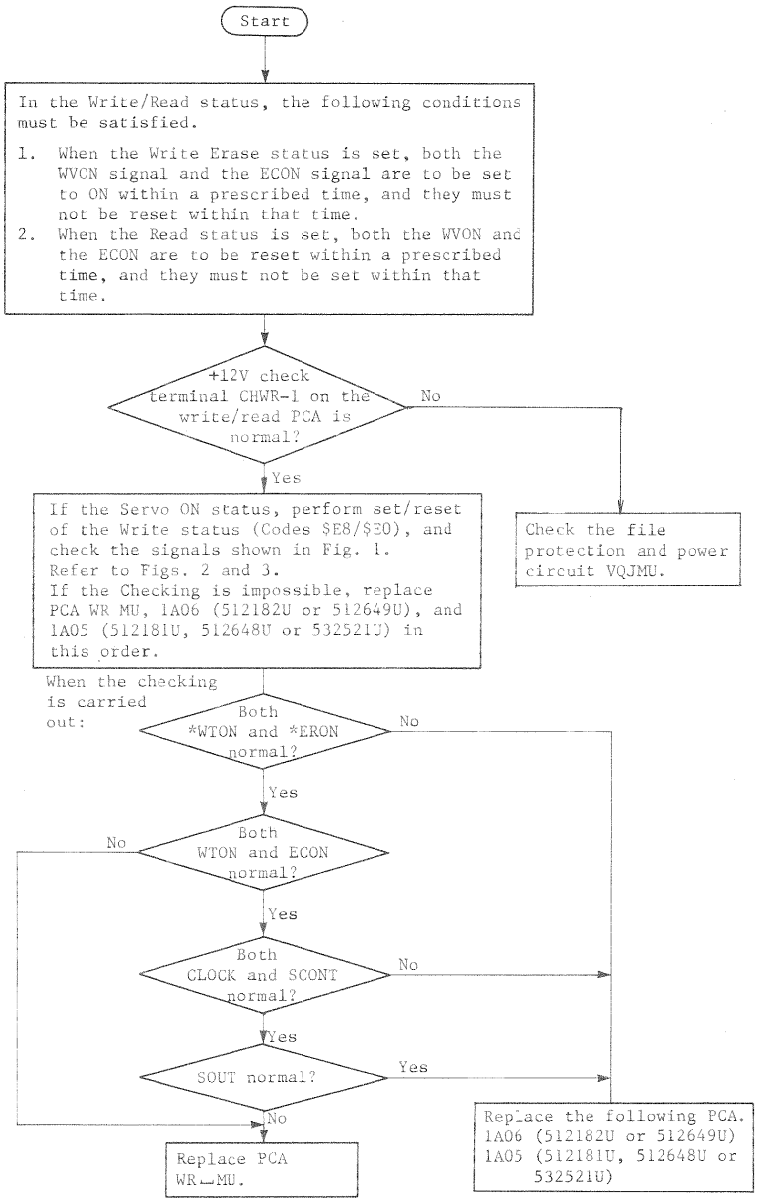
No

Replace TKBMU or TKHMU.

Replace the following PCA
1A05 (512181U, 512648U or 532521U)
1A06 (512182U or 512649U)



A0330	Abnormality Regarding Write/Read Status



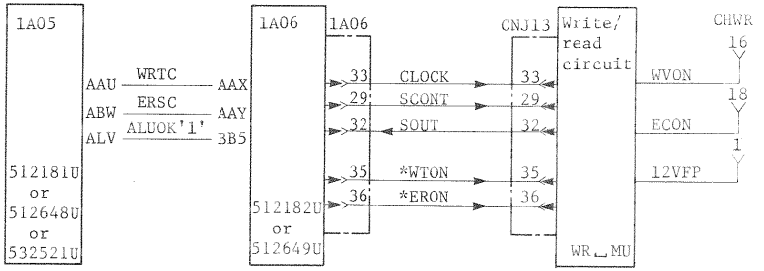


Fig. 1

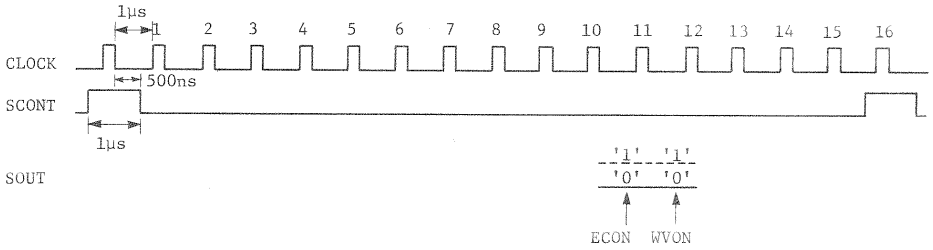


Fig. 2

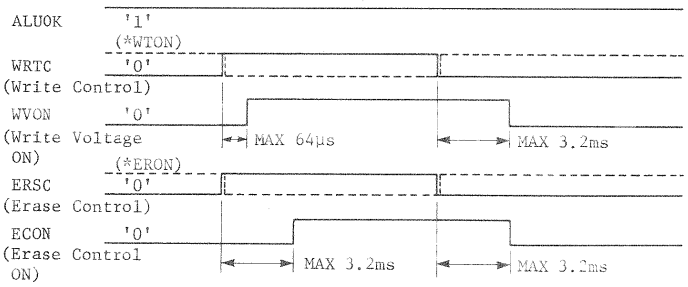
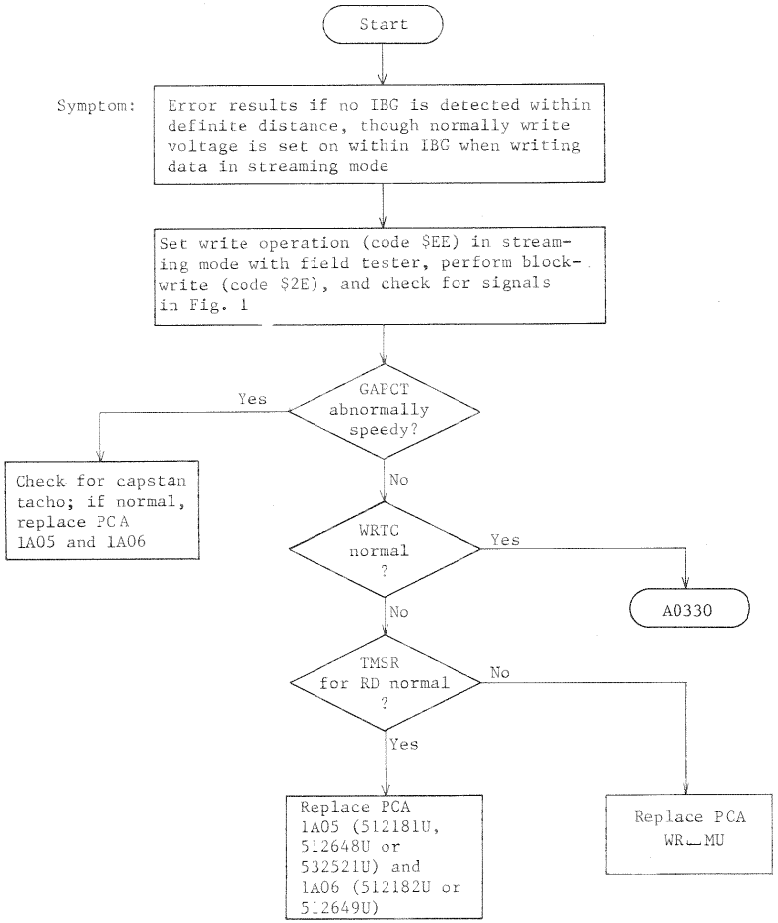


Fig. 3

A0340	Error Code = 85



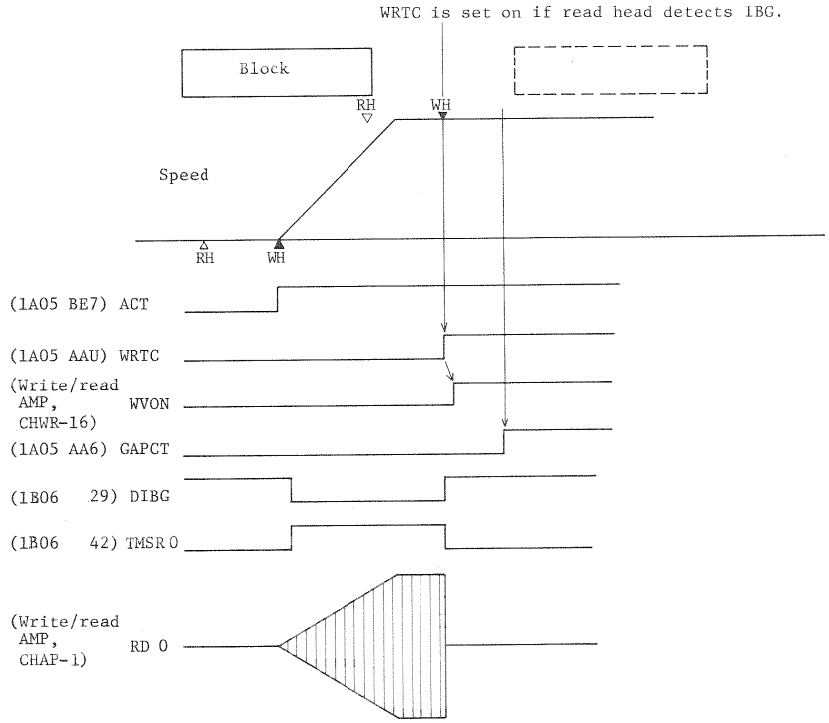


Fig. 1

A0350	Error Code = 49

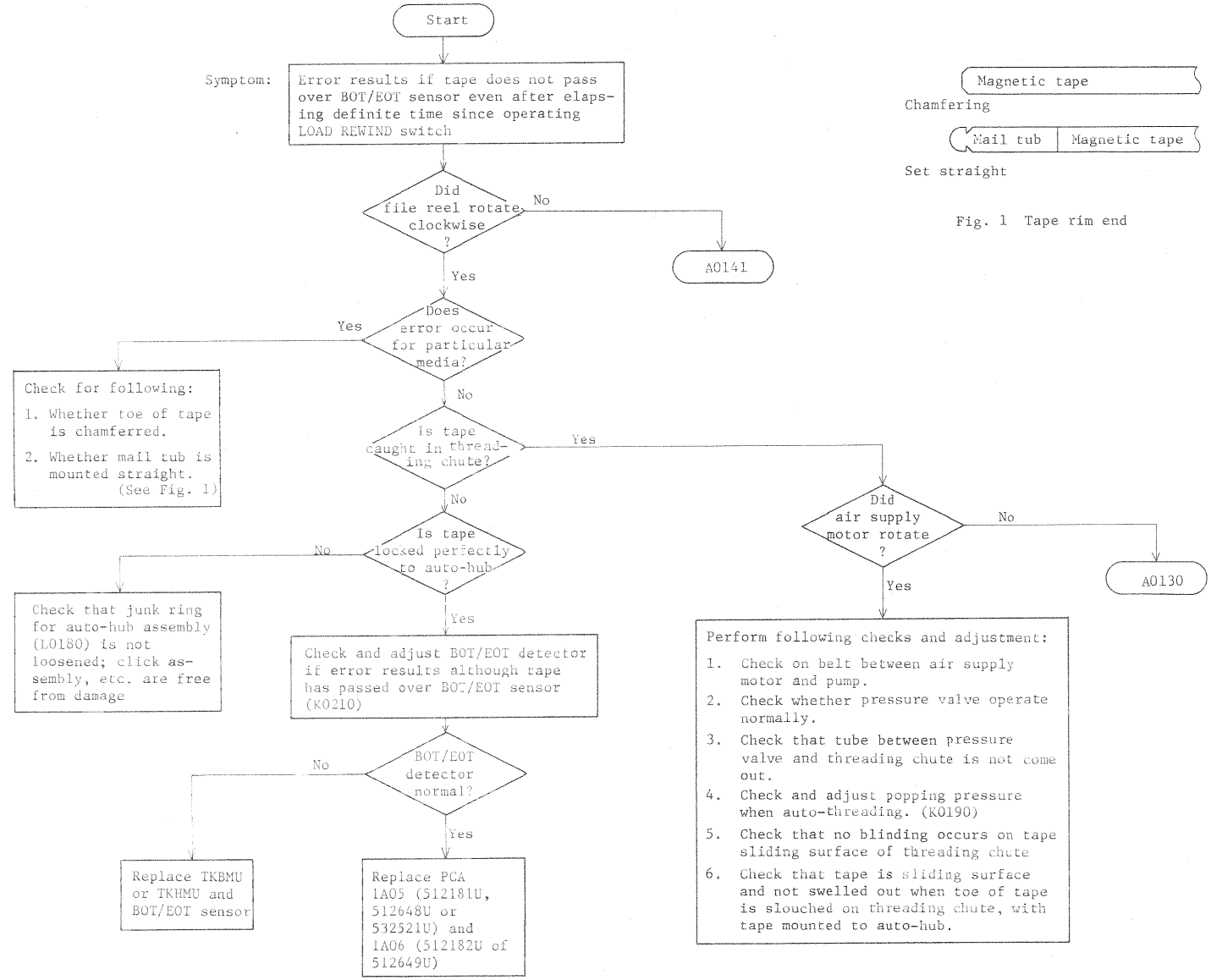
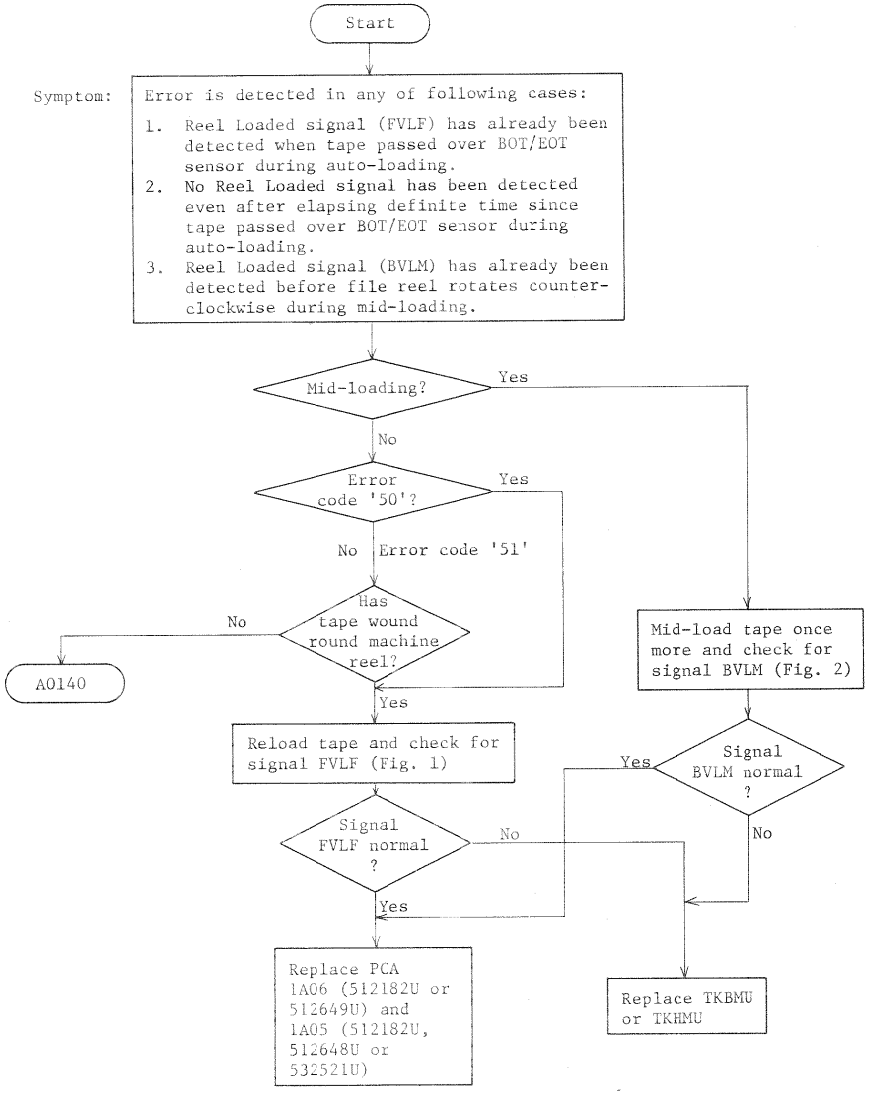


Fig. 1 Tape rim end

A0360	Error Code = 50, 51



FVLF: Forward Voltage Limit File

BVLM: Backward Voltage Linit Machine

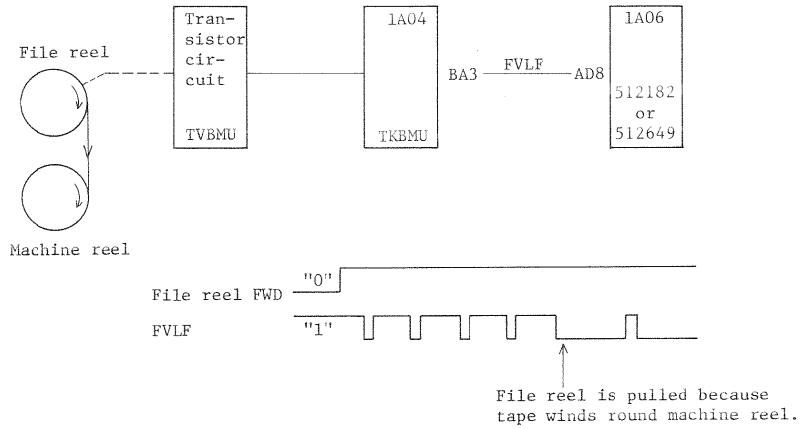


Fig. 1 Reel Loaded check when auto-loading

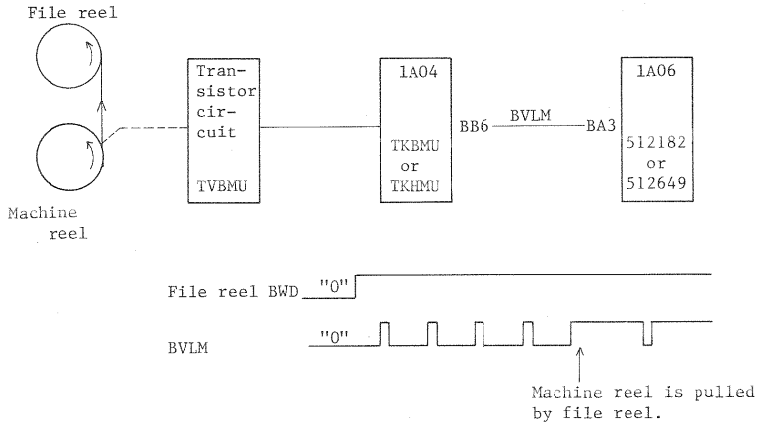
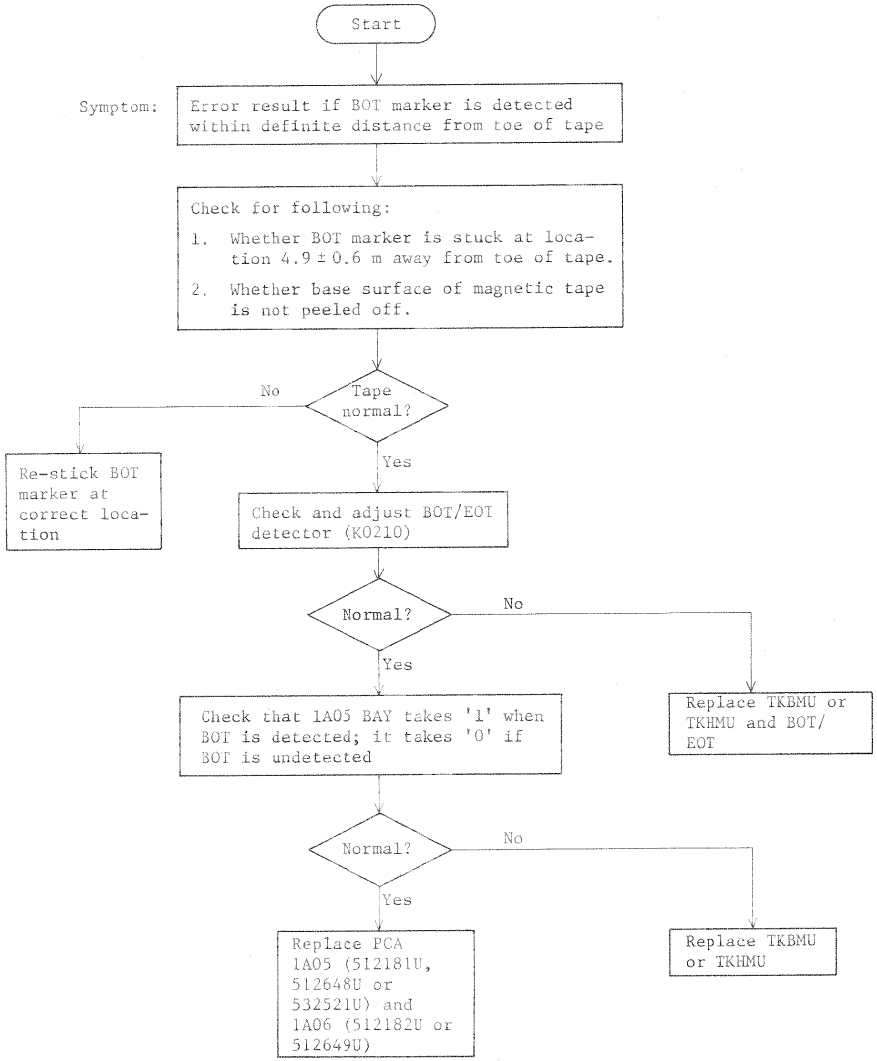
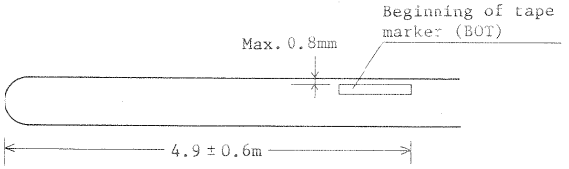


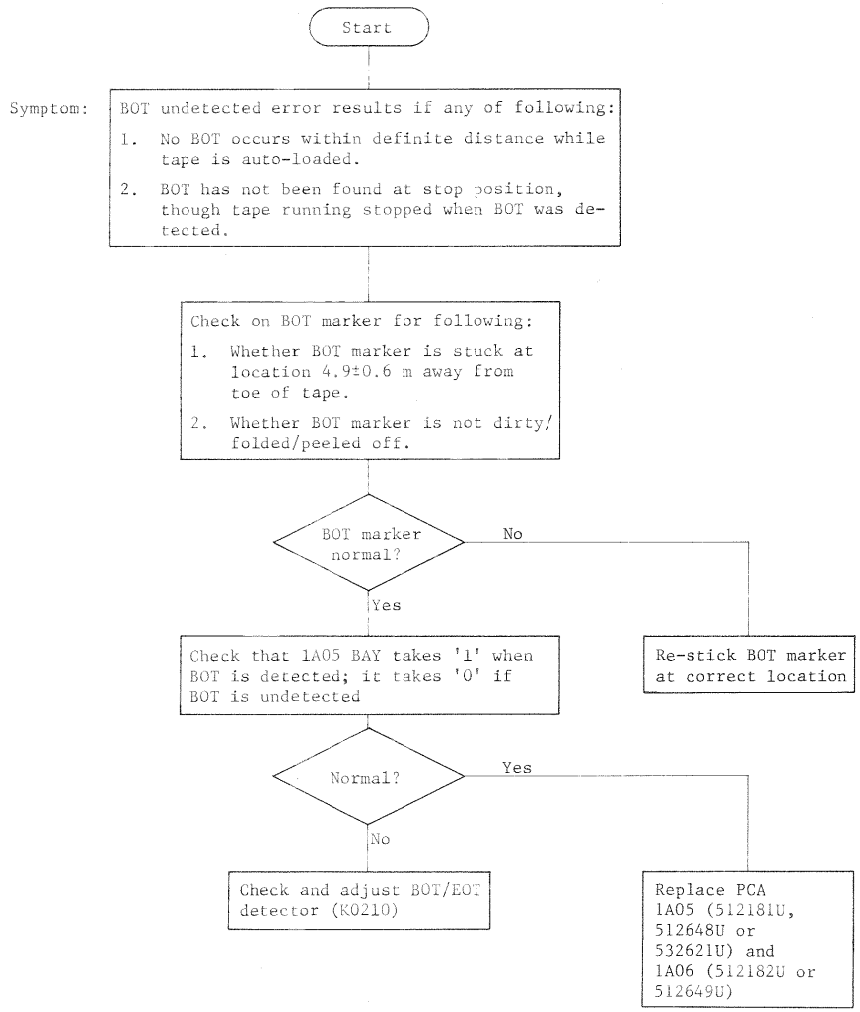
Fig. 2 Reel Loaded check when mid-loading

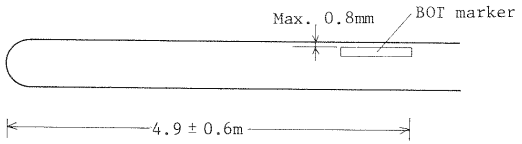
A0380	Error Code = 52



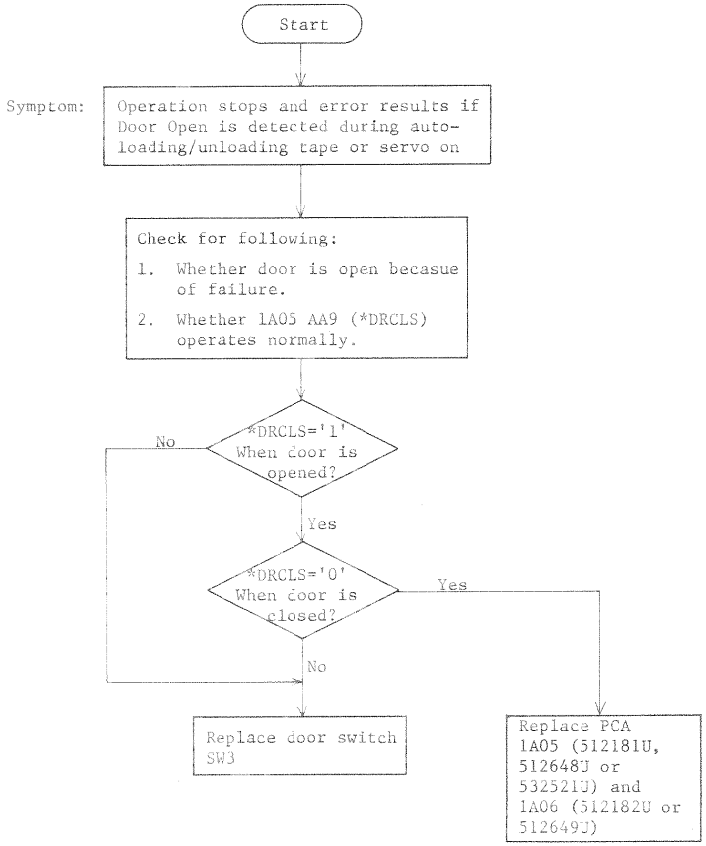


A0400	BOT Marker is not Detected





A0420	Error Code = 35, 40, 65



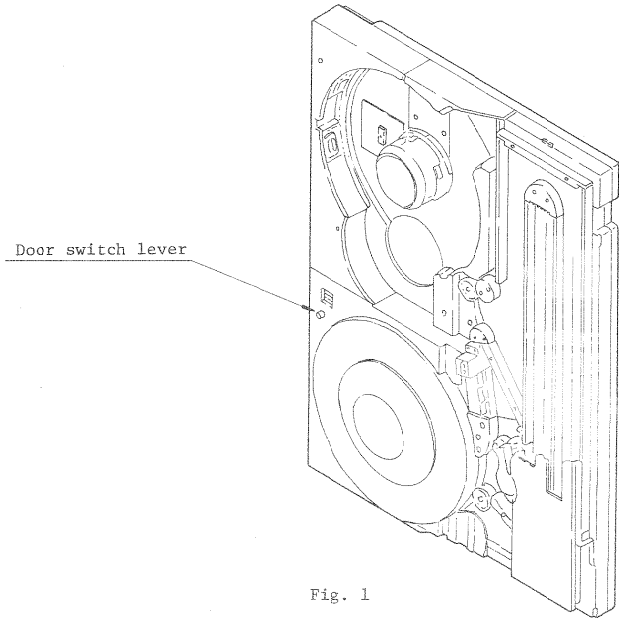


Fig. 1

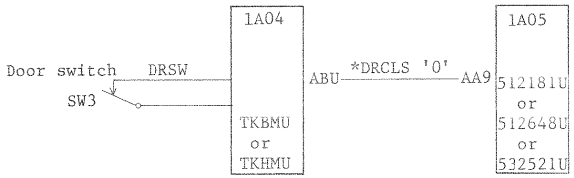
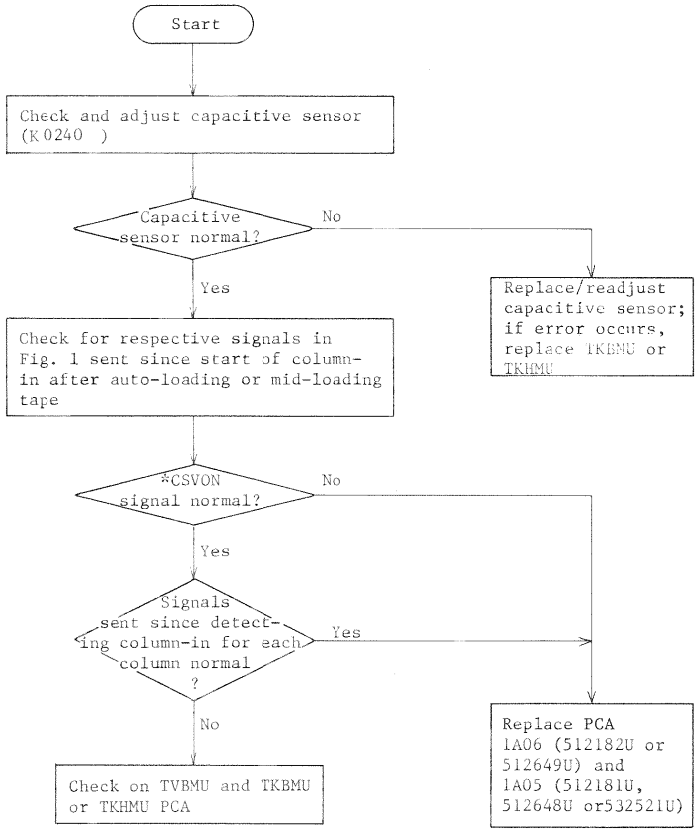


Fig. 2

A0430	Error Code = 56, 57

Symptom: Error results if tape loop pass warning detection hole after column-in has been detected once during column-in action.



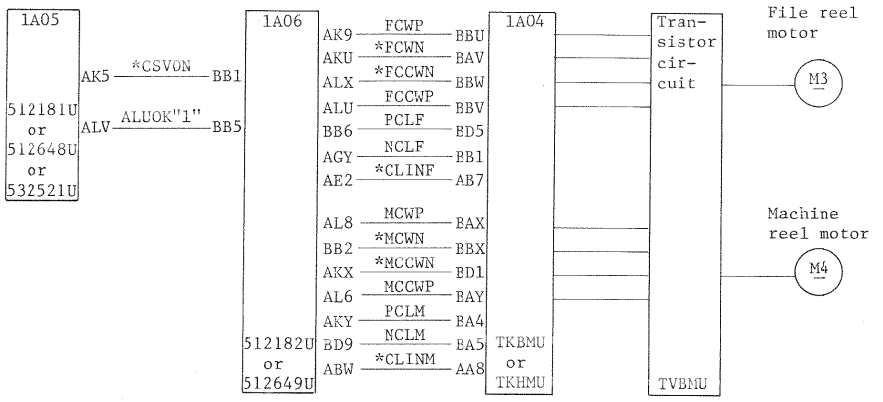


Fig. 1

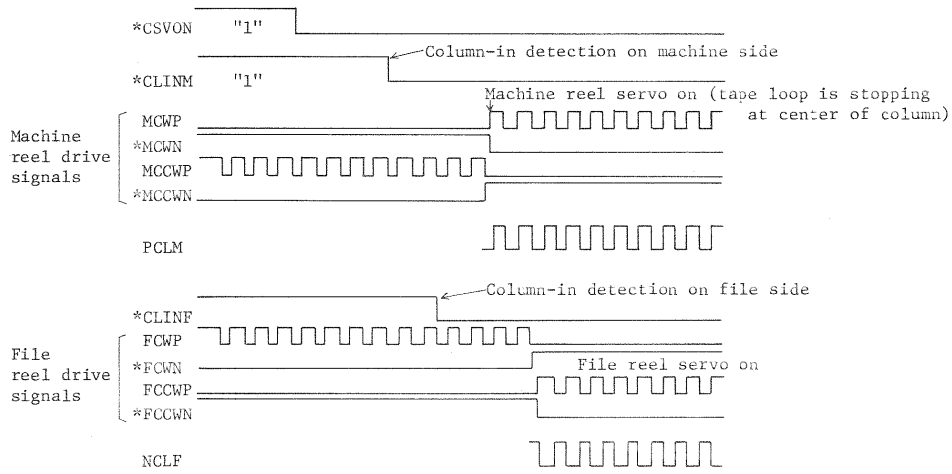
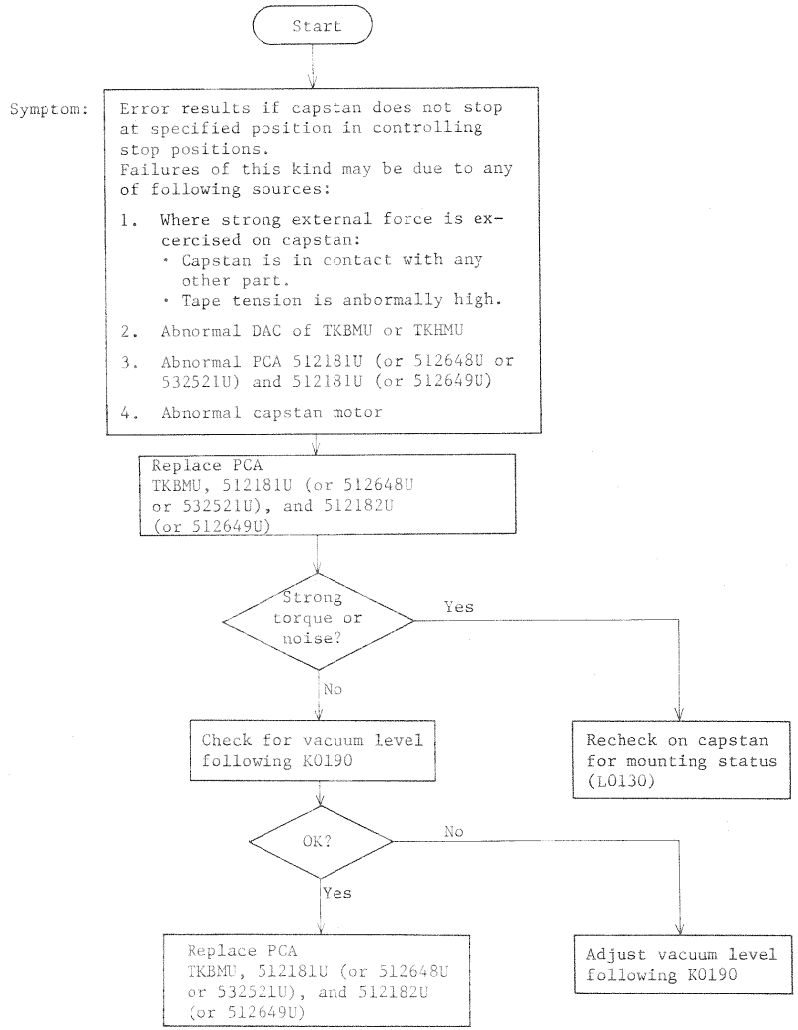
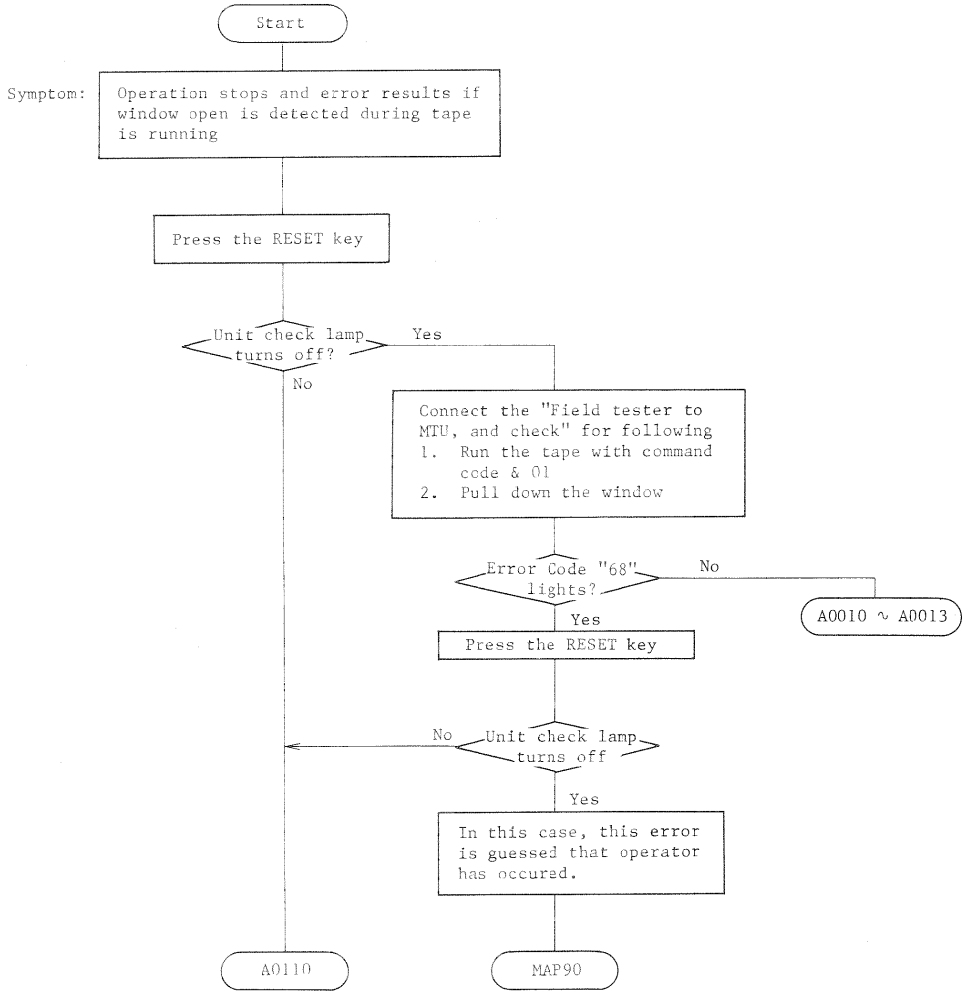


Fig. 2

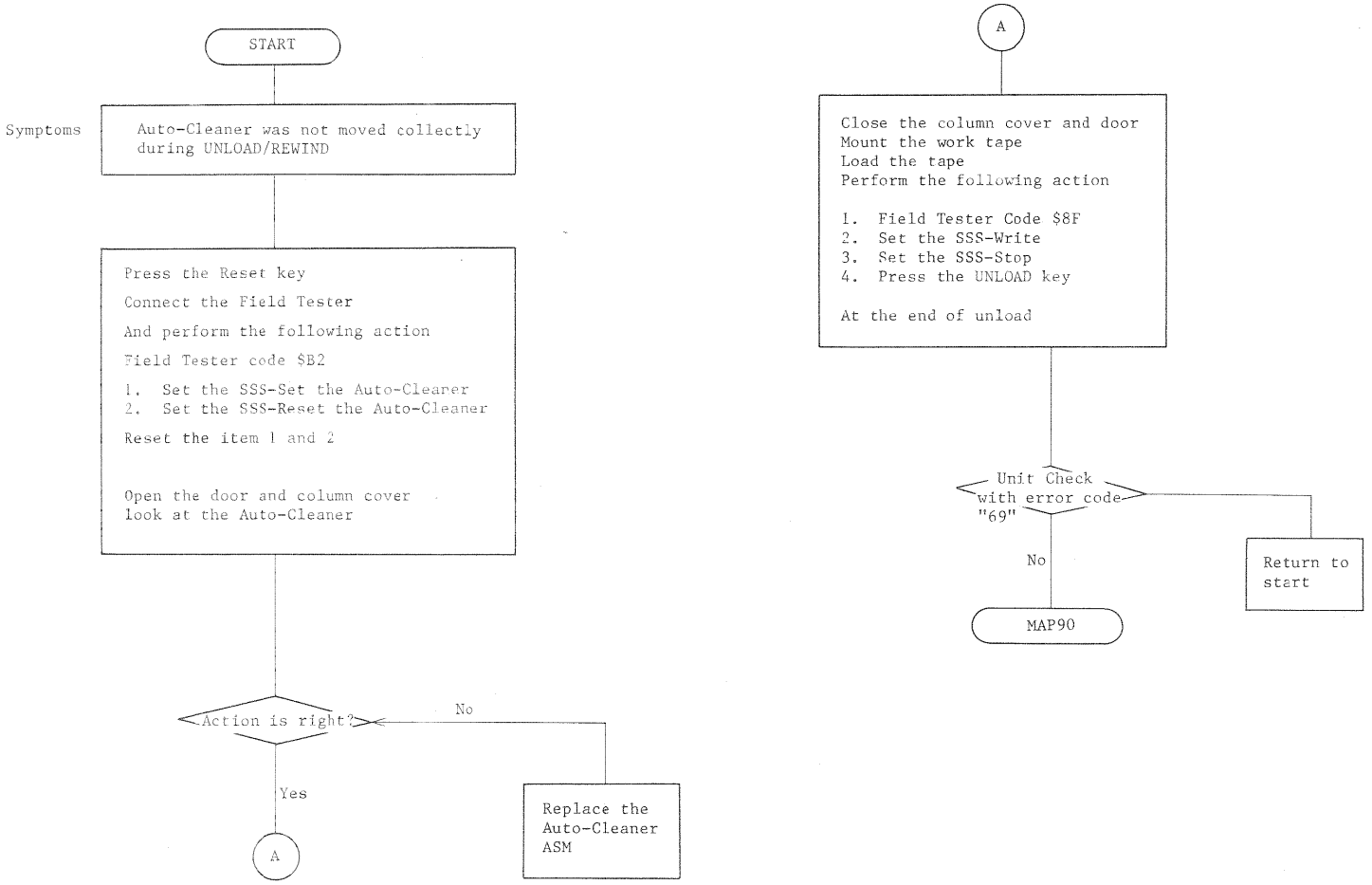
A0450	Error Code = 74, 75



A0460	Error Code = 68



A0470	Error Code = 69



A0500	Error Code = 72, 73

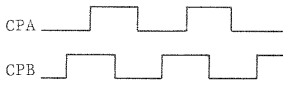
Start

Symptom: Error results if Opposite Direction (OD) signal to detect rotational direction of capstan motor during position control is abnormal:

1. OD does not become '1' even if capstan motor is rotated in reverse direction of internal status.
2. OD remains '0' even if capstan motor is rotated in same direction as internal status.

Manually rotate capstan motor with servo set off and check for capstan tacho (CPA and CPB)

While capstan is rotating forward

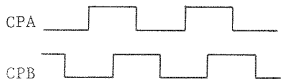


CPA and CPB normal?

No

Check on CTPA and CTPB; if abnormal, replace capstan motor; if normal, replace 1A06 (512182U or 512649U)

While capstan is rotating backward



Yes

With servo set on, set streaming (code $E6) and reset streaming (code $E2) for each of forward status and backward status with field tester and check for signals in Fig. 1.

DAC normal?

No

Replace PCA in following order:
TKBMU
1A05 (512181U, 512648U or 532521U)
1A06 (512648U or 512649U)

Yes

CPA and CPB output?

No

Replace PCA
TVAMU and TKBMU or TKHMU

Yes

Replace PCA
1A05 (512181U, 512648U or 532521U) and
1A06 (512182U or 512649U)

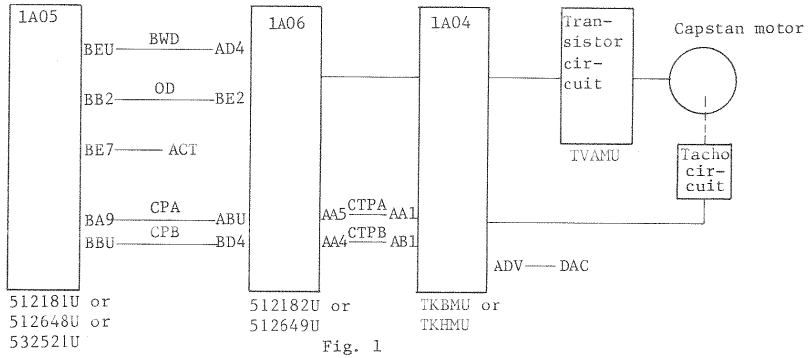


Fig. 1

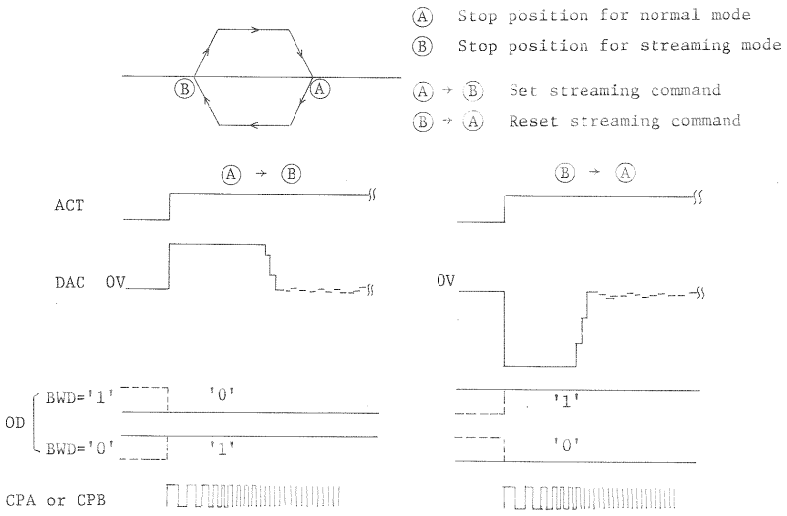
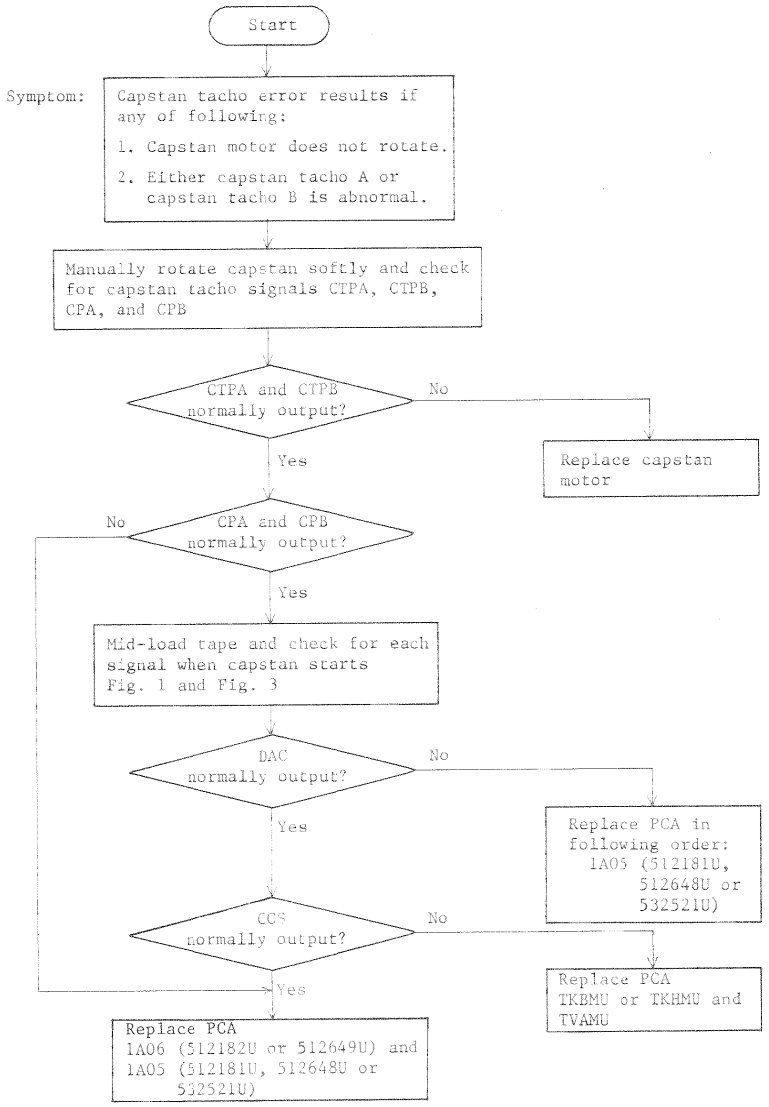


Fig. 2

A0550	Capstan Tacho Error



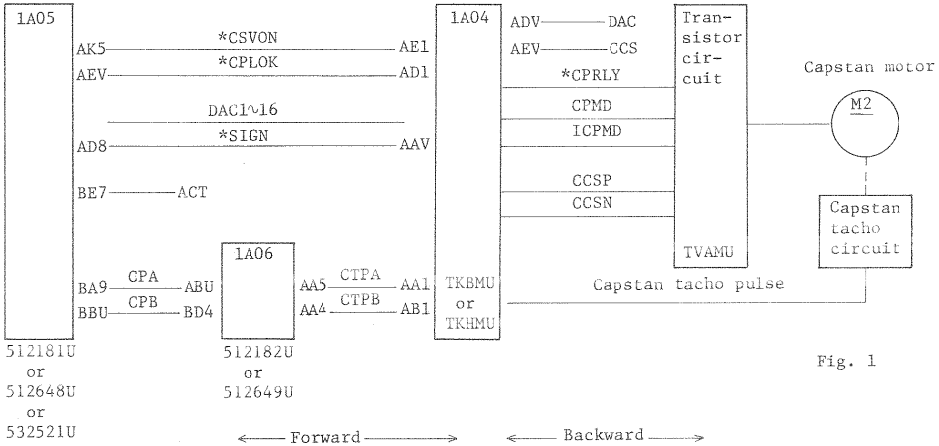


Fig. 1

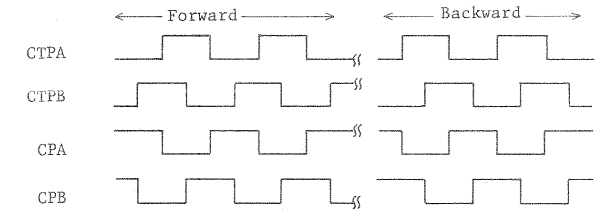


Fig. 2

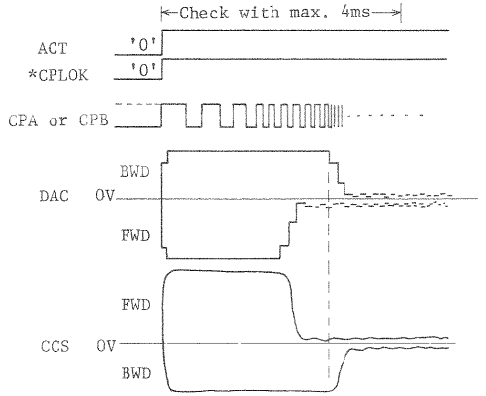
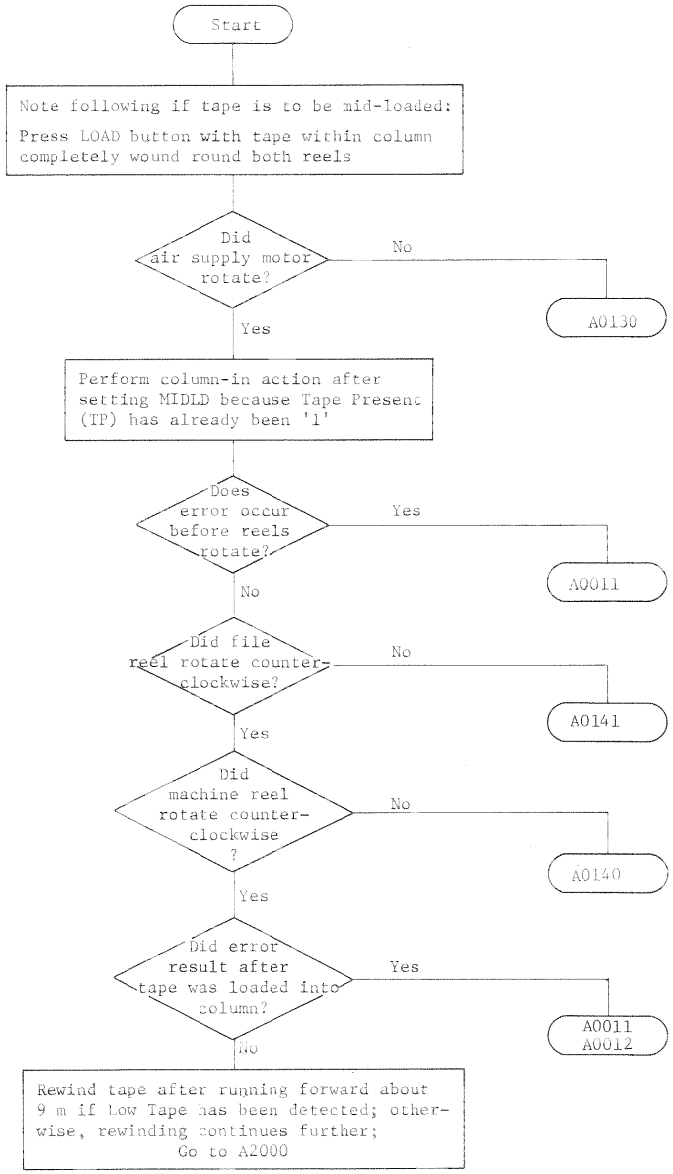
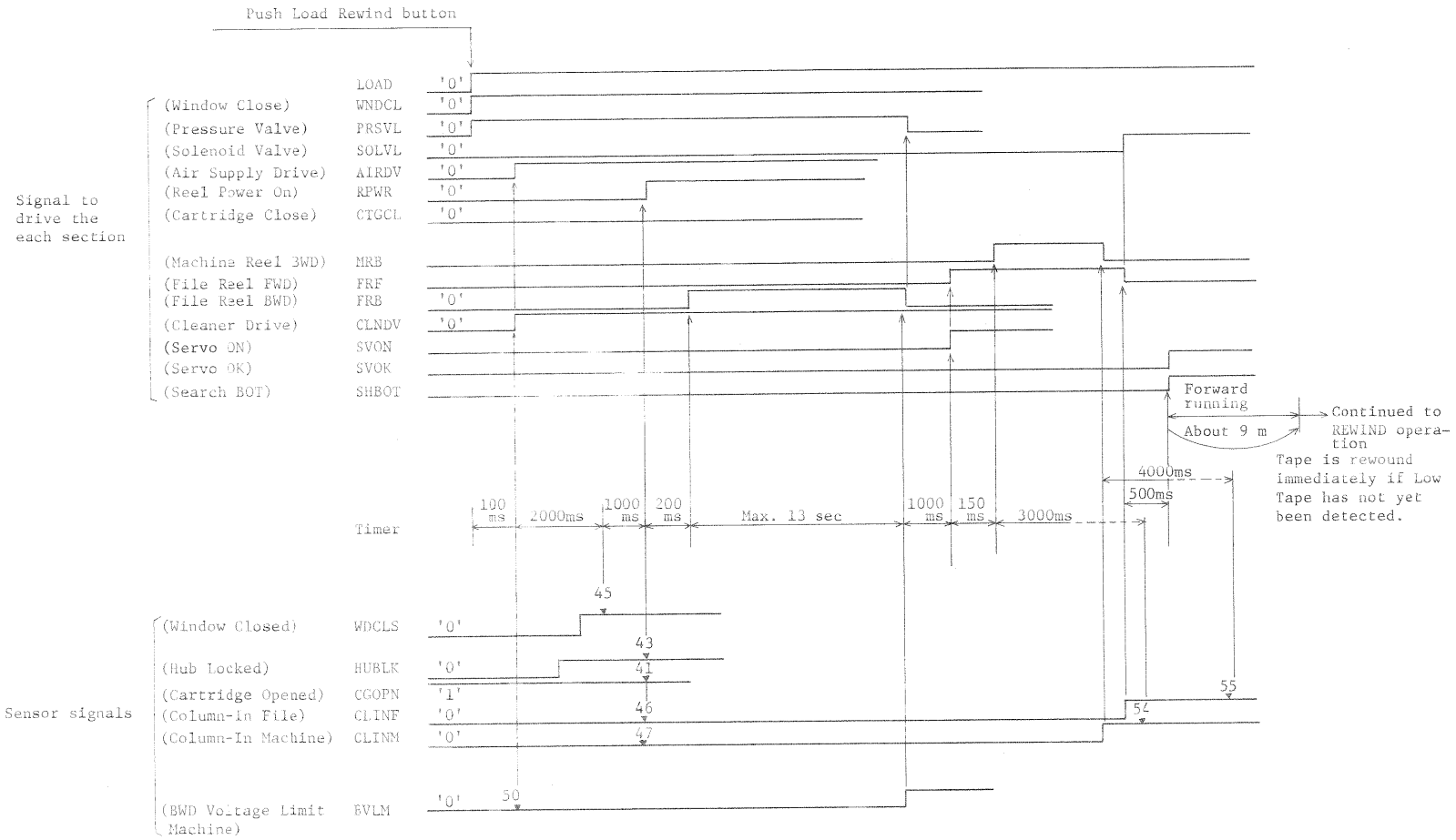


Fig. 3

A1000	Mid-Loading Trouble

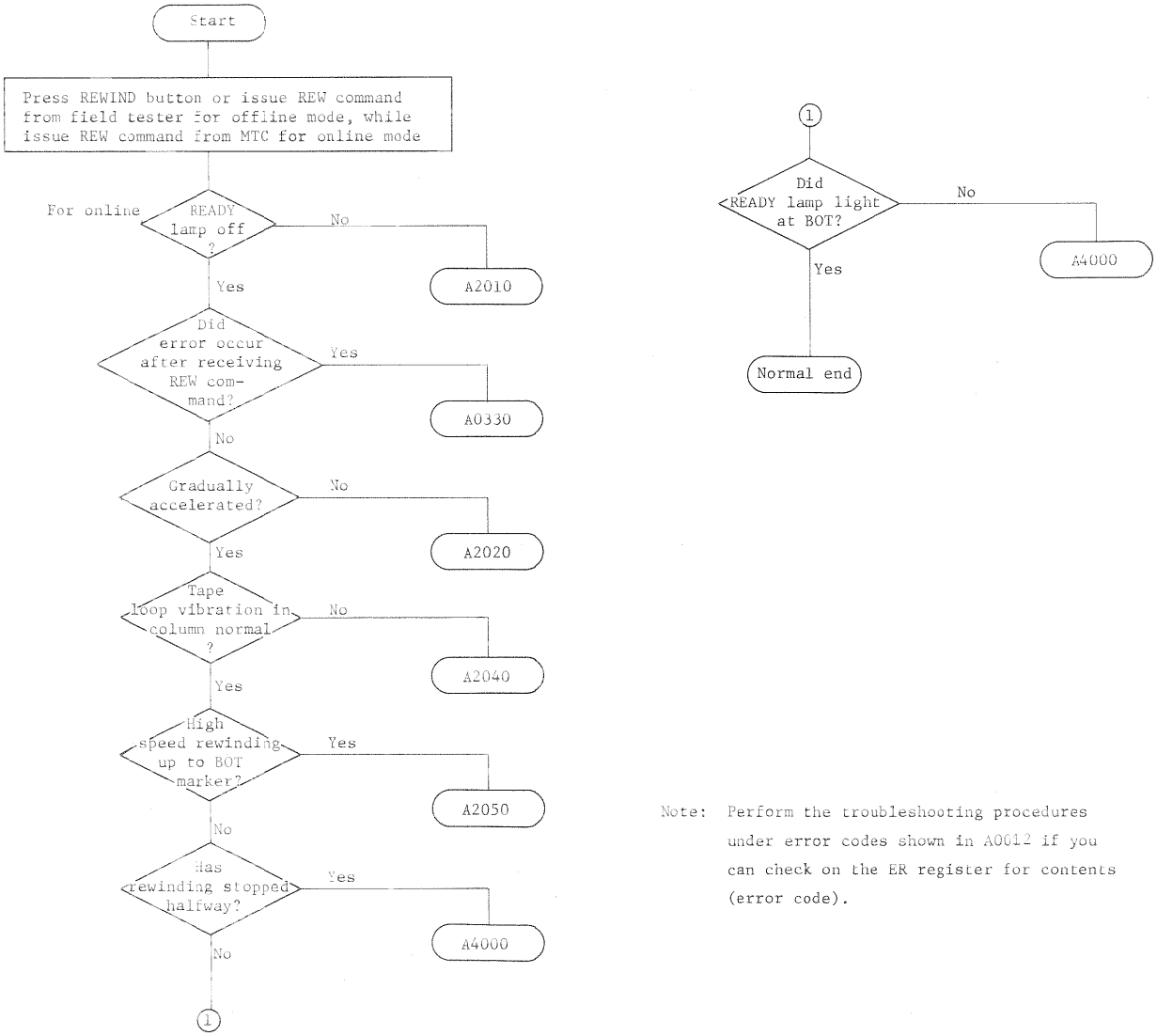


A1001	Mid-Load Timing Chart



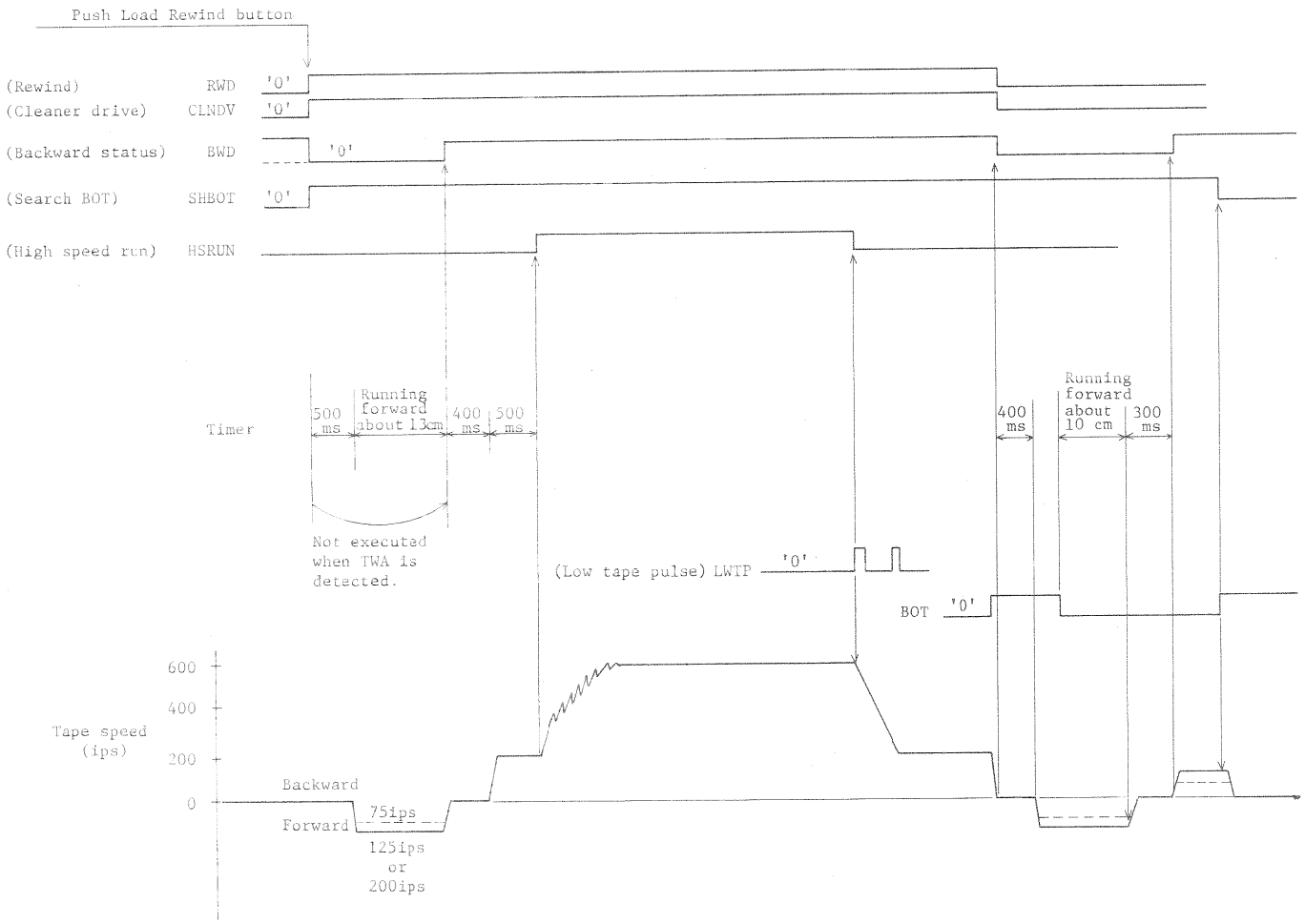
Note: The marks "▼" indicate the timings when the program checks the logical level of sensors during mid-loading. The hexadecimal number in upper of the mark "▼" means Error code which is set to ER register.

A2000	Rewind Trouble

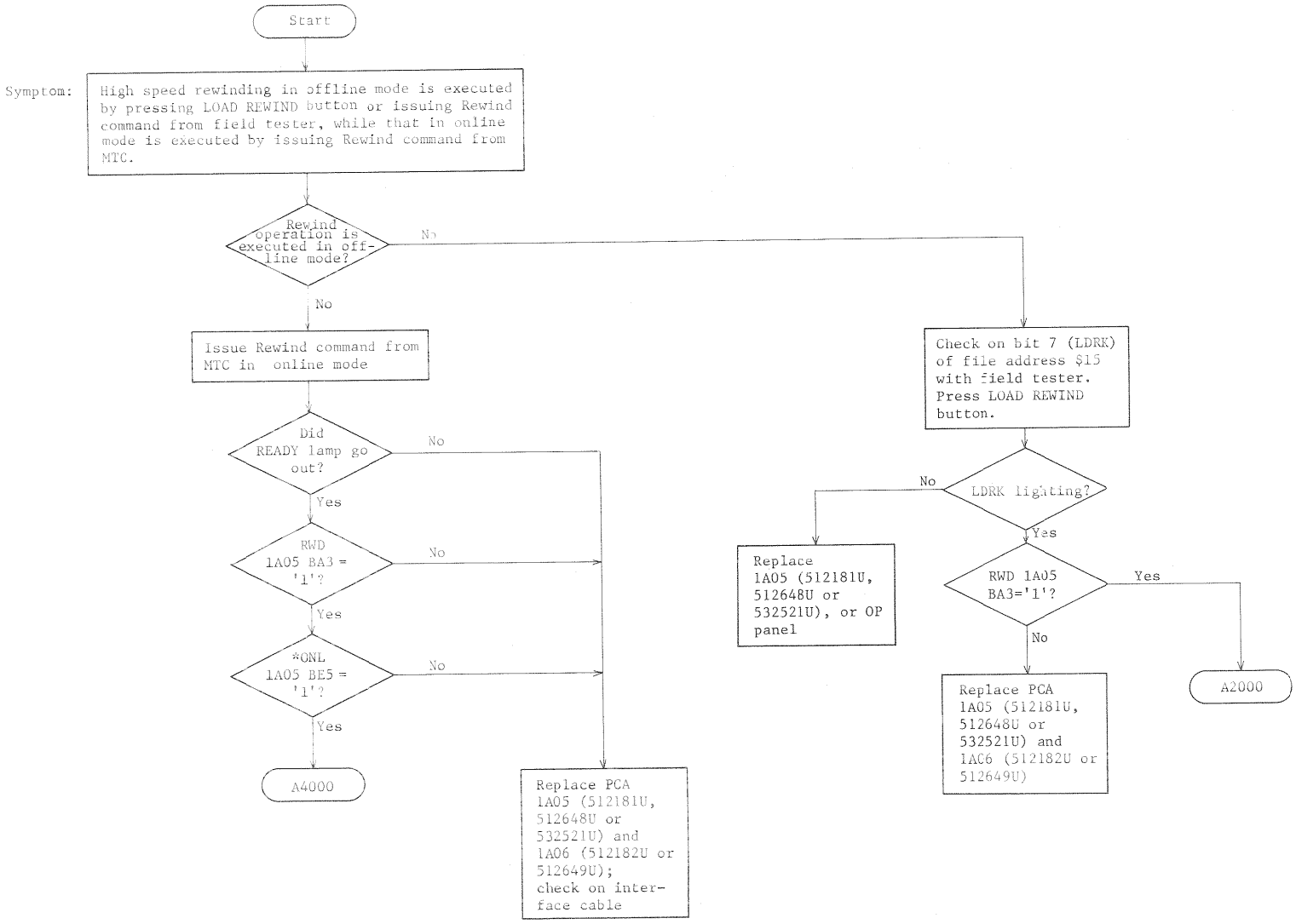


Note: Perform the troubleshooting procedures under error codes shown in A0012 if you can check on the ER register for contents (error code).

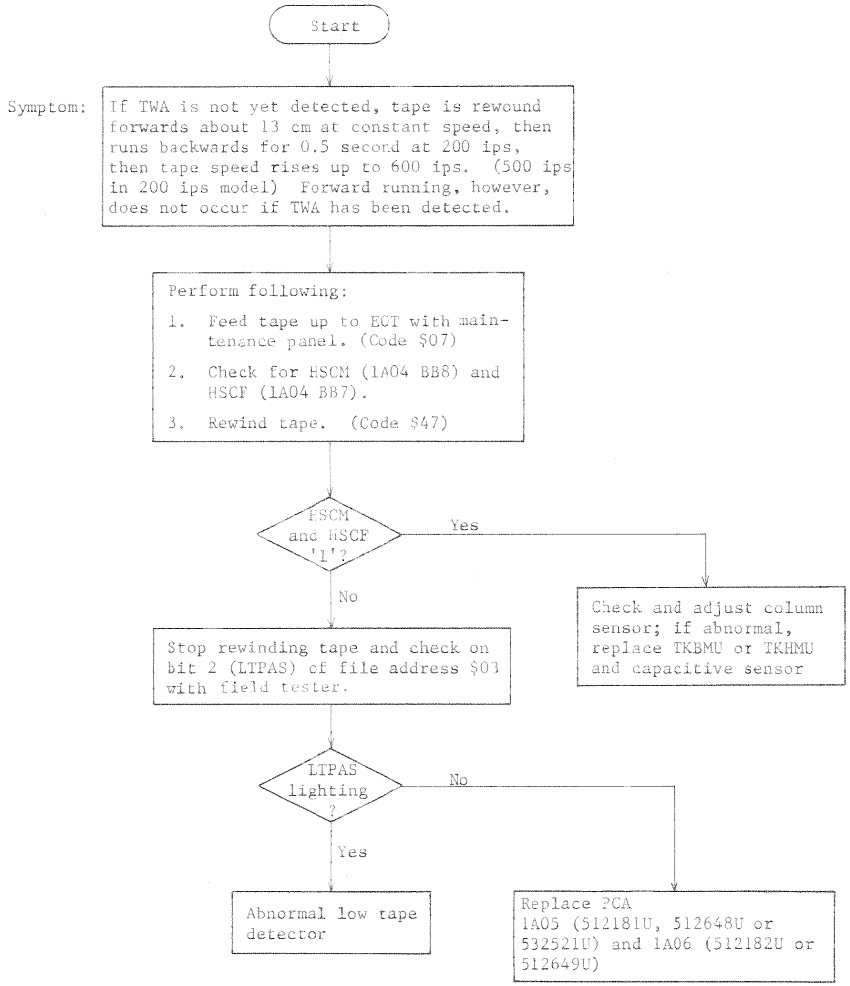
A2001	Rewind Timing Chart



A2010	No Rewind Operation is Performed



A2020	Capstan Rotation does not Gradually Acceleratd.



A2040	Tape Loop Trouble in Columns (200 ips to 600 ips, 600 ips to 200 ips)

Start

Symptom: After tape is rewound for 0.5 second at 200 ips, tape speed accelerates gradually by 40 ips per 100 ms if Speed Down signal (HSCM/HSCF) from reel controller does not become '1', while it decelerates gradually by 40 ips per 100 ms if Speed Down signal becomes '1'.
If low tape marker is detected, then tape speed decelerates gradually at intervals of 100 ms.

Check for HSCM (1A04 BA8) and HSCF (1A04 BB7) by taking following steps with tape stopped:

1. Lower file column loop slowly and stop it near alarm detection hole to check for HSCF signal.
2. Wind up machine column loop slowly and stop it near alarm detection hole to check for HSCM signal.

For HSCF signal: '0' if loop is at center of column; '1' if loop is near alarm detection hole?

No → Check and adjust column sensor; if abnormal, replace capacitive sensor

Yes

For HSCM signal: '0' if loop is at center of column; '1' if loop is near alarm detection hole?

No → Check and adjust column sensor; if abnormal, replace capacitive sensor

Yes → Wind up tape and check for capstan tacho with maintenance panel (code $9D)

Unit check?

No → Replace PCA 1A05 (512181U, 512648U or 532521U) and 1A06 (512182U or 512649U)

Yes → Replace capstan motor because capstan tacho is abnormal

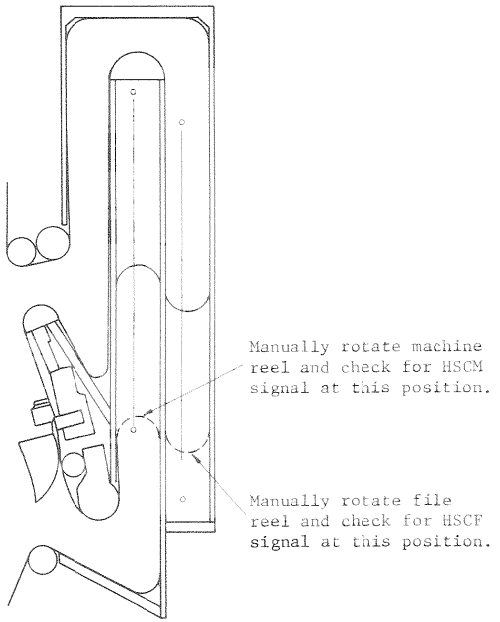
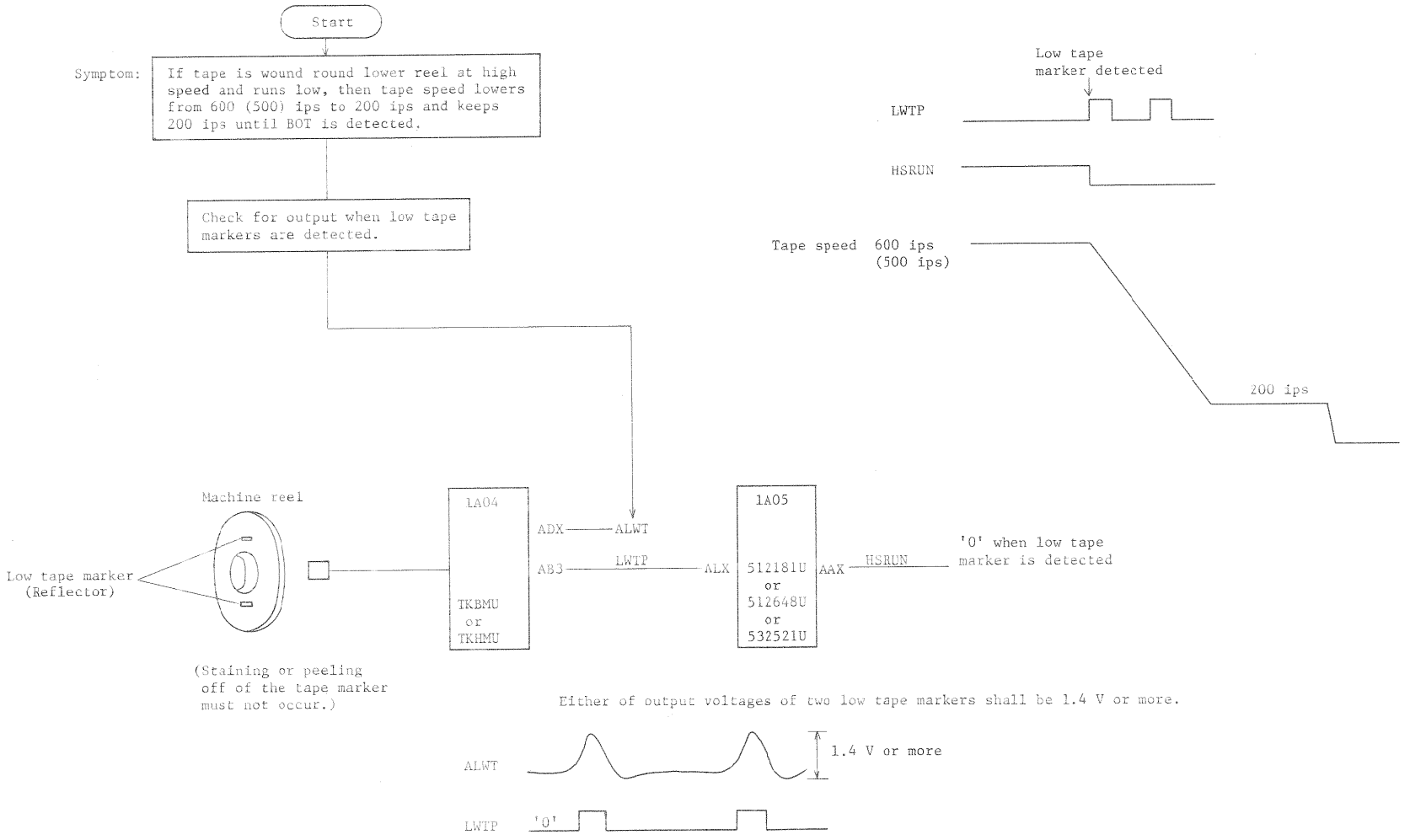
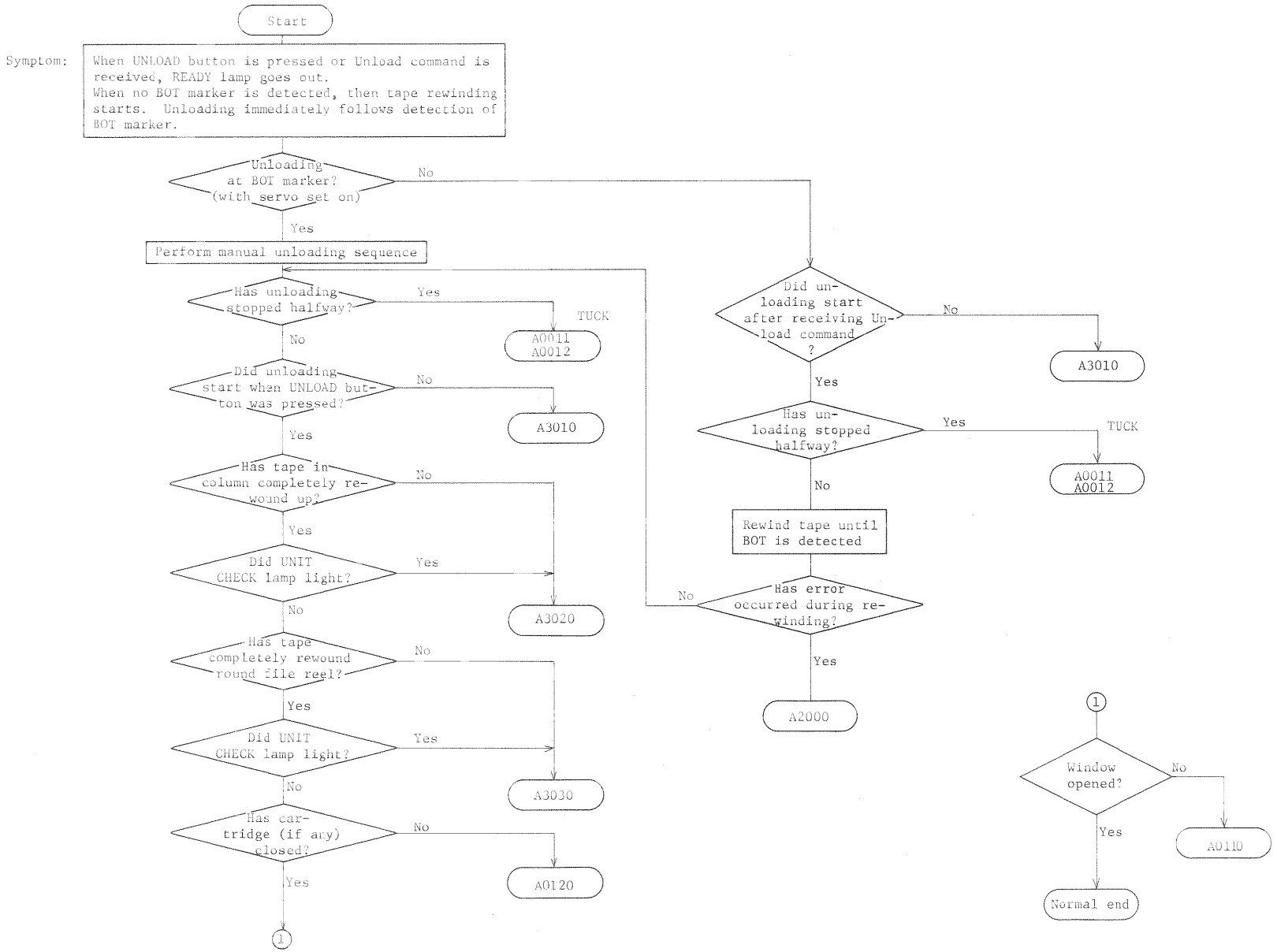


Fig. 1

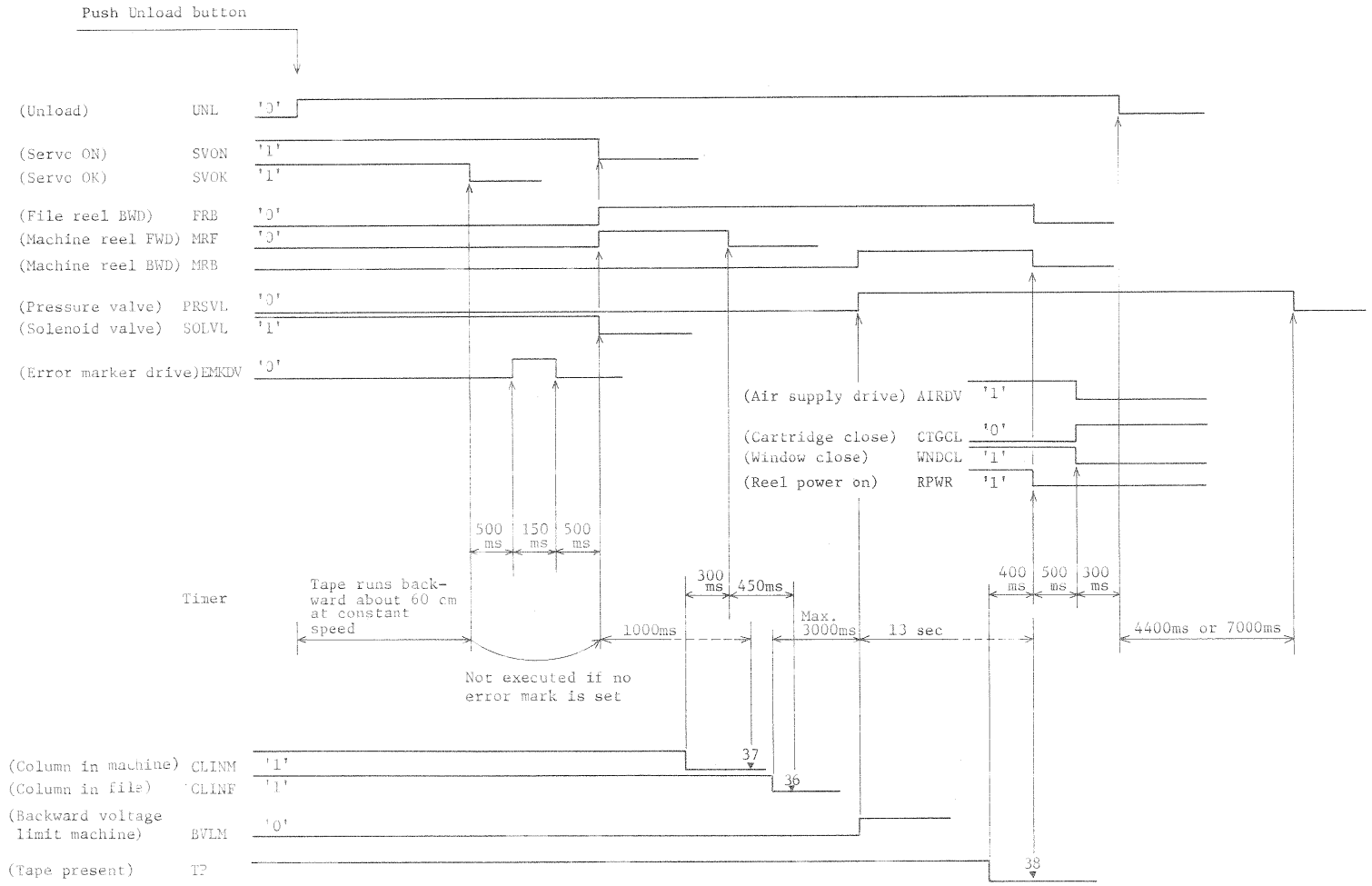
A2050	Tape is Rewound at High Speed Until the BOT.



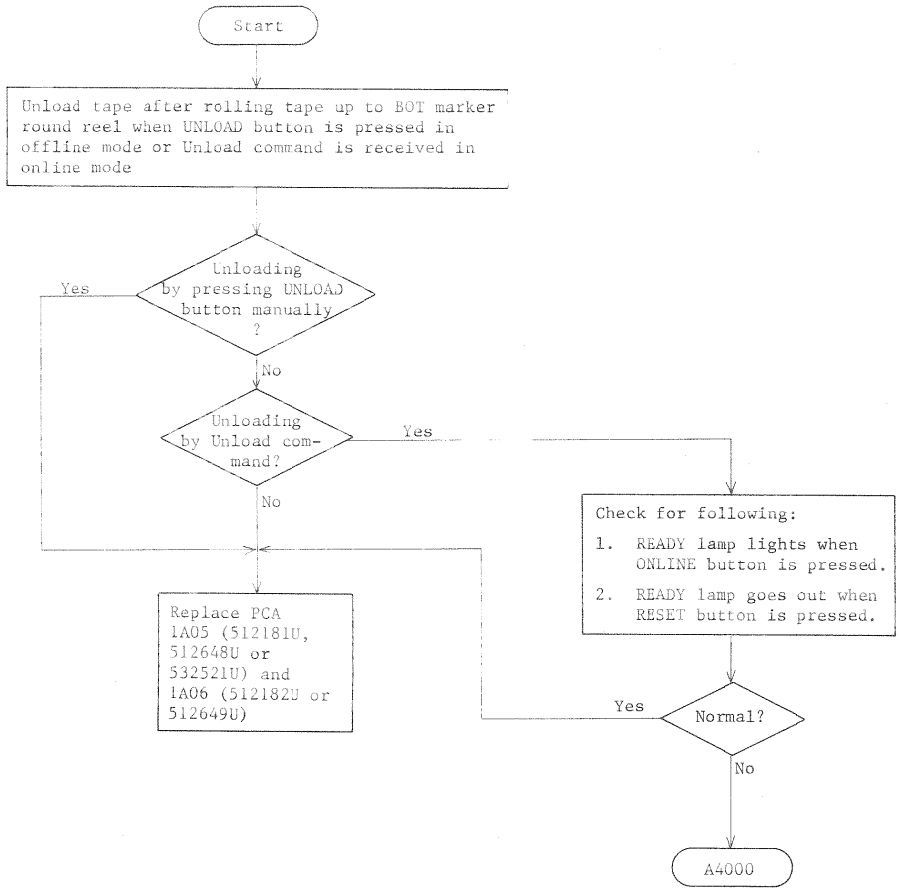
A3000	Troubles during Unloading Sequence



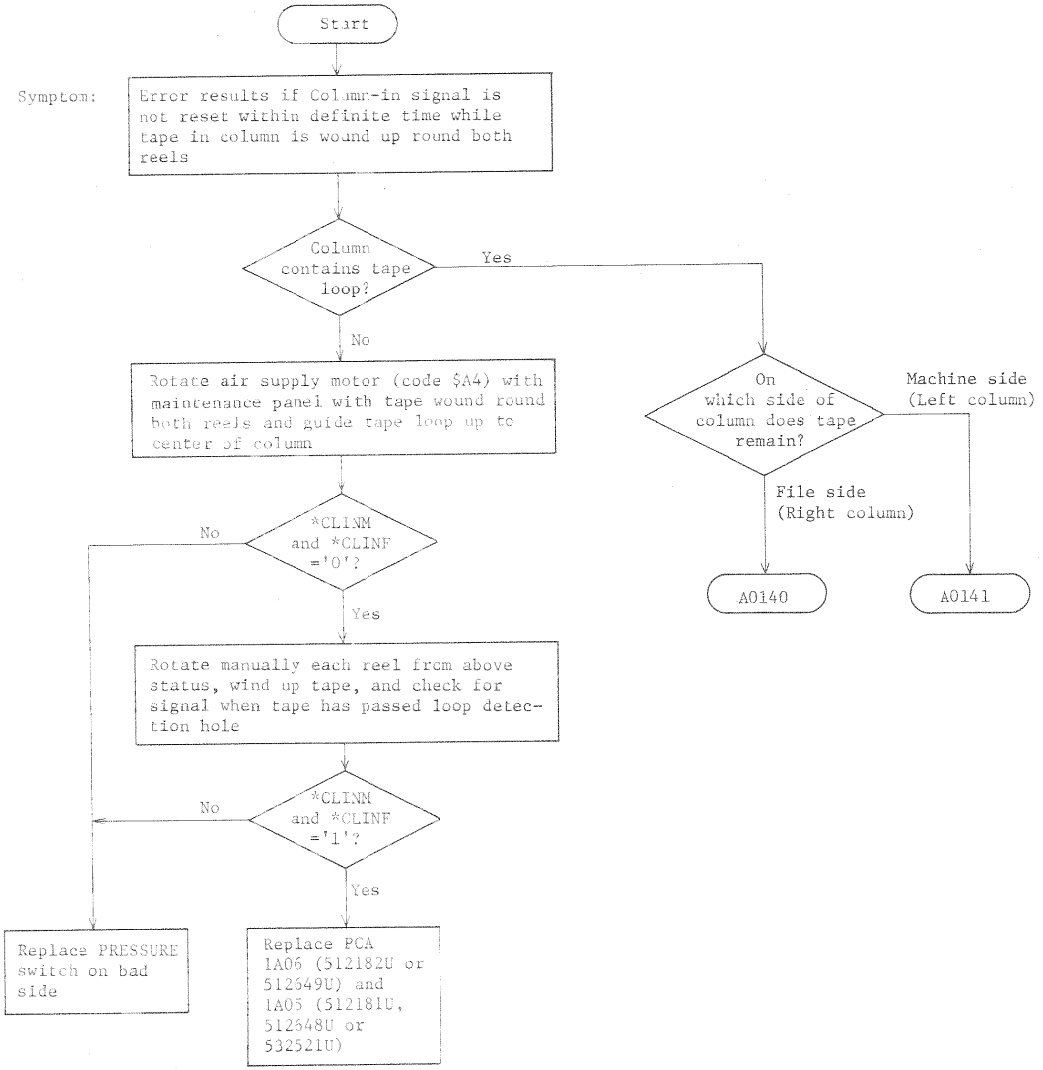
A3001	Unload Timing Chart



A3010	Unloading cannot be Performed.



A3020	Error Code = 36, 37



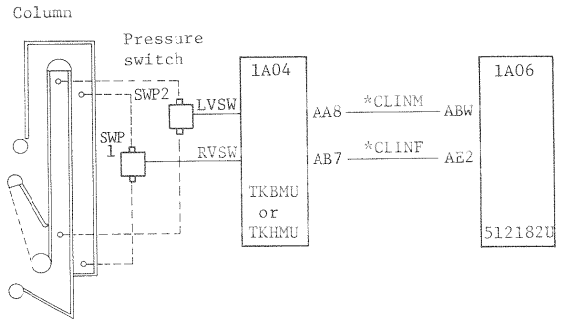
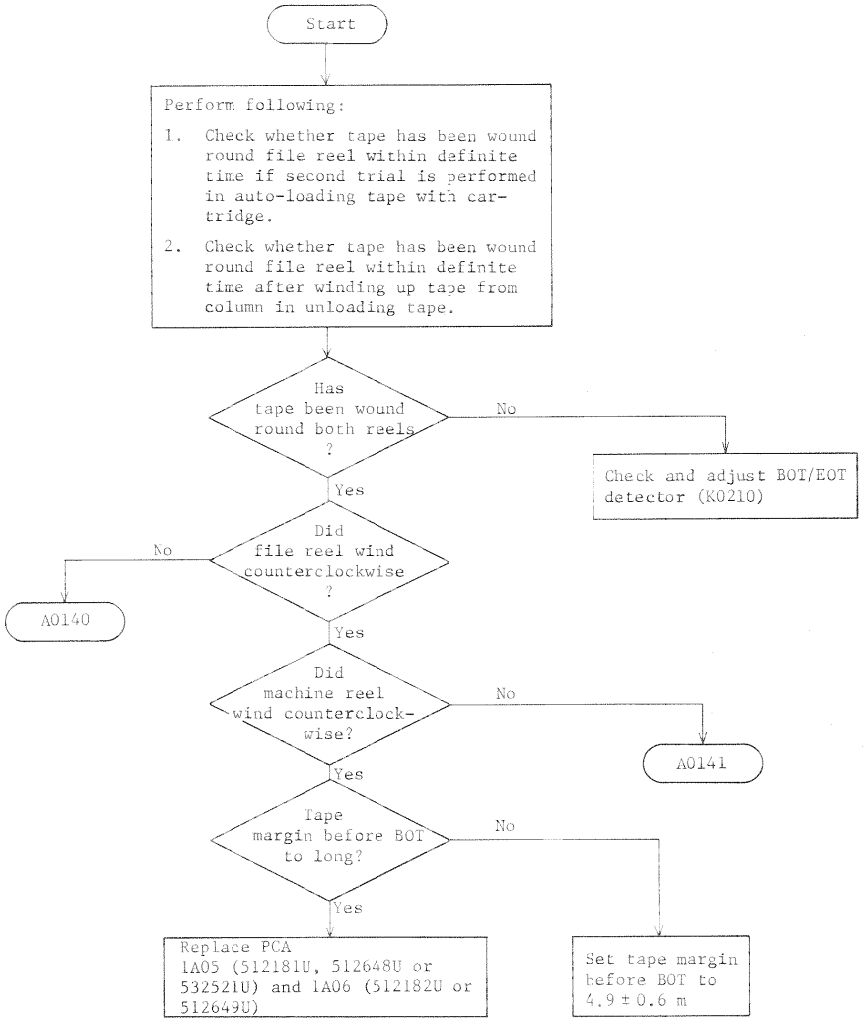
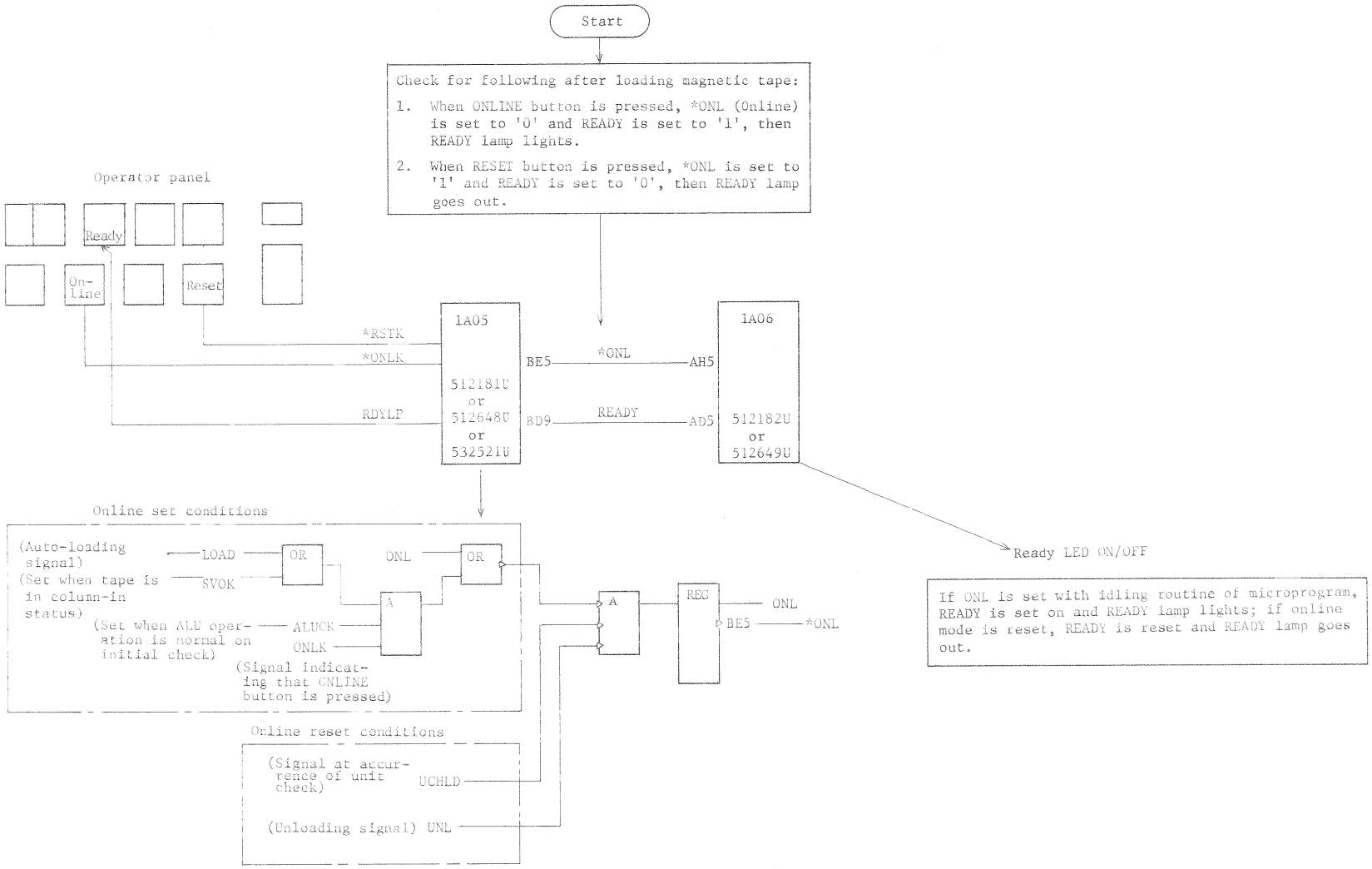


Fig. 1

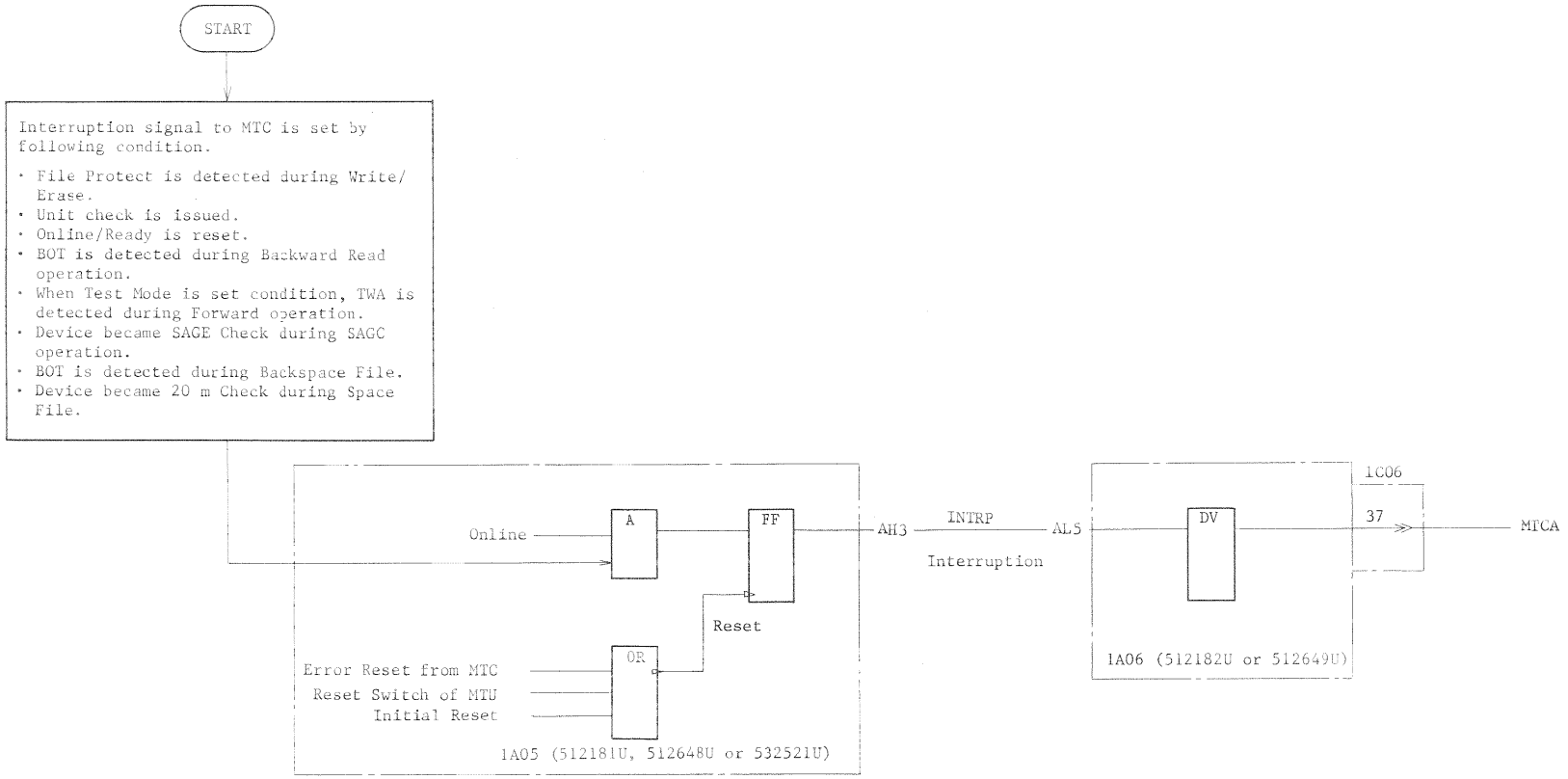
A3030	Error Code = 38, 48



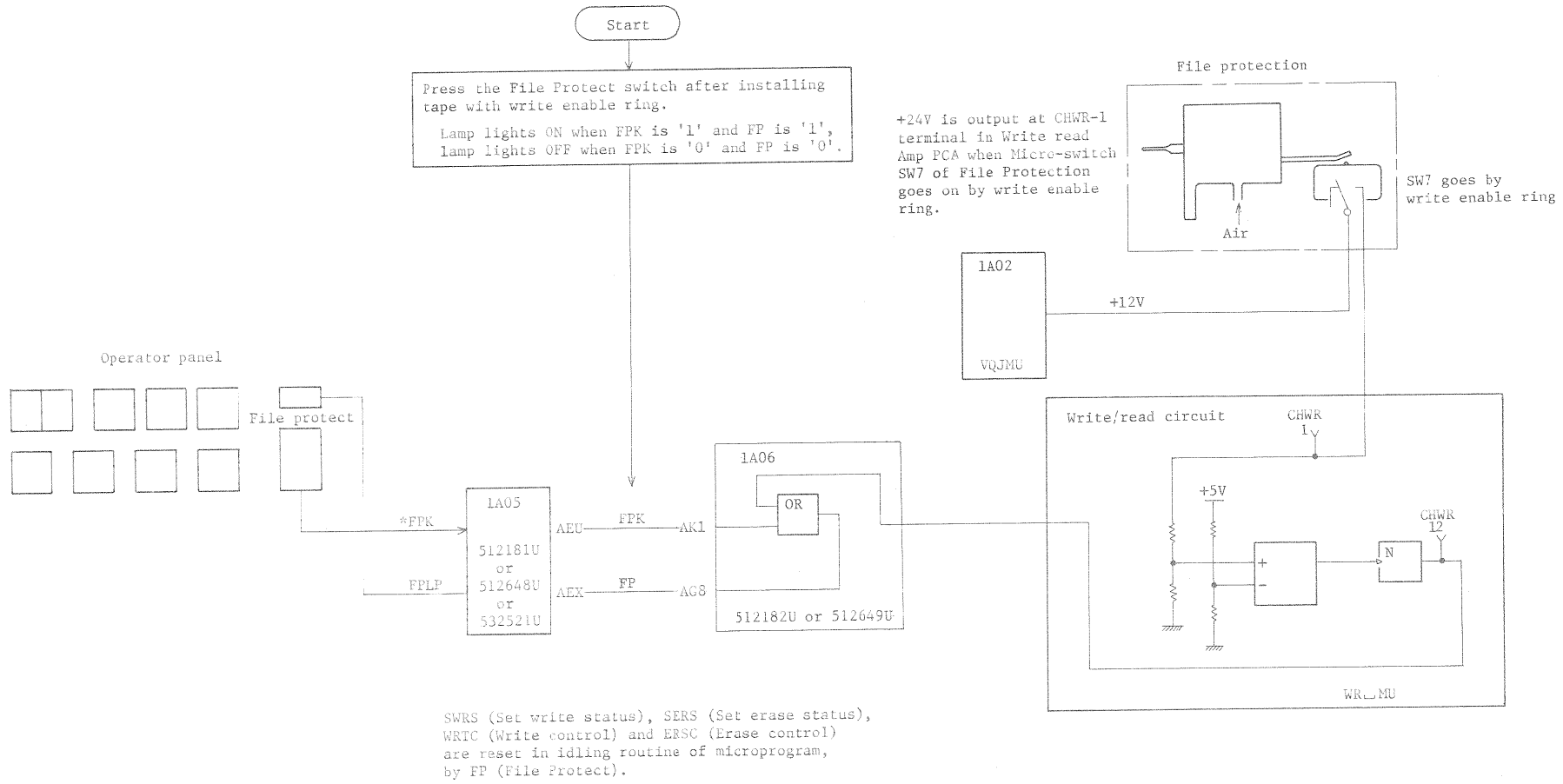
A4000	Ready Troubleshooting



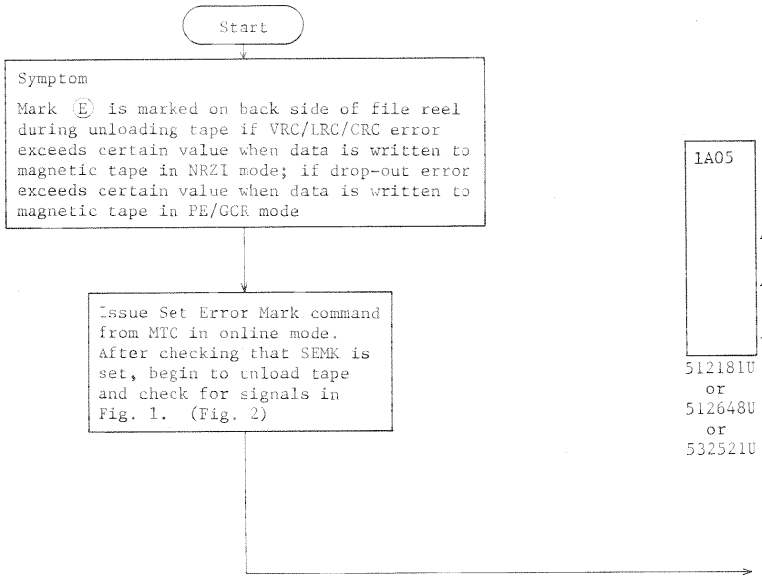
A4010	Interruption



A5000	File Protection and Lamp Trouble



A6000	Error Marker Drive



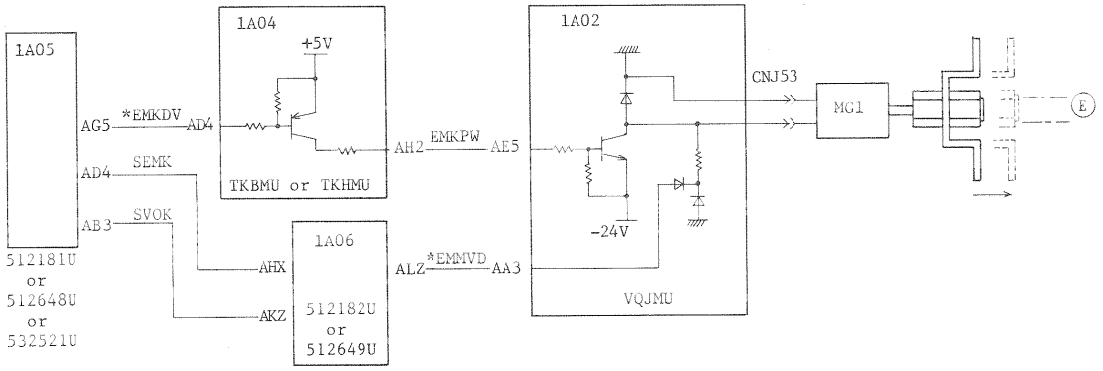


Fig. 1

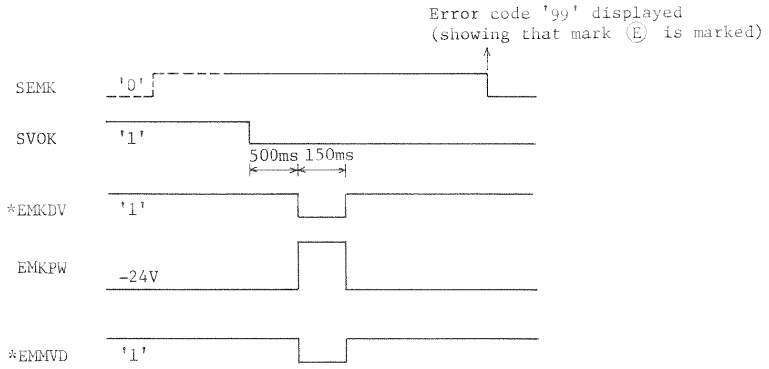
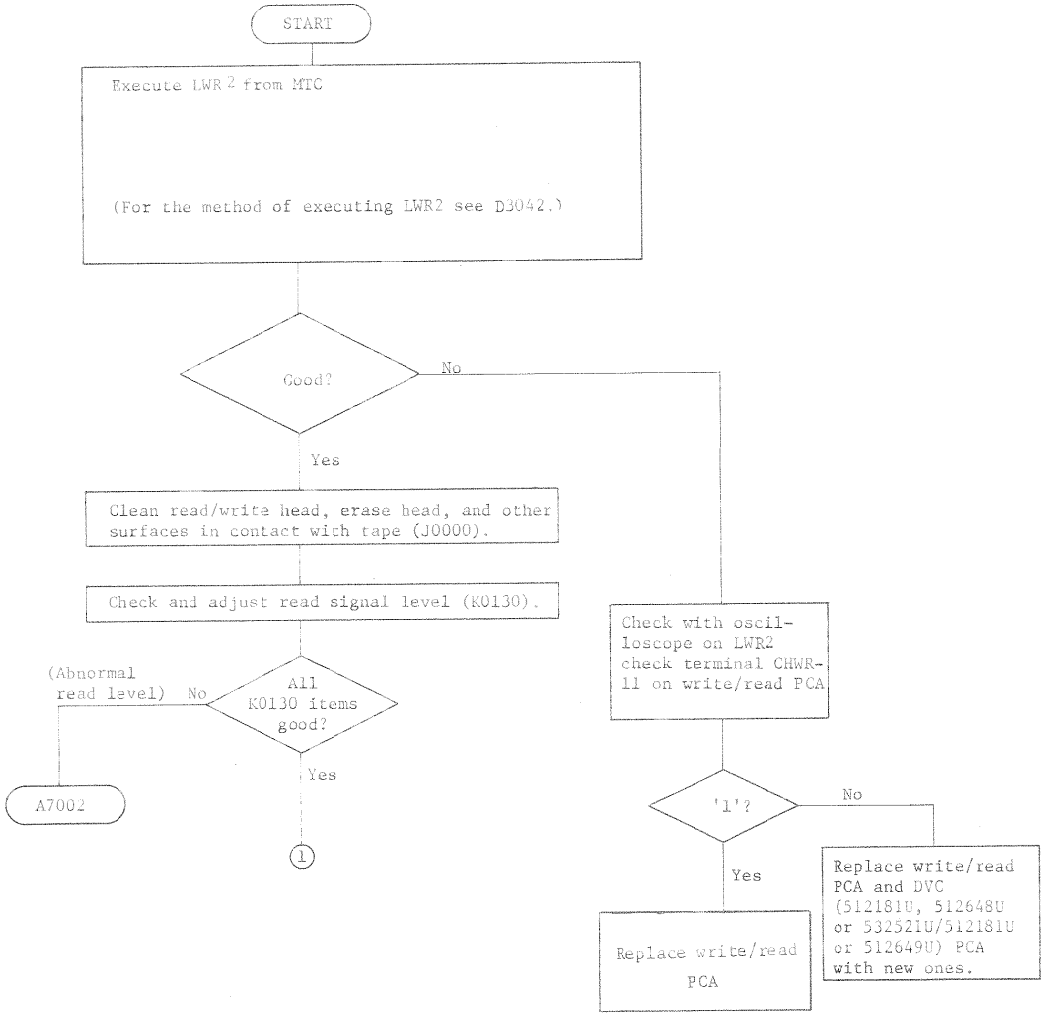
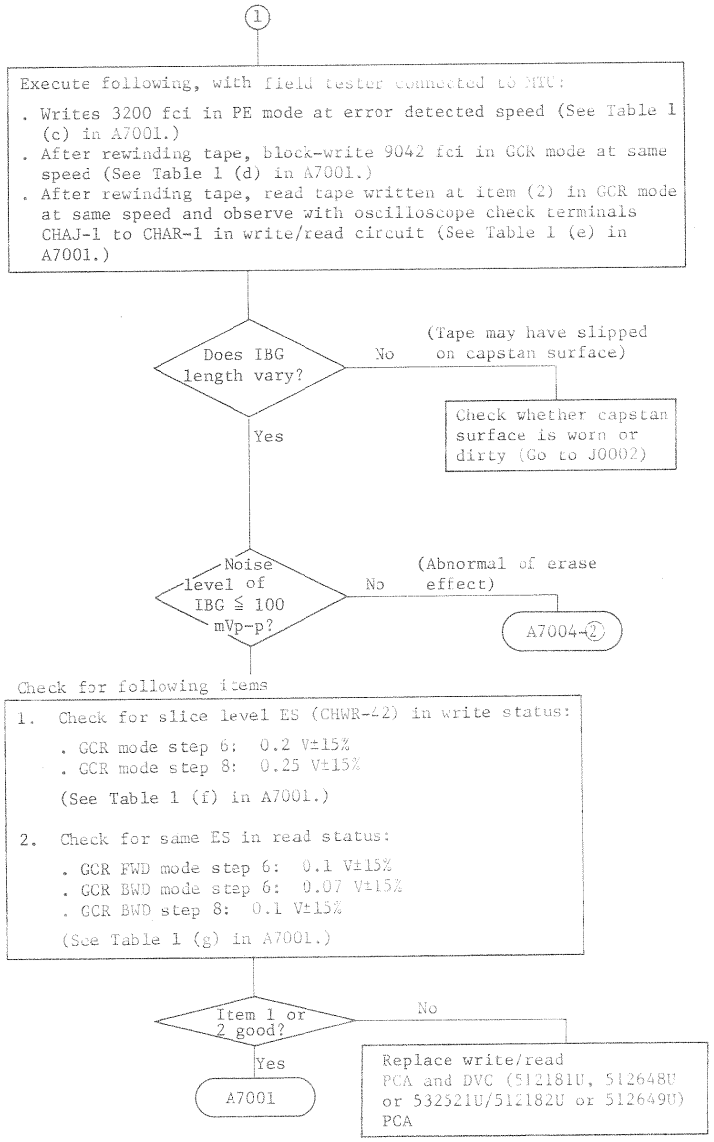


Fig. 2

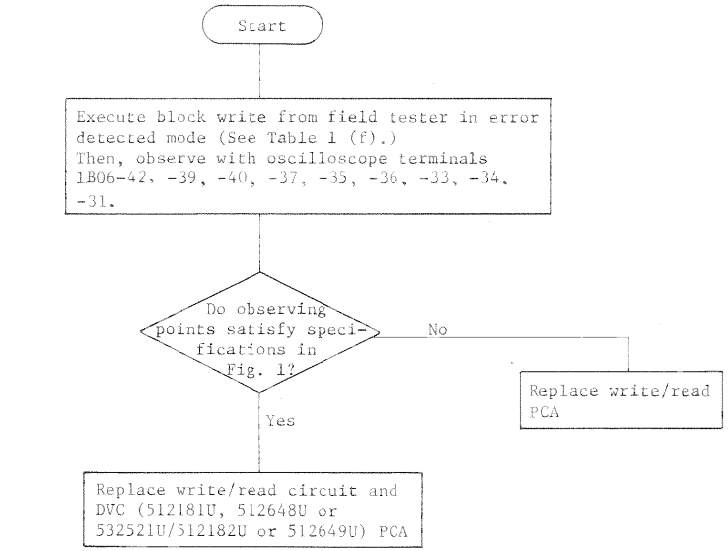
A7000	Read/Write Section Troubleshooting Procedures

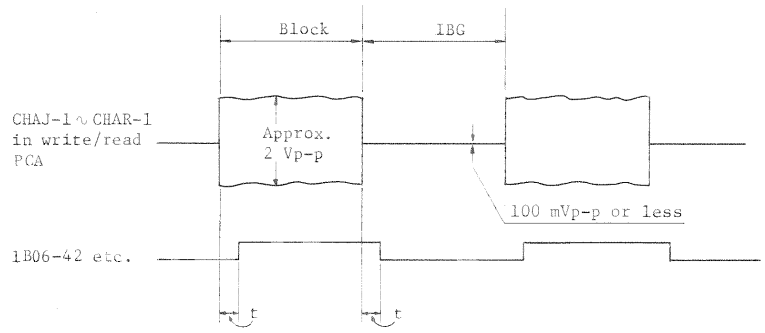
If a malfunction occurs in read/write operation of a 6250/1600 rpi MTU, then take the following troubleshooting procedures.





A7001	Troubleshooting for Read/Write





t = 15 μs±30% (Tape speed; 75 ips)

t = 9 μs±30% (Tape speed; 125 ips)

t = 6 μs±30% (Tape speed; 200 ips)

Fig. 1

Table 1

Item	Operation	Procedure	Field tester		Remarks
			Code	Setting switch	
(a)	Write mode	1	Low speed PE : $E8 Low speed GCR: $EA High speed PE: $EC High speed GCR: $EE	SSS	
(b)	Read mode	1	Low speed PE : $E0 Low speed GCR: $E2 High speed PE: $E4 High speed GCR: $E6	SSS	
(c)	PE 3200 fci write	1	Set to PE write mode at item (a).	SSS	
		2	$89	SSS	
(d)	Block write	1	Set to write mode specified at item (a).	SSS	
		2	$25	SSS	
(e)	FWD read	1	Set to read mode specified at item (b).	SSS	
		2	Low speed: $01 High speed: $02	SSS	
(f)	GCR write mode with specified step	1	Step specification: Step 6: $C6 Step 8: $C8	Switch SSS sw twice.	First switching causes tape to run; second switching causes tape to stop.
		2	Low speed GCR write: $EA	SSS	
(g)	GCR read mode with specified step	1	Step/running direction specification: FWD step 6: $C6 FWD step 8: $C8 BWD step 6: $D6 BWD step 8: $D8	Switch SSS sw twice.	

Note: For details see "Maintenance Panel Operating Method".

A7002	Abnormality for Read Level (1)

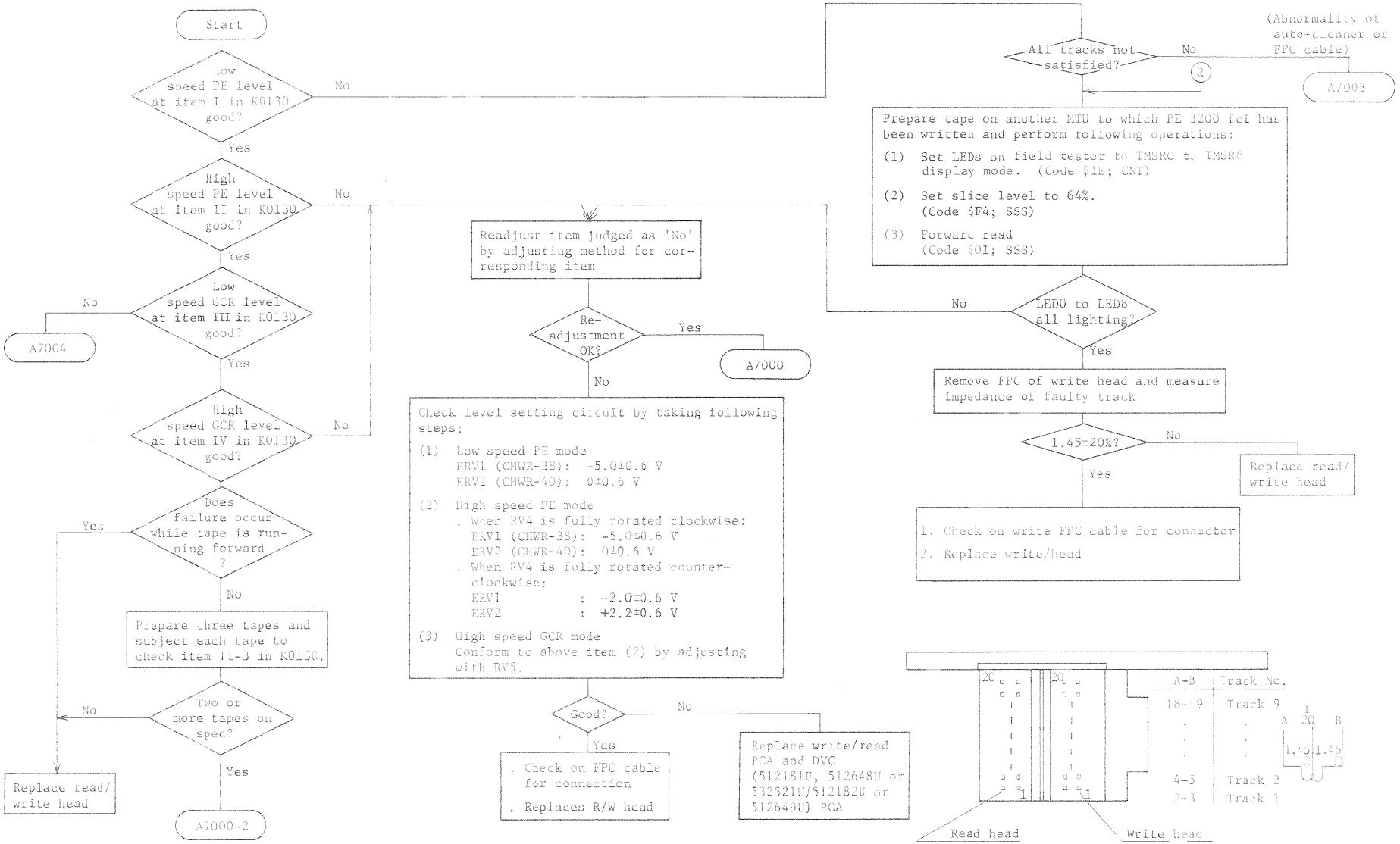
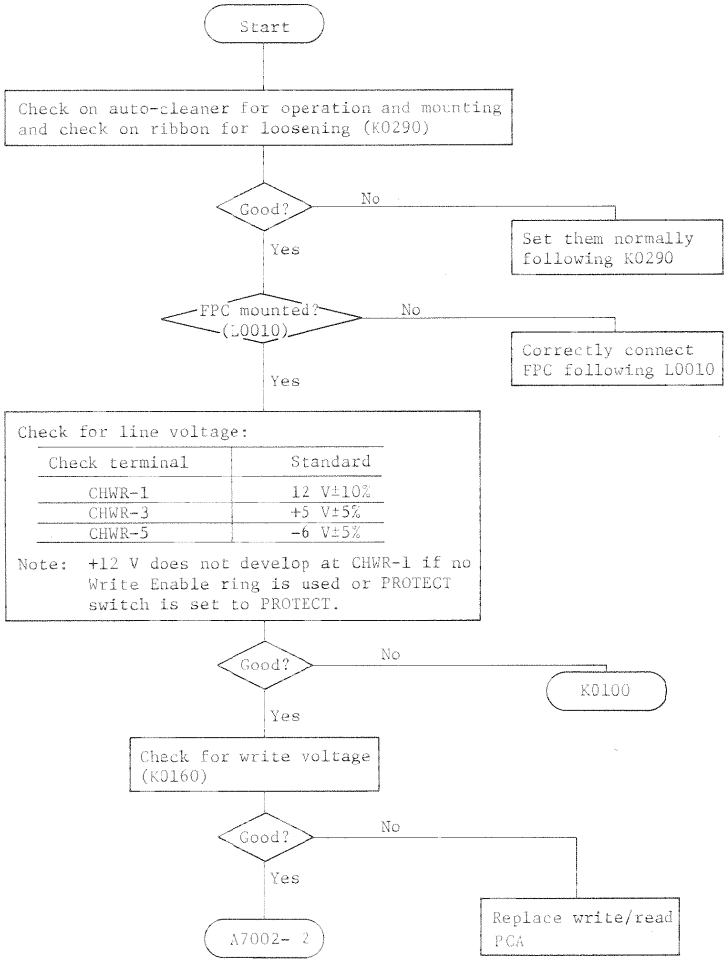
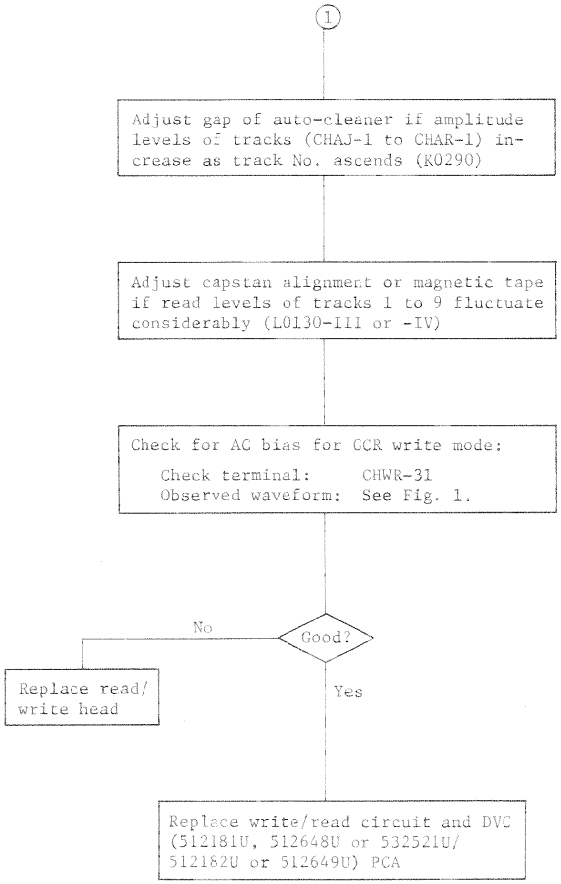


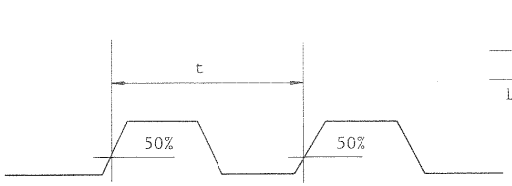
Fig. 1 R/W head (viewed from head connector side)

A7003	Abnormality for Read Level (2)



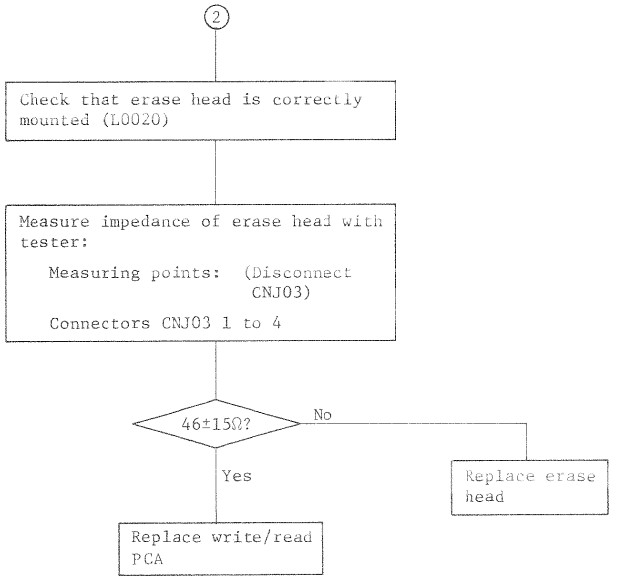
A7004	Abnormality for Read Level (3)





MTU Type	t[ns]
75/125 IPS MTU	260
125/200 IPS MTU	160

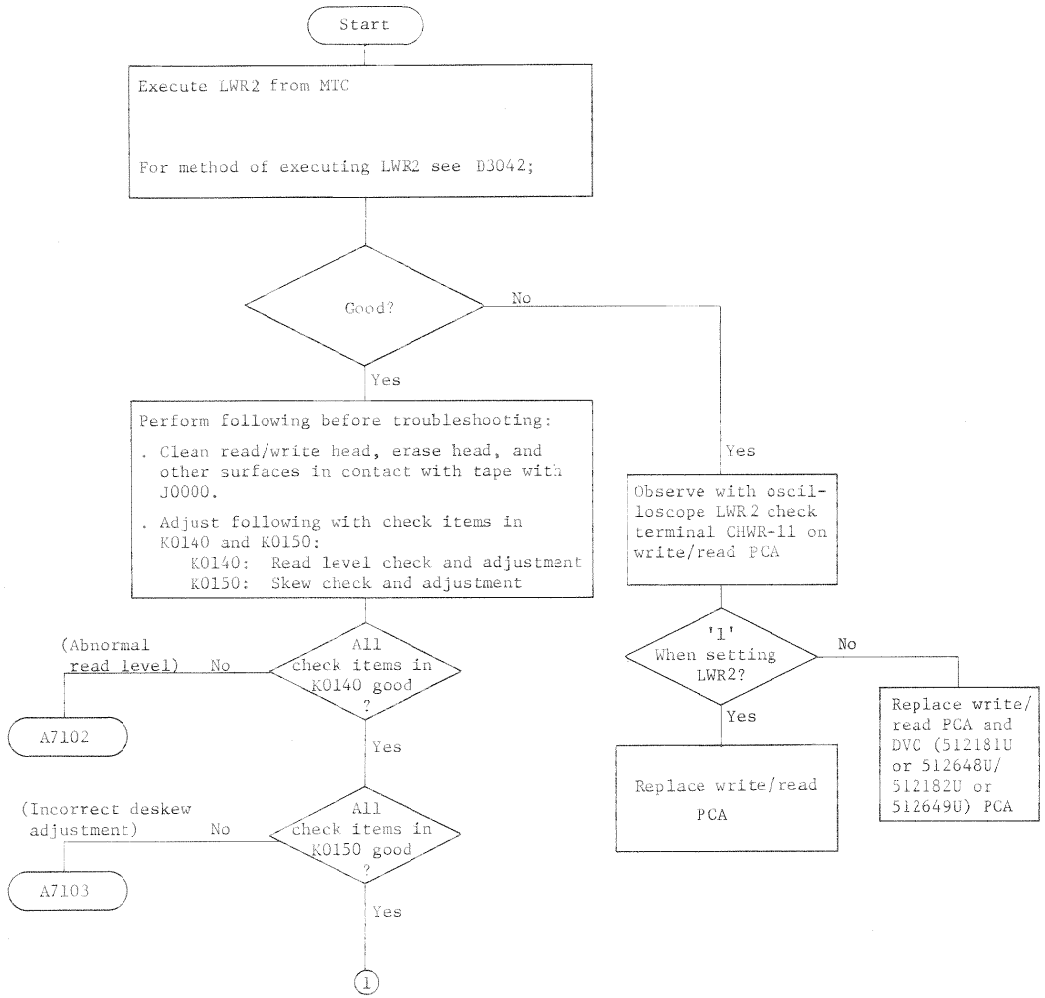
Fig. 1 AC bias waveform (CHWR-31)

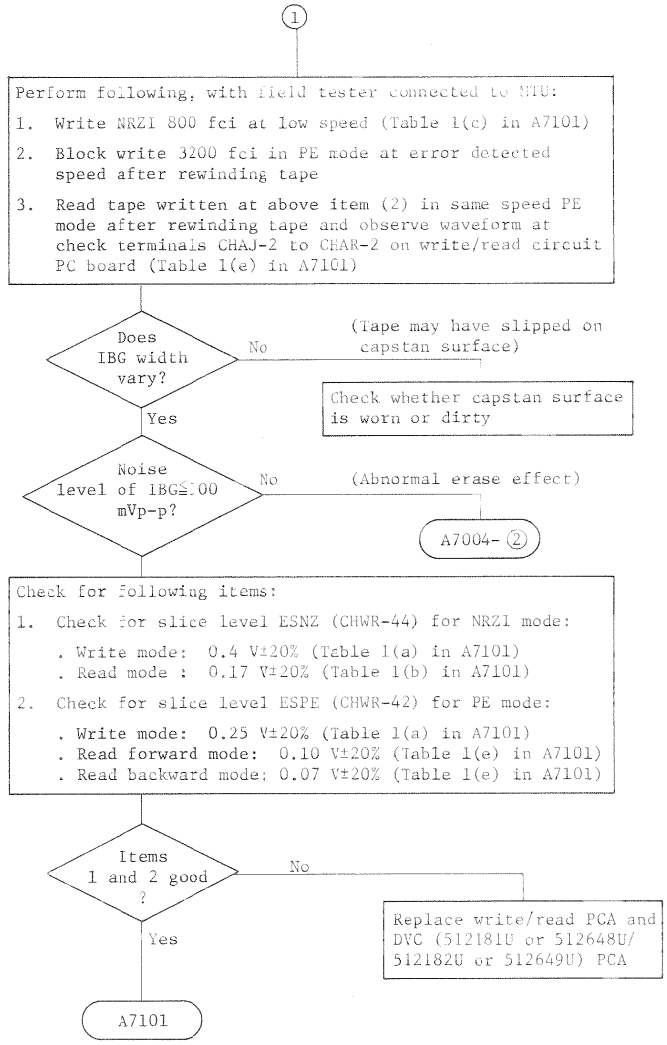


A7100	Troubleshooting for Read/Write Section (1600/800 rpi MTU) (1)

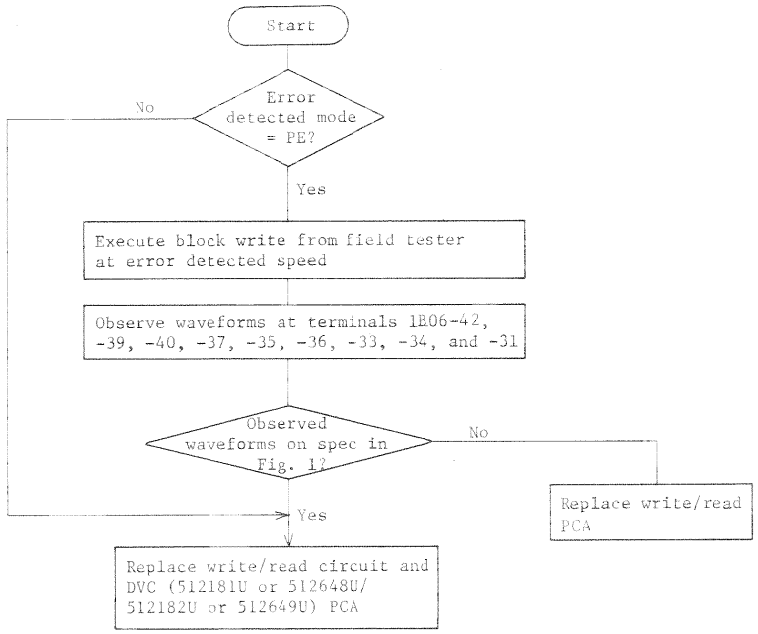
Symptom:

If a read/write system failure occurs in the 1600/800 rpi MTU, then perform troubleshooting in the following sequence:





A7101	Troubleshooting for Read/Write Section (1600/800 rpi MTU) (2)



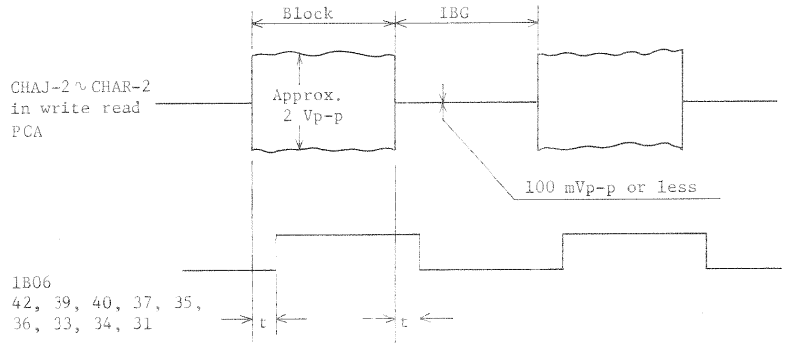


Fig. 1
t = 25 μs±30% (Tape speed: 75 ips)
t = 15 μs±30% (Tape speed: 125 ips)
t = 9 μs±30% (Tape speed: 200 ips)

Table 1

Item	Operation	Procedure	Field tester		Remarks
			Code	Setting switch	
(A)	Write mode	1	NRZI : $E8 Low speed PE : $EA High speed PE : $EE	SSS	
(b)	Read mode	1	NRZI : $E0 Low speed PE : $E2 High speed PE : $E6	SSS	
(c)	NRZI 800 fci write	1	$89	SSS	
(d)	Block write	1	Set to write mode specified at item (a)	SSS	
		2	$25	SSS	
(e)	FWD read action	1	Set to read mode specified at item (b)	SSS	Does not operate at the high speed while in NRZI mode.
		2	Low speed FWD : $01 High speed FWD : $02 Low speed BWD : $41 High speed BWD : $42	SSS	

Note: For details see Field Tester Operating Method".

A7102	Abnormality for Read Level (1600/800 rpi MTU) (1)

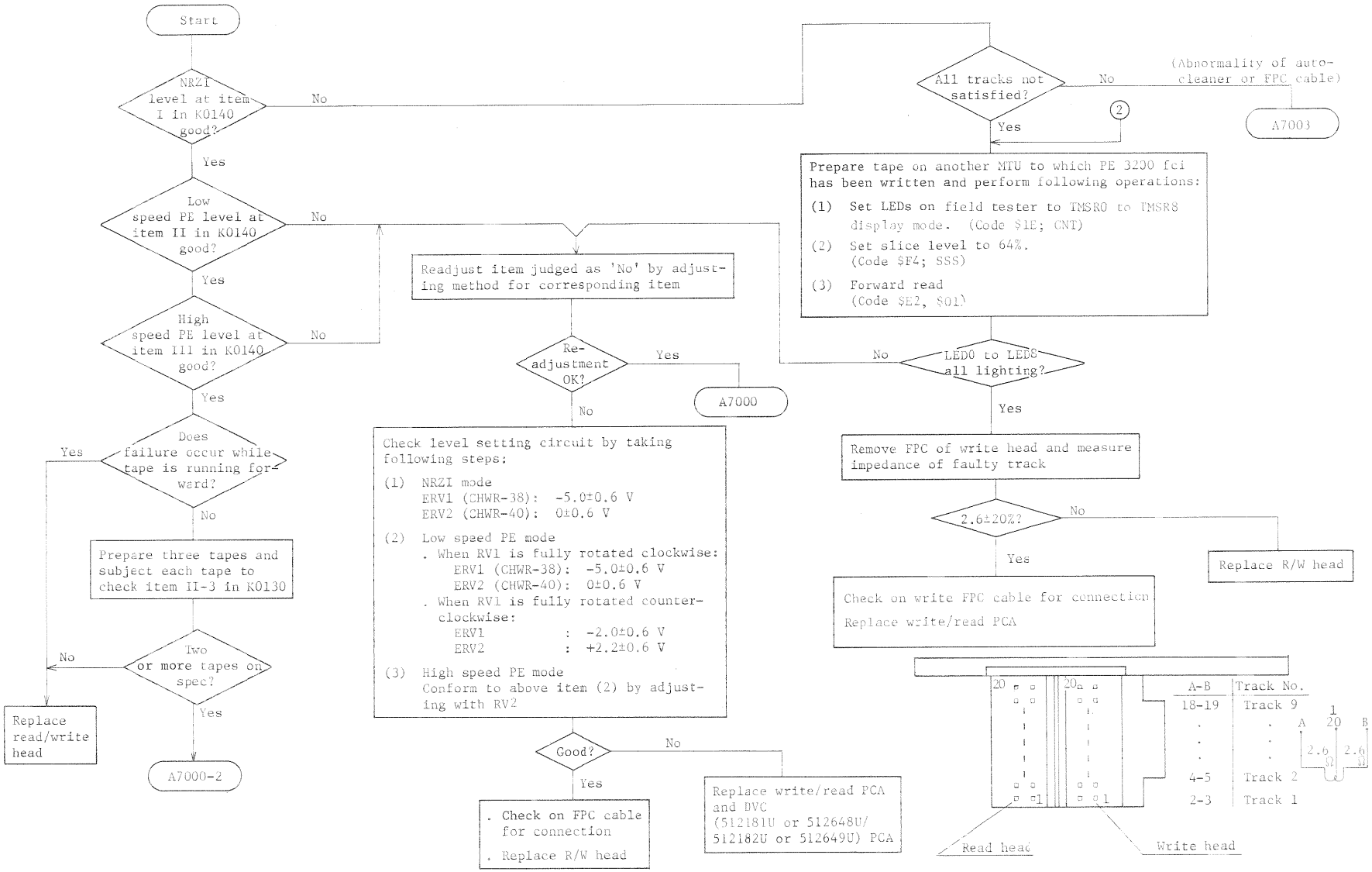
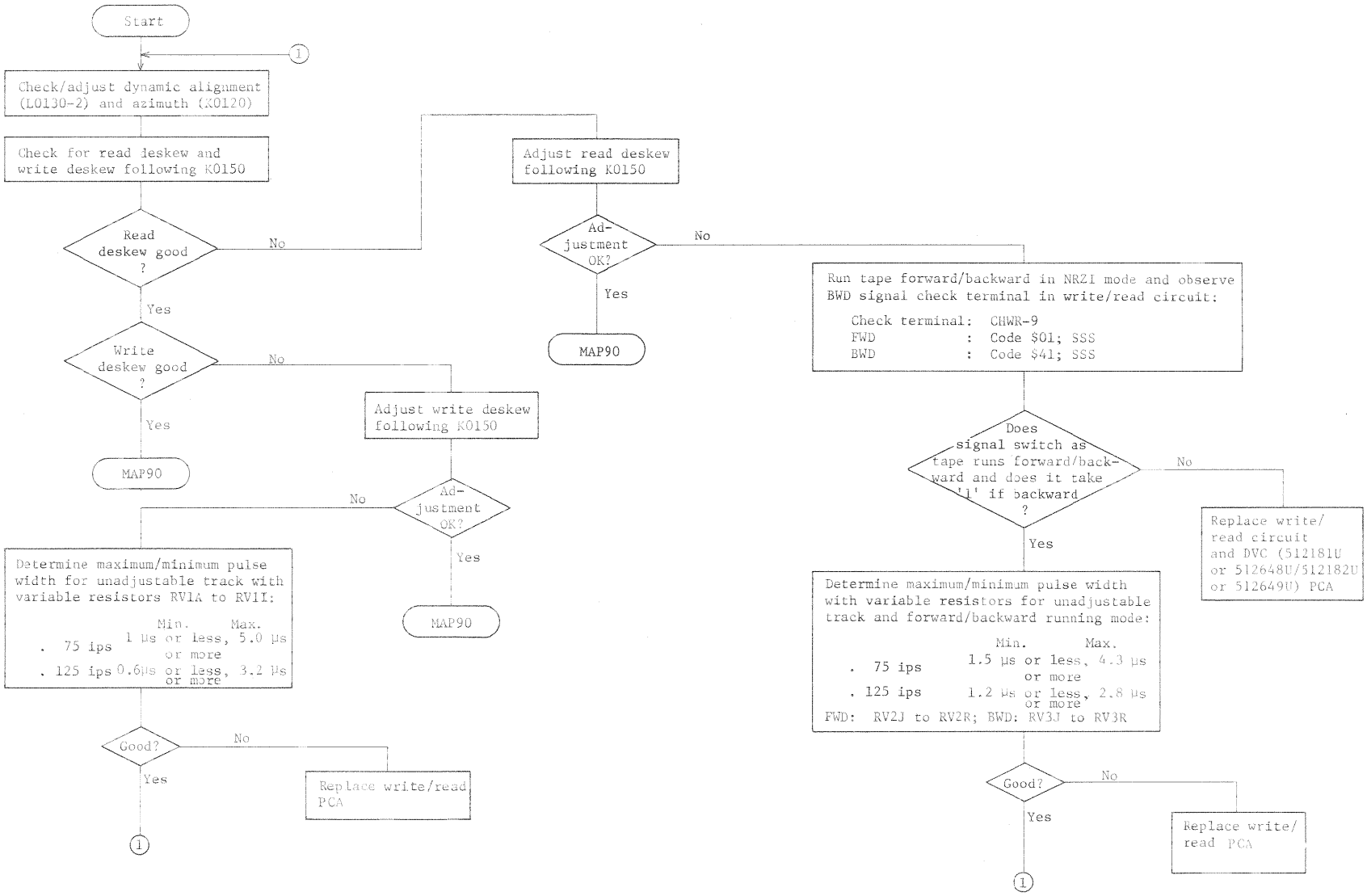


Fig. 1 R/W head
(viewed from head connector side)

A7103	Abnormality for Read Level (1600/800 rpi MTU) (2)



A7104 : Deskew (1600/800 rpi MTU)

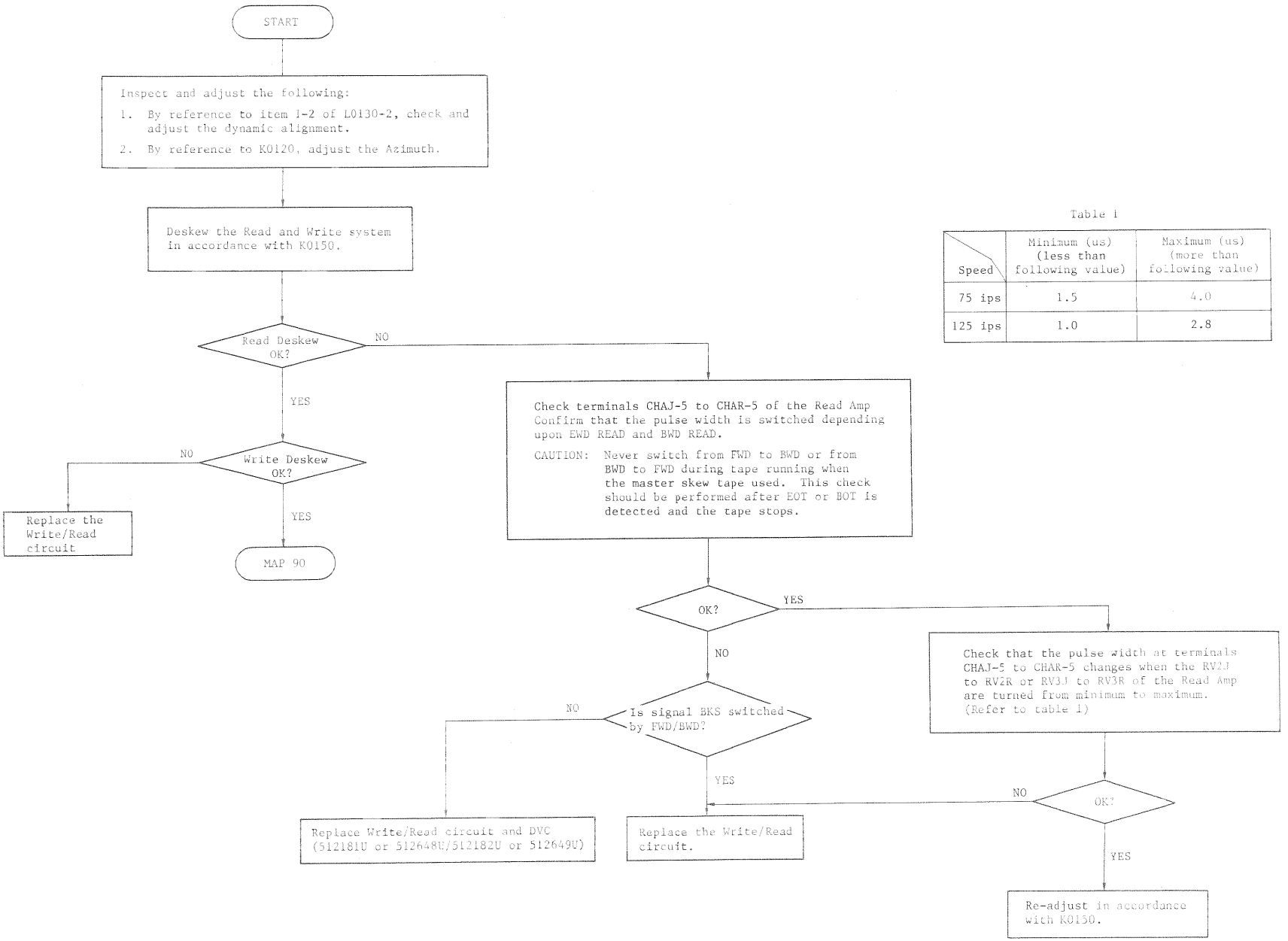
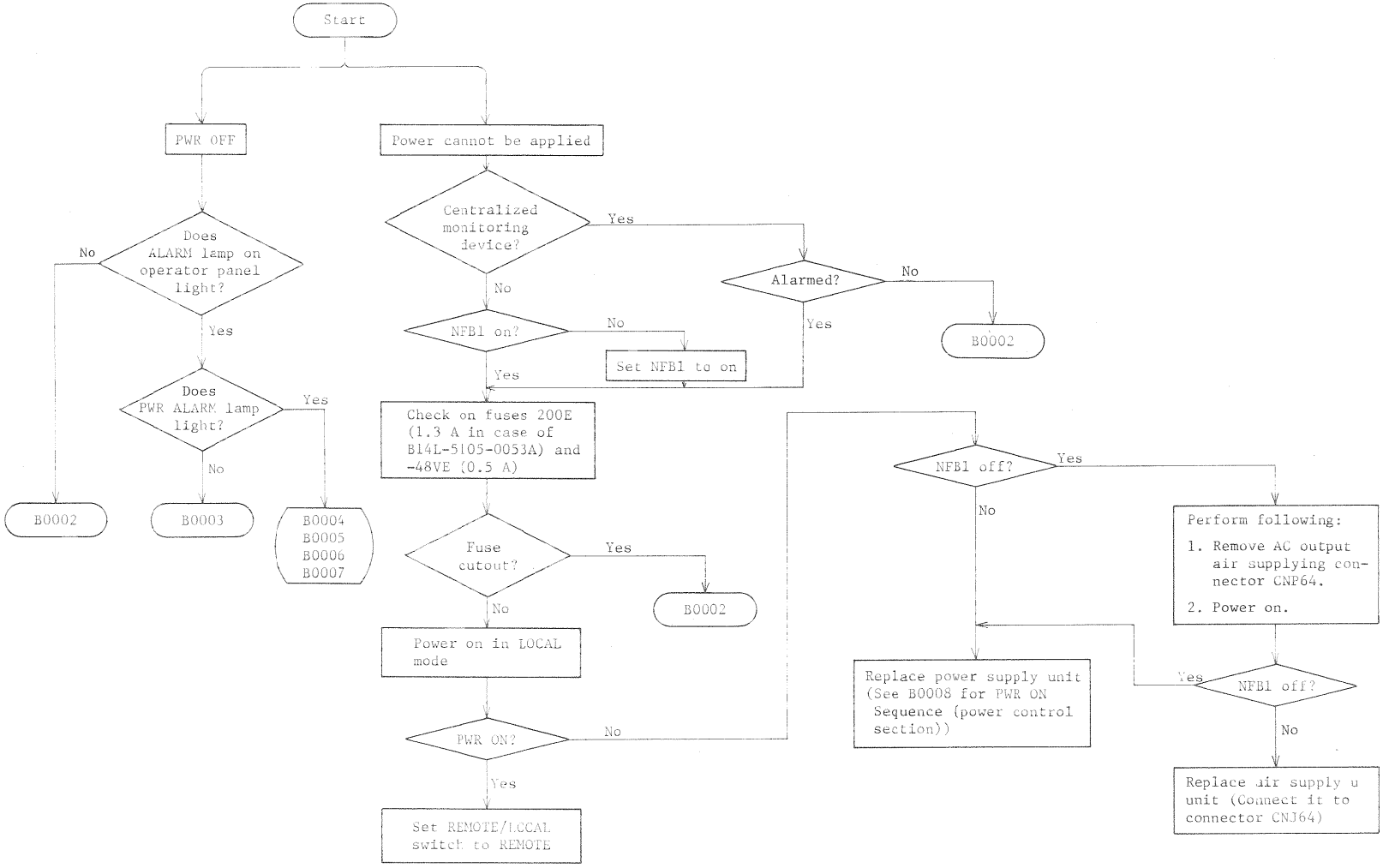


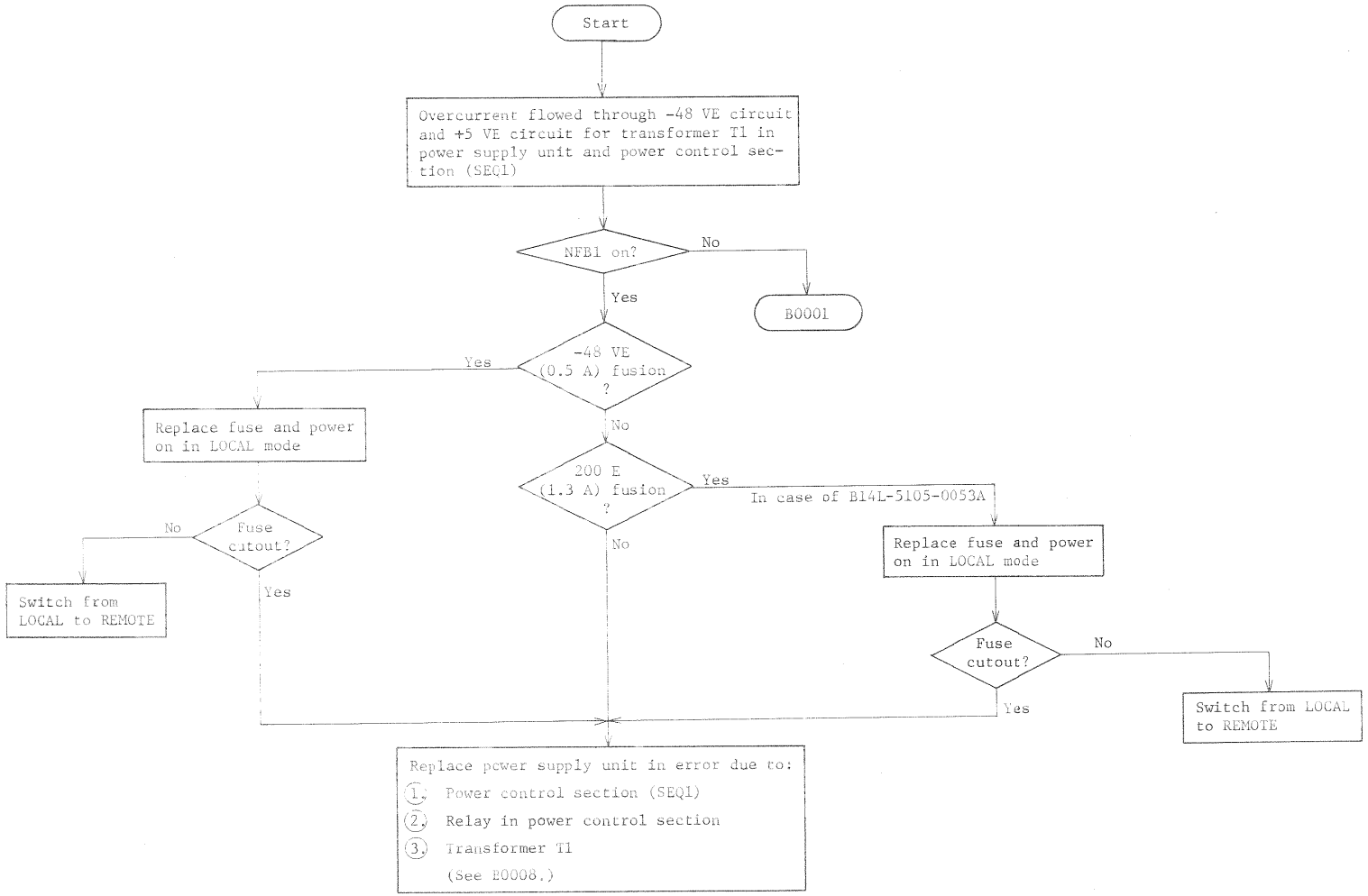
Table 1

Speed	Minimum (us) (less than following value)	Maximum (us) (more than following value)
75 ips	1.5	4.0
125 ips	1.0	2.8

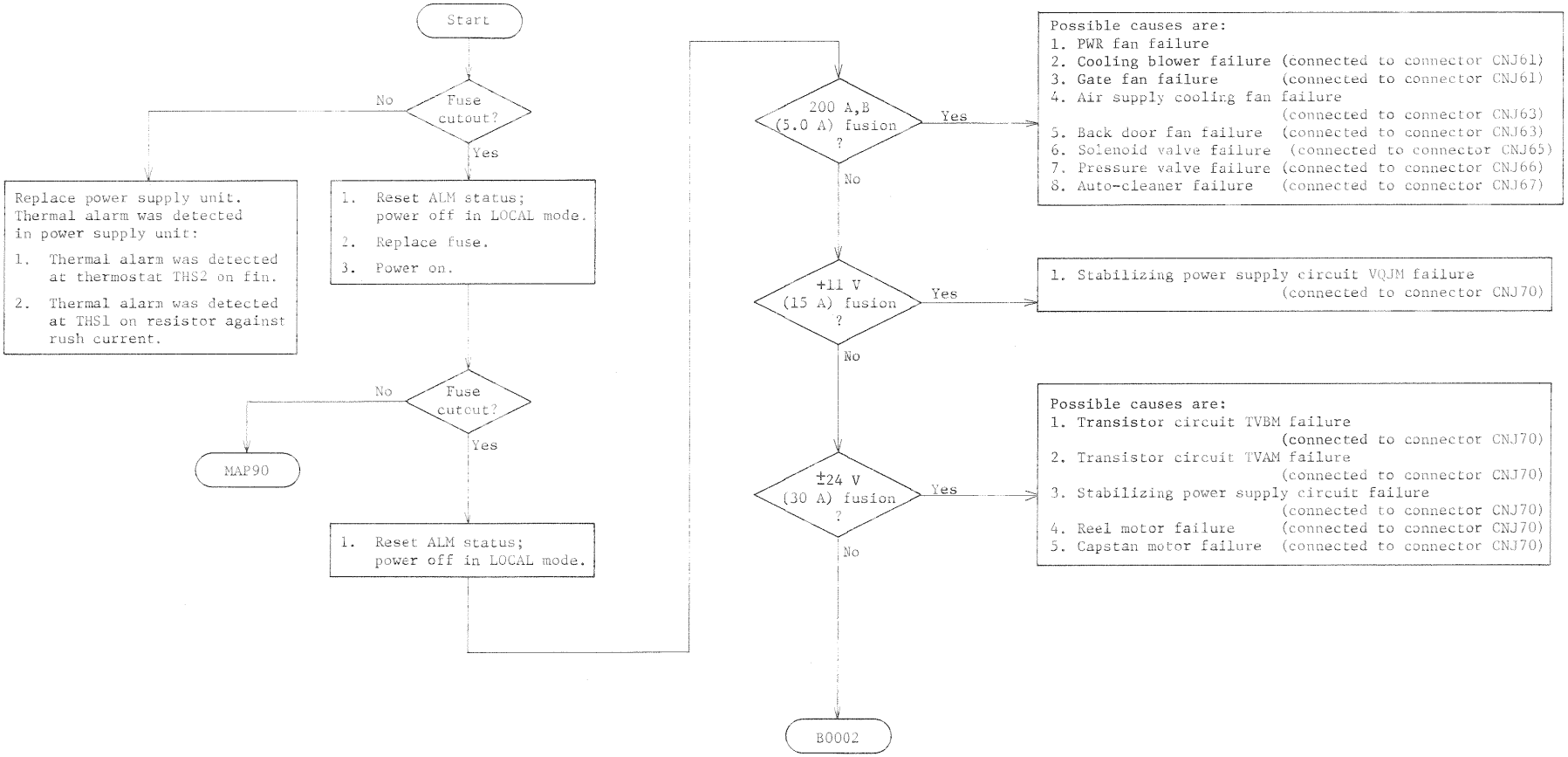
B0001	MTU Power Supply Troubleshooting



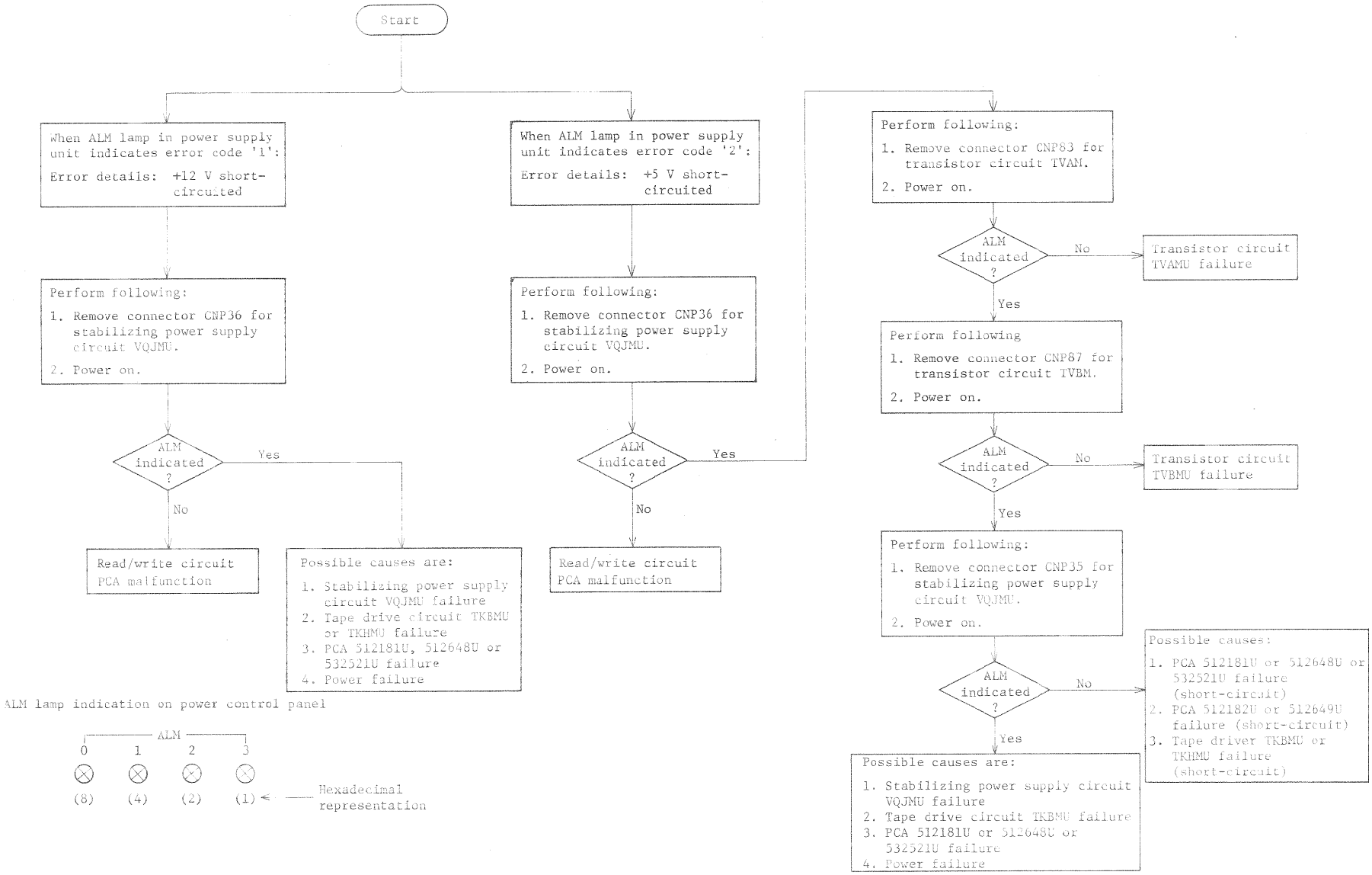
B0002	Power On Impossible



B0003	Alarm LED Indication by Power Supply Trouble

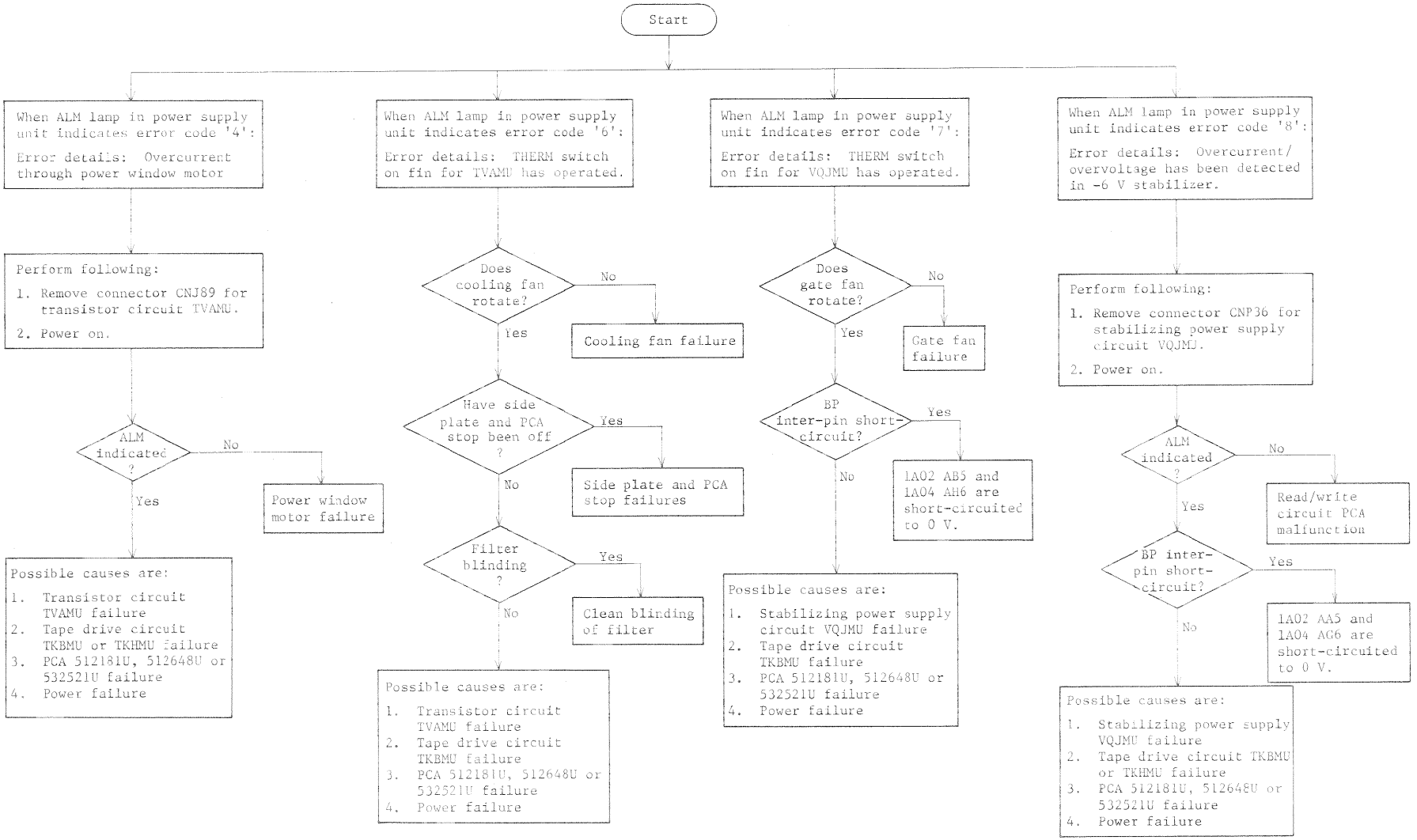


B0004	Alarm LED Indication by MTU Trouble (1)

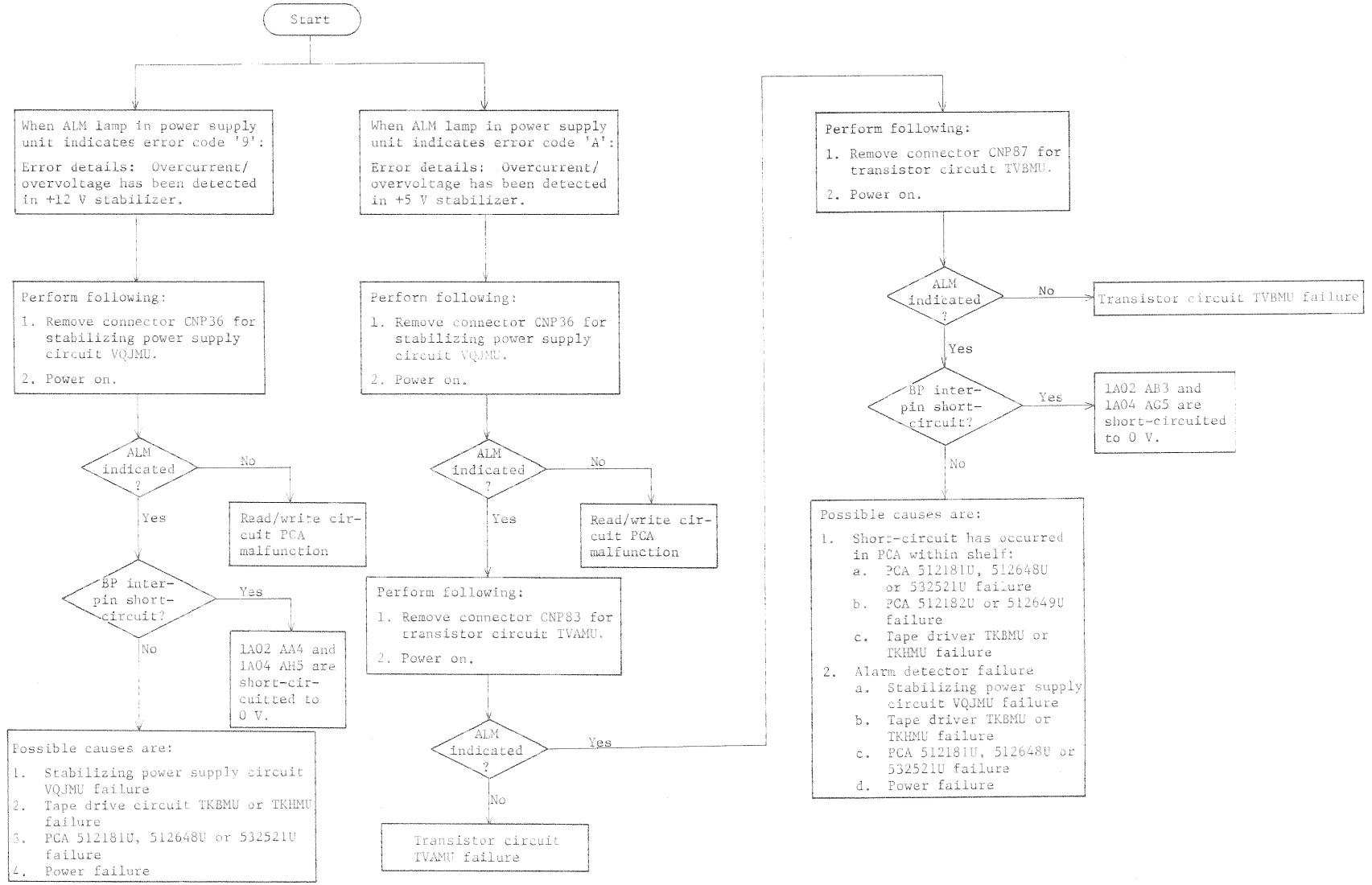


ALM lamp indication on power control panel

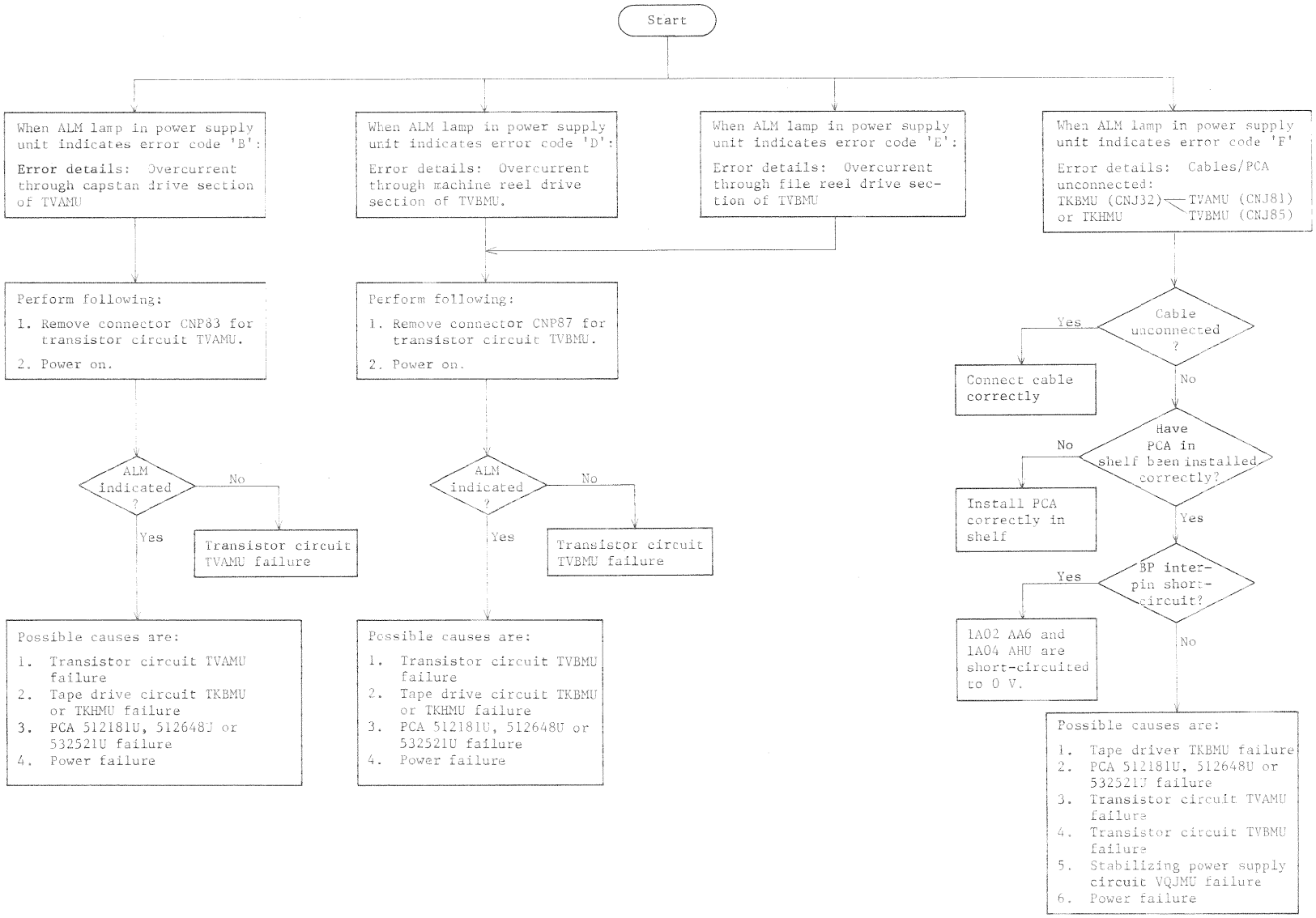
B0005	Alarm LED Indication by MTU Trouble (2)



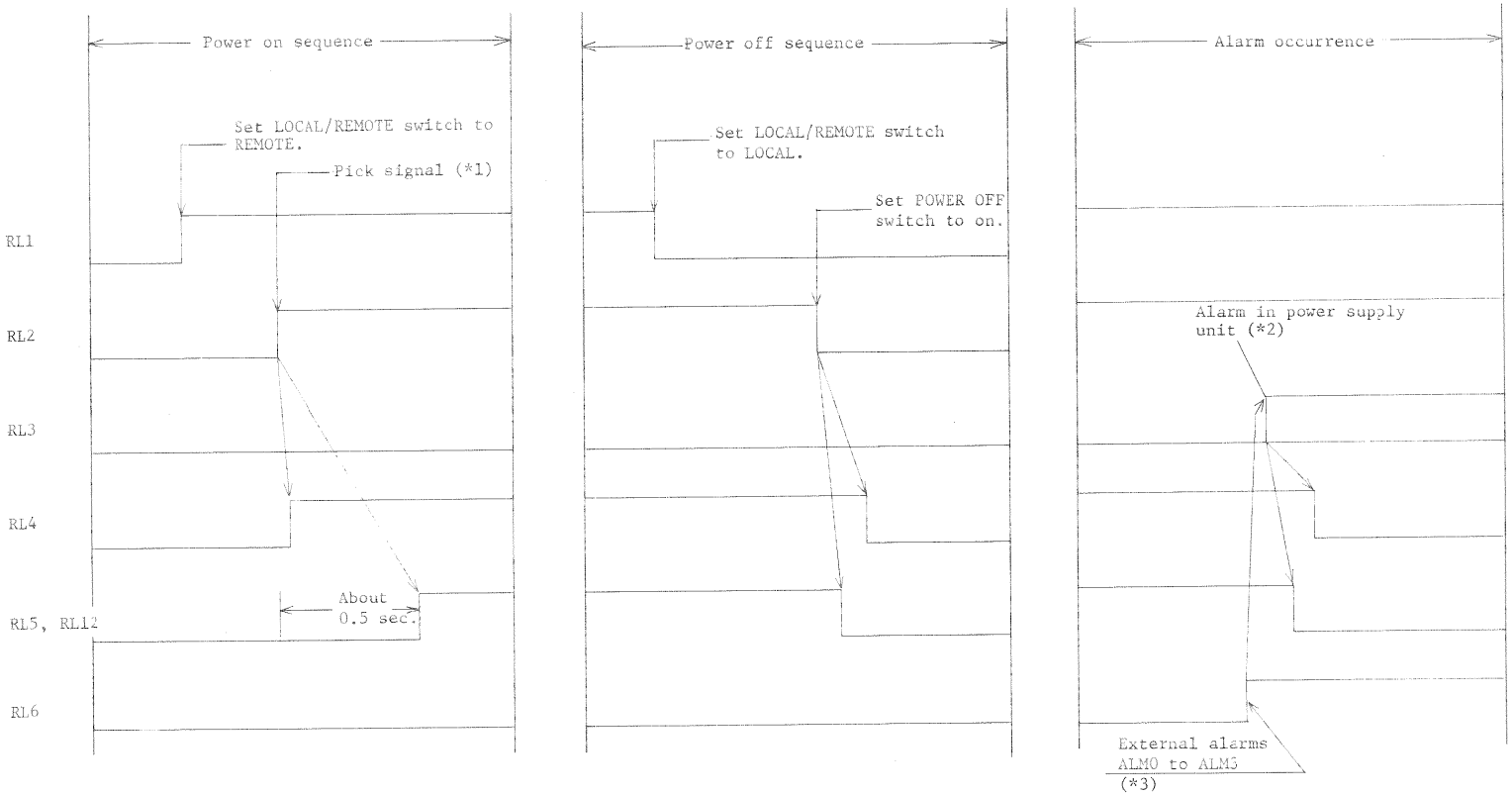
B0006	Alarm LED Indication by MTU Trouble (3)



B0007	Alarm LED Indication by MTU Trouble (4)



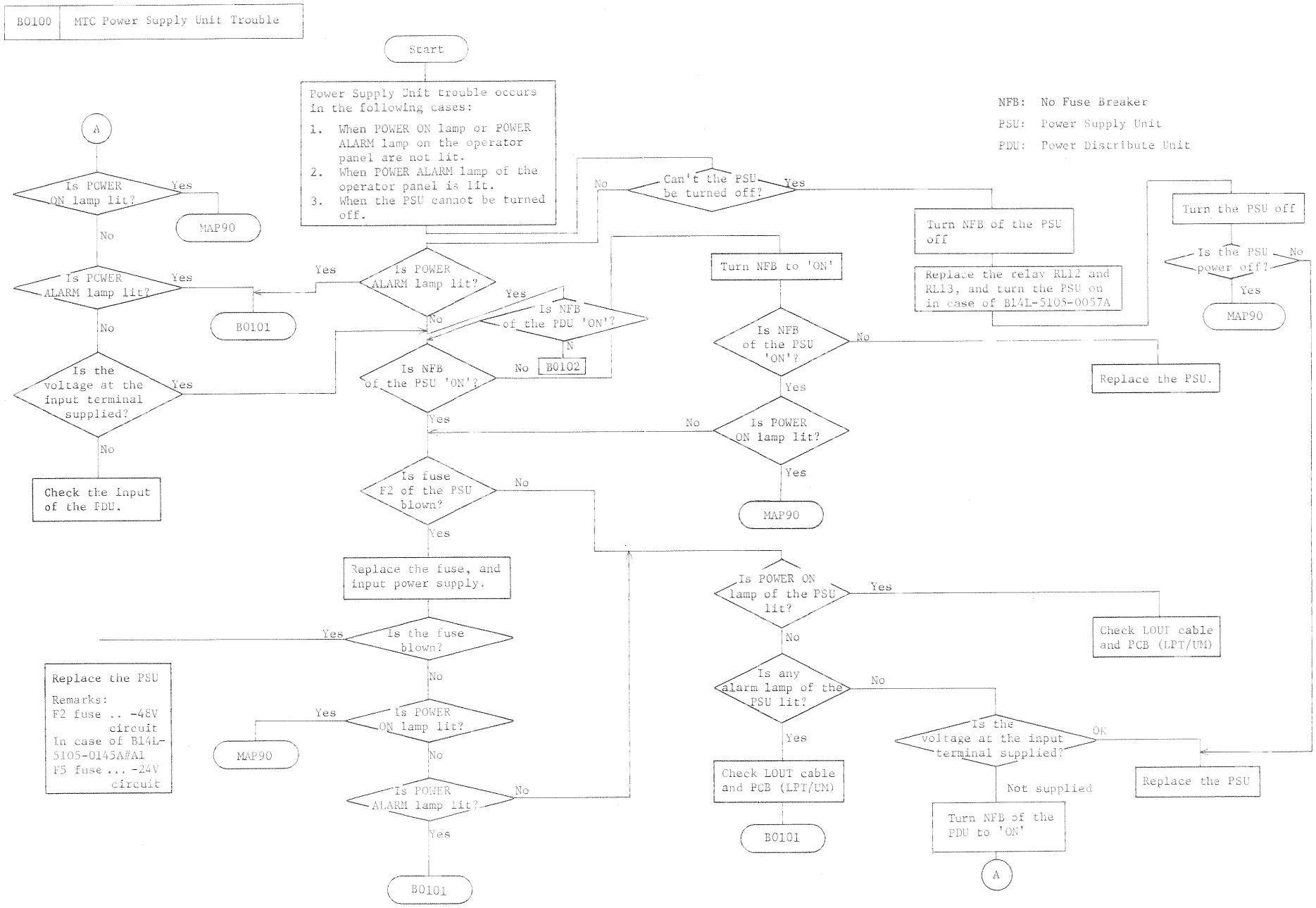
B0008	Power ON/OFF Sequence



*1: RL1 is off while power is applied in the LOCAL mode.
If POWER ON switch is set to ON, then RL2 is set on and the relays are sequentially set on.

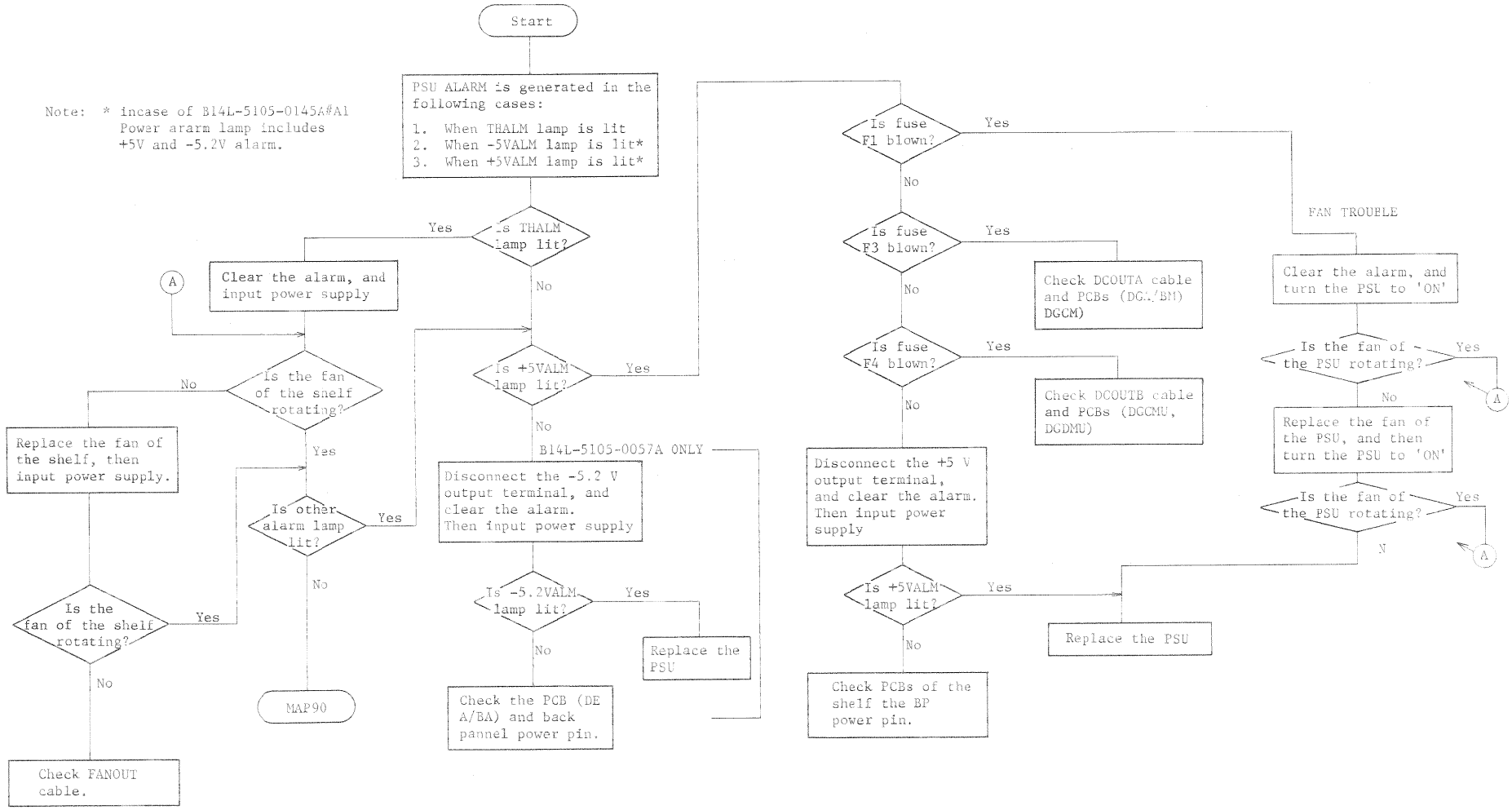
*2: If any fuses except -48 VE and 200E are melted or a thermal alarm status in the power supply unit is detected by THS1 and THS2, then RL3 is set on and the powering off sequence starts.

*3: If an external alarm status occurs in a section other than the power supply section, then RL6 is set on, then RL3 operates, then the powering off sequence starts.


B0100 MTC Power Supply Unit Trouble
Start
Power Supply Unit trouble occurs in the following cases:
1. When POWER ON lamp or POWER ALARM lamp on the operator panel are not lit.
2. When POWER ALARM lamp of the operator panel is lit.
3. When the PSU cannot be turned off.
NFB: No Fuse Breaker
PSU: Power Supply Unit
PDU: Power Distribute Unit
A
Is POWER ON lamp lit?
Yes
MAP90
No
Is POWER ALARM lamp lit?
Yes
B0101
No
Is the voltage at the input terminal supplied?
Yes
No
Check the input of the FDU.
Is POWER ALARM lamp lit?
Yes
No
Is NFB of the PDU 'ON'?
Yes
No
B0102
Is NFB of the PSU 'ON'?
No
Yes
Is fuse F2 of the PSU blown?
No
Yes
Replace the fuse, and input power supply.
Is the fuse blown?
Yes
Replace the PSU
Remarks:
F2 fuse .. -48V circuit
In case of B14L-5105-0145A#A1
F5 fuse ... -24V circuit
No
Is POWER ON lamp lit?
Yes
MAP90
No
Is POWER ALARM lamp lit?
No
Yes
B0101
Can't the PSU be turned off?
No
Yes
Turn NFB of the PSU off
Replace the relay RL12 and RL13, and turn the PSU on in case of B14L-5105-0057A
Turn the PSU off
Is the PSU power off?
No
Yes
MAP90
Turn NFB to 'ON'
Is NFB of the PSU 'ON'?
No
Replace the PSU.
Yes
Is POWER ON lamp lit?
No
Yes
MAP90
Is POWER ON lamp of the PSU lit?
Yes
Check LOUT cable and PCB (LPT/UM)
No
Is any alarm lamp of the PSU lit?
No
Yes
Check LOUT cable and PCB (LPT/UM)
B0101
Is the voltage at the input terminal supplied?
OK
Not supplied
Replace the PSU
Turn NFB of the PDU to 'ON'
A

B0101	PSU Alarm

— MTC —



B0102	MTC Power Supply ALARM

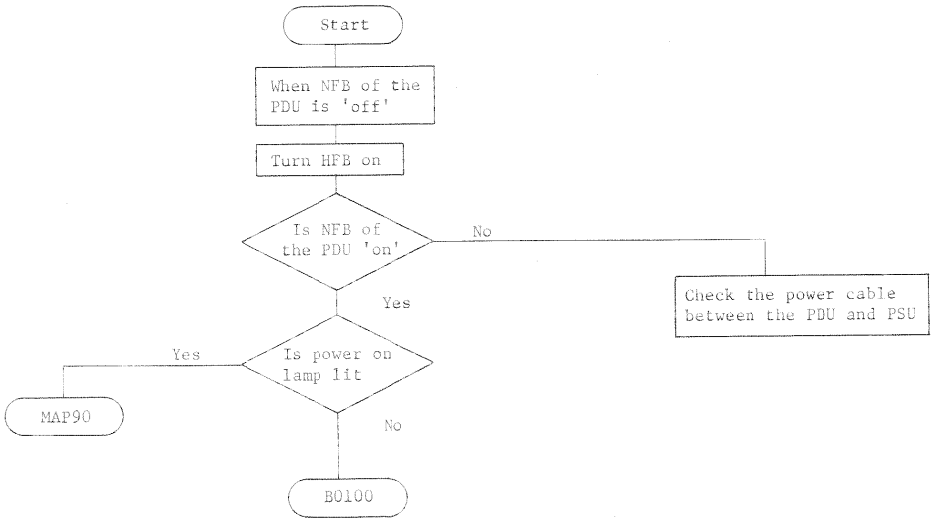
MTC POWER ALARM

B14L-5105-0057A refer to Fig. 1

	Appearance	Cause
1	NFB break	Short circuit of AC 200V input circuit.
2	F1 FUSE ALARM	Power Supply internal FAN, Gate FAN (200VF 1.3A)
3	F2 FUSE ALARM	Power Supply internal circuit (200VE 1.3A)
4	F3 FUSE ALARM	CHU A Interface circuit (+5V 7.5A)
5	F4 FUSE ALARM	CHU B Interface circuit (+5V 7.5A)
6	+5V ALARM LAMP	+5V Overvoltage or Undervoltage Thermal alarm for Tr. unit (80°C) Thermal alarm for a resistor against rush current (90°C) Fuse F1, F3 or F4 blown
7	-5.2V ALARM LAMP	-5.2V Overvoltage or Undervoltage
8	TH ALARM LAMP	Thermal alarm for external PC board gate

B14L-5105-0145A#A1 refer to Fig. 2

	Appearance	Cause
1	NFB break	Same as left
2	F1 Fuse	Same as left (200VF 1.3A)
3	F2 Fuse	Same as left (200VE 3A)
4	F3 Fuse	Same as left
5	F4 Fuse	Same as left
6	F5 Fuse	Power control (-24VE 1A)
7	POWER ALARM LAMP	+5V, -5.2V overvoltage or under voltage. Thermal alarm for PSU internal switch
8	FAN ALARM LAMP	Thermal alarm for external PC board gate



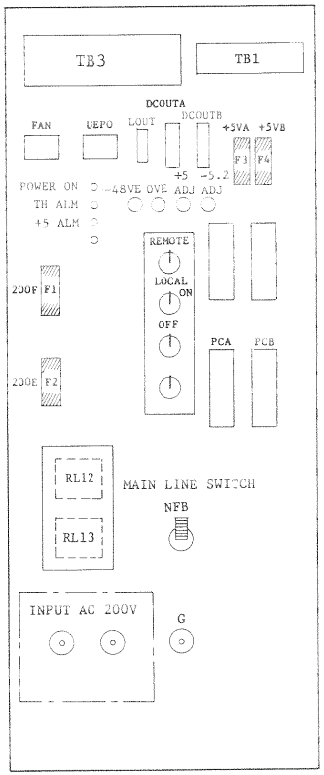


Fig. 1: MTC Power Supply B14L-5105-0057A

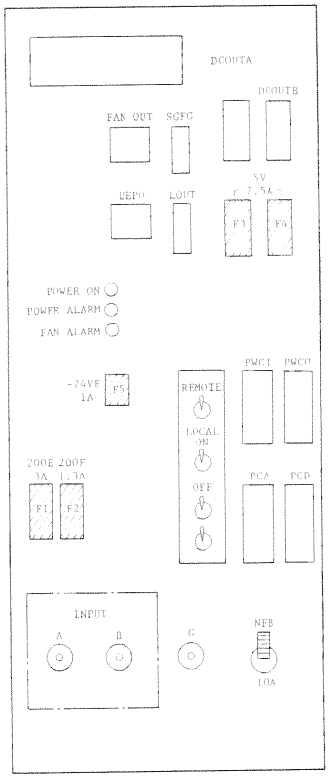
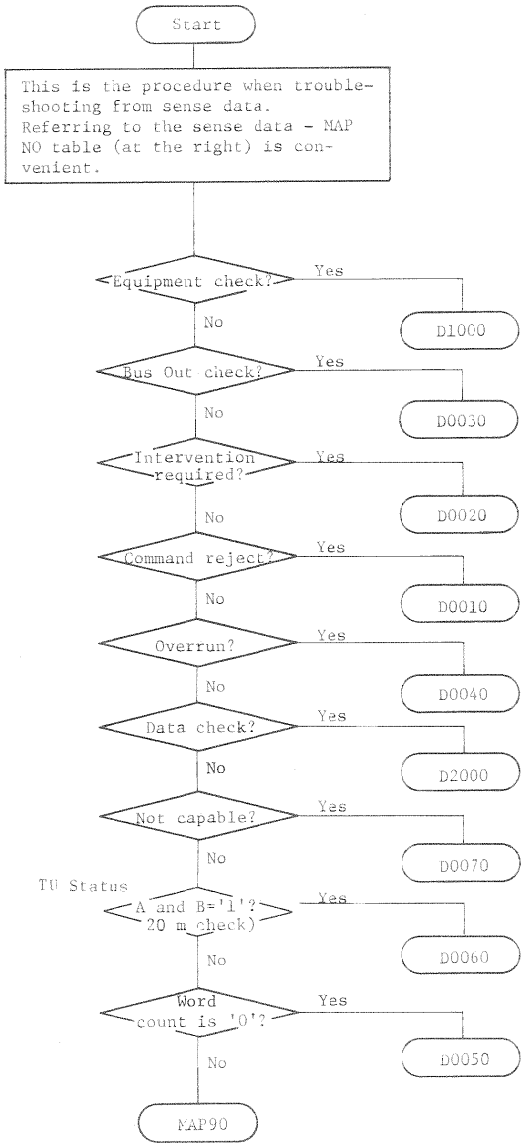


Fig. 2: MTC Power Supply B14L-5105-0145A#A1

D0001	Troubleshooting According to Sense Data



Bit / Byte	0	1	2	3	4	5	6	7
Byte 0	Command reject D0010	Intervention required D0020	Bus Out check D0030	Equipment check D1000	Data check D2000	Overrun D0040	Word count zero D0050	Data convert-er check '0'
1	Noise D2100	TU status A When both A and B are '1' D0060	TU status B	7 track '0'	Load point	Write status	File protect	Not capable D0070
2	Error track							
	0	1	2	3	4	5	6	7
3	VRC error D2001	Multiple track error D2001 LRC error D2001	Skew error D2001	End data check D2001 CRC error D2001	Envelope check D2001	1600 rpi	Backward	P compare D2110
4	MP hardware error D1010	Reject TU D1200	Tape indicate (EOT)	Write trigger VRC D2120		Loop write read	Tape unit check D1210	
5	New Subsystem '0'	New Subsystem '1'	Write tape mark error D1220	ID burst check D1230	Start read check D2002	Partial record D2002	Postamble error D2002	Error count overflow D2004
6	7 Track TU '0'	Write cirucit alarm A0330	Dual density	Not set 1600 rpi	6250 rpi tape unit	Tape unit model '1' '1' '0'	Tape unit model '0' '0' '1'	Tape unit model '1': 200 ips '0': 125 ips '1': 75 ips
7	Miscellane-ous error A0010	Tape loop alarm left A0310	Tape loop alarm right A0310	Reset key D1300	DSE	Fuse alarm A0100 A0110	Air bearing alarm A0310	Load failure A0100
8	IBG detected D1250	Error track P		Early begin read back check D1350	SASC check D1260	Slow begin read back check D1350	Slow end read back check D1350	Velocity retry D1330
9	1 or 2 track correction	Velocity change D1340	Channel buffer check D2110	CRC III error D2003	6250 rpi MTC	'1'	MTU reserve	MTC reserve
10	Status tag response check D1400	Command tag response check D1400	Control tag response check D1400	No block detected D1270	Dynamic reversal D1310	Tacho start failure D1320		Velocity check D1330
11	Read/write overrun D1450	Missing position D1460	Tag in check D1440	Register parity error D1010	MP detec-tion error D1010	ROM parity error D1010	MP trap D1205	TU ROM Parity error A0030
12	MTU inner status							
	Erase current ON	MTU action	Backward action	Write current ON	ARA 65% slice	High speed mode	1600 rpi mode	Tape mark detected

D0002	Sense Byte Table

Bit / Byte	0	1	2	3	4	5	6	7
Byte 0	Command reject (U)	Intervention (U)	Bus Out check (U)	Equipment check (U)	Data check (U)	overrun (U)	Word count zero (U)	Data converter check '0' (Not used)
1	Noise (E)(D)	TU status A	TU status B	7 track '0'	Load point (U)*	Write status	File protect	Not capable (U)
2	Error track							
	0	1	2	3	4	5	6	7
3	VRC error (D)	Multiple track error LRC error (D)	Skew error (D)	End data check (D)	Envelope check (D)	1600 rpi	Bachward	P compare (D)
4	MP hardware error (E)	Reject tape unit (E)	Tape indicate	Write trigger VRC (D)		Loop write to read	Tape unit check (E)**	
5	New subsystem '0'	New subsystem '1'	Write tape mark error (E)	ID burst check (U)	Start read check (D)	Partial record (D)	Post-amble error (D)	Error count overflow (D)
6	7 track TU '0'	Write circuit alarm (E)	Dual density	Not set 1600 rpi	6250 rpi Tape unit	Tape unit model 101: 200 ips MTU 100: 125 ips MTU 011: 75 ips MTU		
7	Miscellaneous error	Tape loop alarm left	Tape loop alarm right	Reset key	DSE	Fuse alarm	Air bearing alarm	Load failure
8	IBC detected	Error track P		Early begin read back check (D)	SAGC check (E)(D)	Slow begin read back check	Slow end read retry check (D)	Velocity
9	1 or 2 Track correction	Velocity change (D)	Channel buffer check (D)	CRCIII error (D)	6250 rpi MTC	'1'	MTU reserve	MTU reserve
10	Status tag response check (E)	Command tag response check (E)	Control tag response check (E)	No block detected (E)	Dynamic reserval (E)	Tacho start failure (E)		Velocity check (E)
11	Read/write overrun (E)	Missing position (E)	Tag in check (E)	Register parity error (E)	MP detection error (E)	ROM parity error (E)	MP Trup	TU ROM parity error

(U) sets "Unit Check".
(E) sets "Equipment Check".
(D) sets "Data Check.
(U)* becomes a cause of "Unit Check" while commands belonging to back category are being executed.
(E)** becomes a cause of "Equipment Check" except load failure.

Bit / Byte	0	1	2	3	4	5	6	7
12	Erase current ON	MTU action	Back-ward action	Write current ON	ARA 65% slice	High speed mode	1600 rpi mode	Tape mark detected
13	Error count							
14	MTC unique ID							
15	High speed feature	Skip file feature	Reserve	Reserve	TU unique ID (High order) K0010			
16	TU unique ID (Low order)							
17	2-channel switch	800 rpi option	16-drive option		MTC EC level K0006			
18	SAGC count TST6210				Model Conver-sion	TU EC level K0011		
19	TU7	TU6	TU5	TU4	TU3	TU2	TU1	TU0
20	Primed for DEVICE END							
21	MTU error code A0010, D3000, D3010							
22	Field replaceable unit (FRU-1)							
23	Field replaceable unit (FRU-2)							

D0010	Command Reject

Generated in the following cases:

(1) Invalid command has been given.
(Command with command byte bits 5, 6, 7 defined as 011 is handled the same as NO OPERATION.)
FRU1 (Sense byte 22) 01
FRU2 (Sense byte 23) ..... Rejected command code

(2) Sense & controller reserve, sense & controller release command has been given to an MTC not having the 2CH switch function. Otherwise, sense & tape unit reserve, sense & tape unit release, unconditional reserve, sense IO type command has been given to an MTC in "I-compatible" mode.
FRU1 (Sense byte 22) 02
FRU2 (Sense byte 23) ..... Rejected command code

(3) DATA SECURITY ERASE command (DSE) has been given without chaining with ERASE command.
FRU1 (Sense byte 22) 03
RFU2 (Sense byte 23) ..... Last command code
(command code before DSE command)

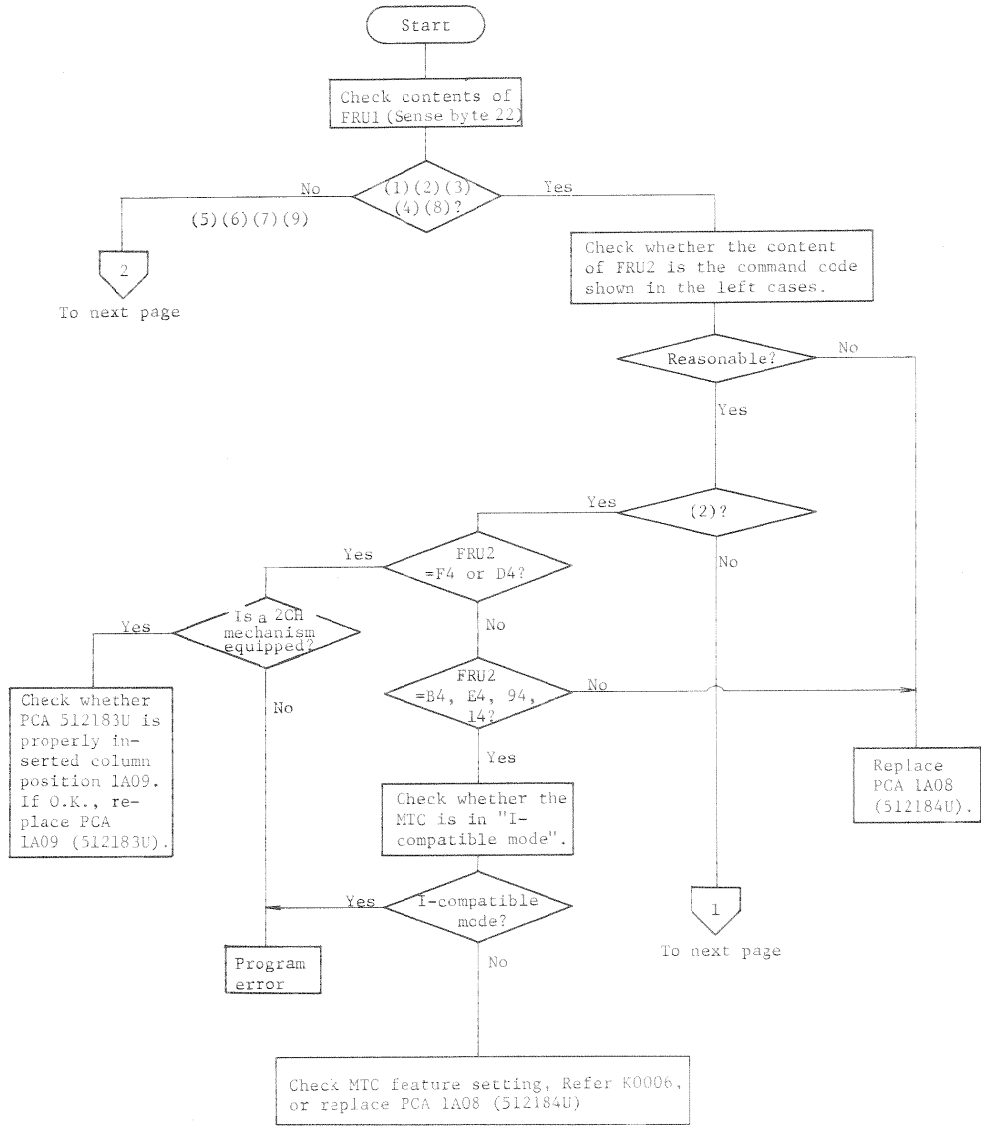
(4) A write tape mark command, a erase command or a write command has been given to a file protected MTU.
FRU1 (Sense byte 22) 04
FRU2 (Sense byte 23) ..... Rejected command code

(5) CAPSTAN TRANSFER WRITE, TIME-SENSE TRANSFER WRITE, ERASE TRANSFER operation has been given to a file protected MTU.
FRU1 (Sense byte 22) 05
FRU2 (Sense byte 23) ..... Rejected transfer code

(6) Diagnostic transfer operation has been given to a MTU detecting BOT/EOT.
FRU1 (Sense byte 22) 06
FRU2 (Sense byte 23) ..... Rejected transfer code

(7) Invalid diagnostic transfer code has been given.
FRU1 (Sense byte 22) 07
FRU2 (Sense byte 23) ..... Rejected transfer code

(Continue)



D0011	Command Reject (continued)

(8) Sense & controller reserve, sense & controller release, sense & tape unit reserve, sense & tape unit release, unconditional reserve has been given as a command other than the first command of the chain sequence.

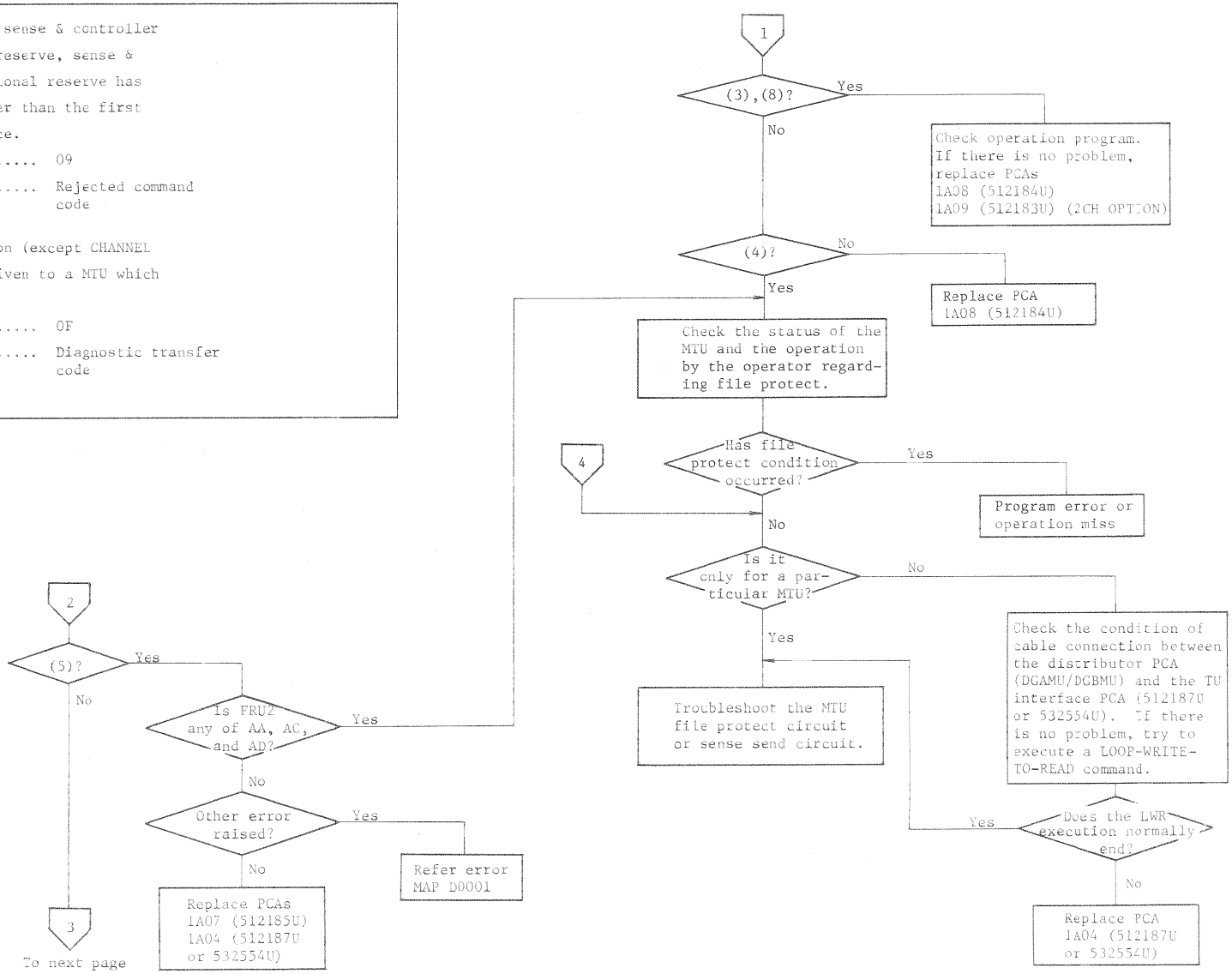
FRU1 (Sense byte 22) 09

FRU2 (Sense byte 23) ..... Rejected command code

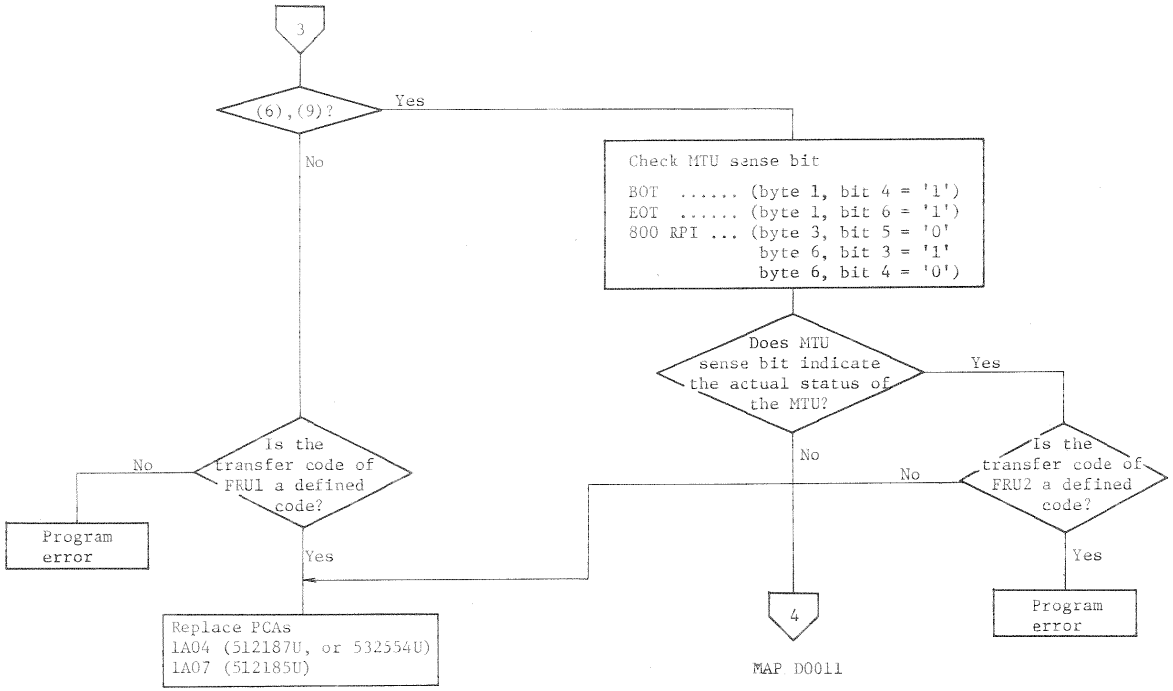
(9) Diagnostic transfer operation (except CHANNEL BUFFER TRANSFER) has been given to a MTU which is in 800 BPI mode.

FRU1 (Sense byte 22) 0F

FRU2 (Sense byte 23) ..... Diagnostic transfer code



D0012	Command Reject (continued)



D0020	Intervention Required

Intervention Required

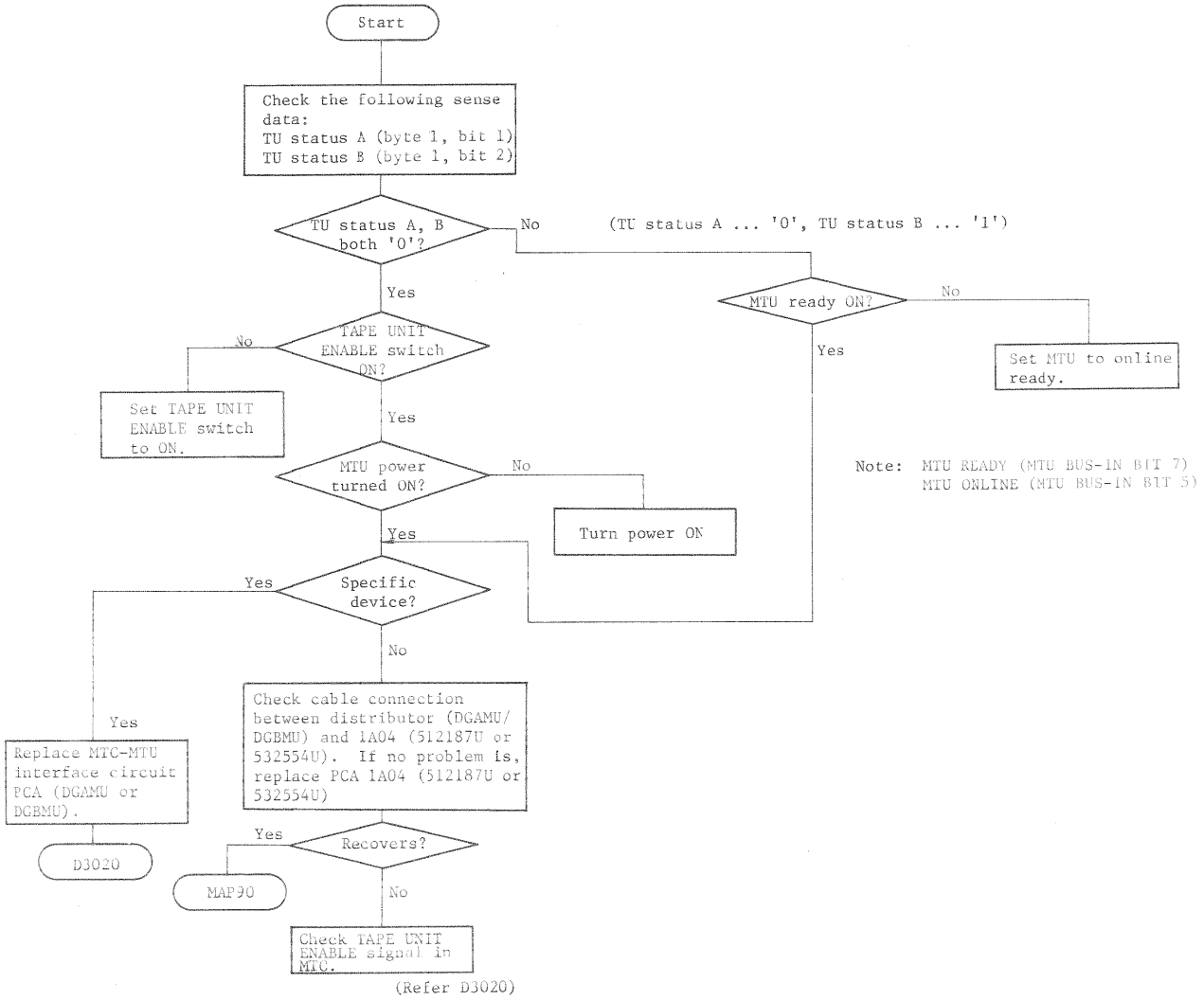
Generated in the following cases,

(1) When MTC operator panel TAPE UNIT ENABLE switch is OFF (DISABLE).

(2) Unpowered MTU specified.

(3) OFFLINE state MTU specified.

(4) MTU placed in OFFLINE status during operation execution.



D0030	Bus Out Check

Generated in the following cases.

(1) Parity error

in a command or data byte received from channel.

FRU1 (Sense byte 22) ... B0

FRU2 (Sense byte 23) ... Content of IFSTA register

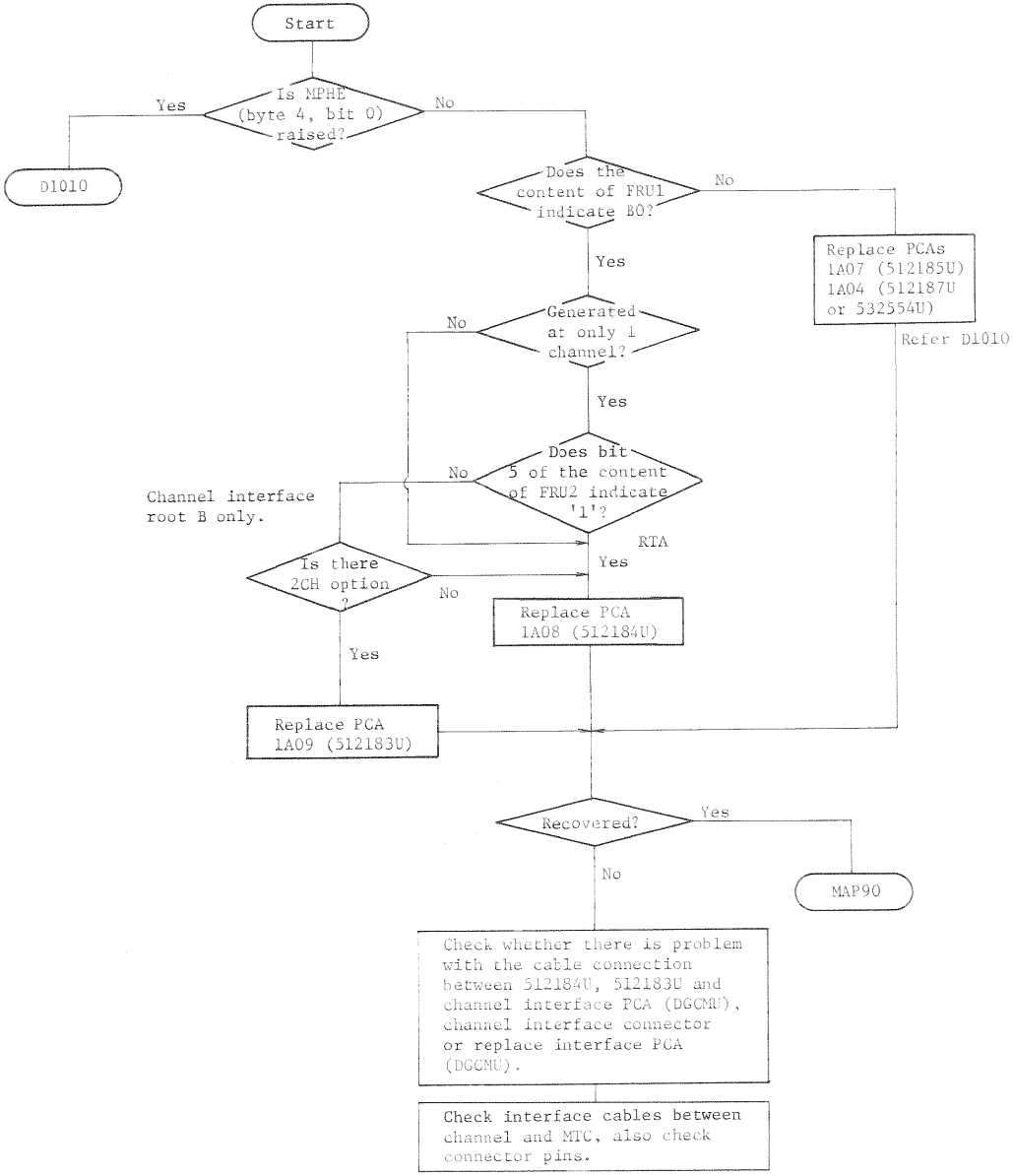
	0	1	2	3	4	5	6	7
IFSTA register						RTA	RTB	

(2) Control unit has detected a temporary hardware error.

In this case;

MP hardware error (byte 4, bit 0) is set, and

also FRU1, FRU2 give more detail information. See D1010.



D0040	Overrun

Overrun

Generated when channel did not respond to data service request within the prescribed time at a write, LWR, read, read backward command.

Note: Overrun is not posed when data check is '1'.

FRU1, FRU2 give more detailed information;

(1) FRU1 (Sense byte 22) ... 20
FRU2 (Sense byte 23) ... The content of IFCTL register

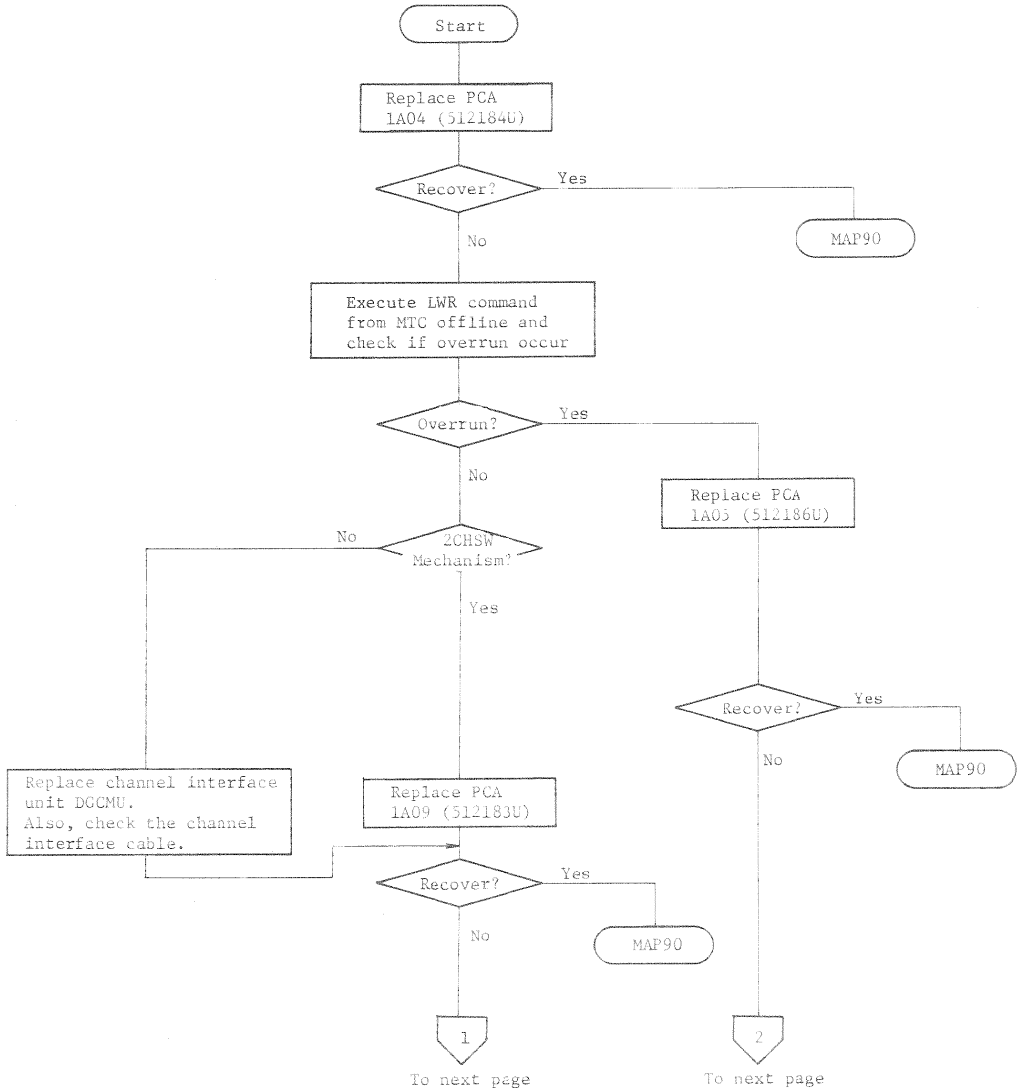
In the WRITE or LWR command, when the amount of the data in a channel data buffer becomes less 6 bytes in case of 6250 RPI mode or zero byte in case of 1600/1800 RPI mode, the data writing ends, and control moves to writing of postamble.
this error is generated;

1) The case when it is detected that channel data buffer does not become empty at the time when all the write operations end. 2) Failure in the data transfer sequence control circuit or the channel buffer circuit.
3) In the read or read backward command, the case when the channel buffer does not become empty even after reading of all the data is completed and further a certain time passes.

(2) FRU1 (Sense byte 22) ... 21
FRU2 (Sense byte 23) ... The content of IFCTL register

In the WRITE or LWR command, the case when the channel buffer becomes the empty state in which there is no data in the channel buffer (less than 6 bytes in case of 6250 RPI mode) before receiving a message of indicating data ending from the channel during writing data.

In the READ or READ BACKWARD command, the case when the channel buffer becomes full during reading data.



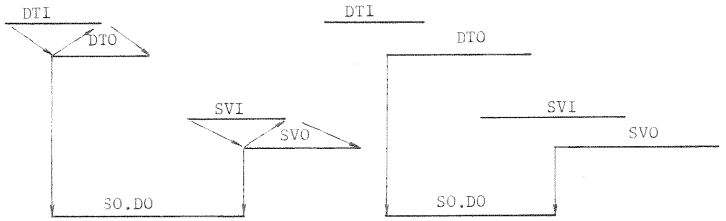
D0041	Overrun (continued)

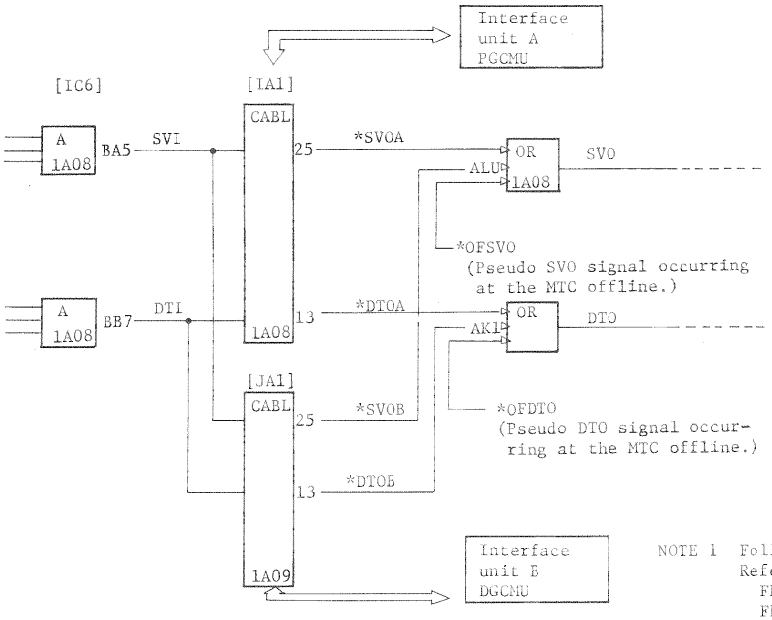
Maximum cable length

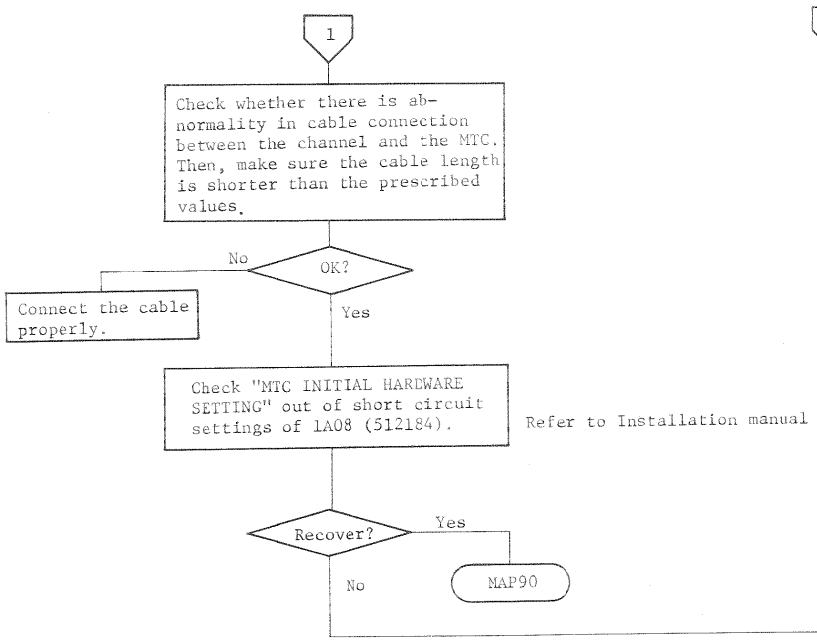
36 m (118 ft) for 200 IPS operation mode

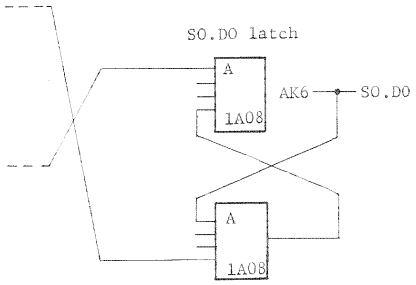
61 m (200 ft) for 125/75 IPS operation mode

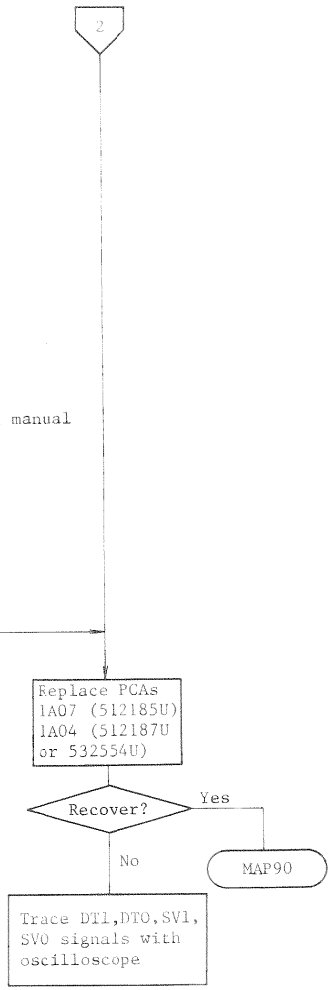
When Channel Interface Cable Extension Feature (Offset Interlock mode) is selected, maximum length may be increased. (80m (267 Ft))
See NOTE 1 in this case.











NOTE 1 Following FRU code may be posted when Offset-Interlock mode.
Refer FRU code table for detail explanation.
FRU1 .... '22'
FRU2 .... contents of IFCTL register

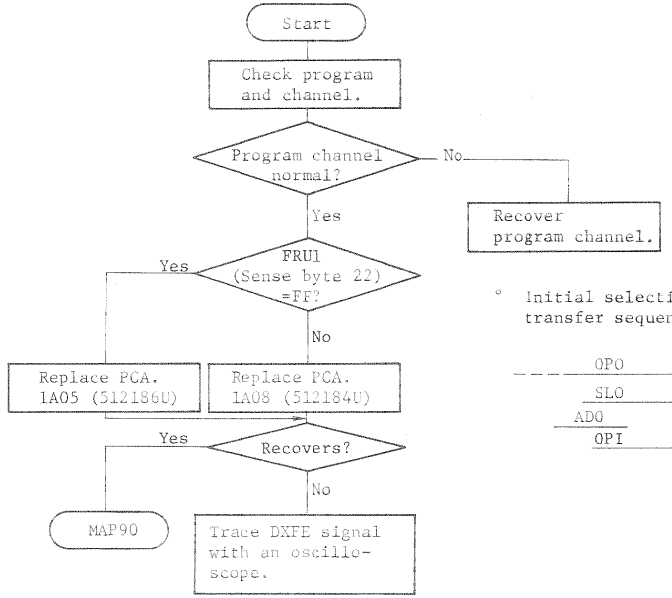
D0050	Word Count Zero

Word Count Zero

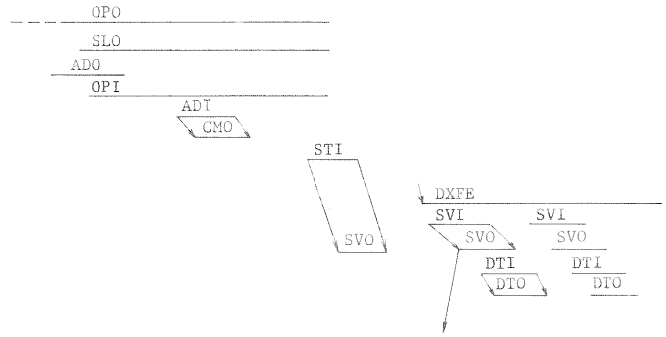
Generated when data transfer halt command received before first data received at write command.

(1) When data byte count is '0'.

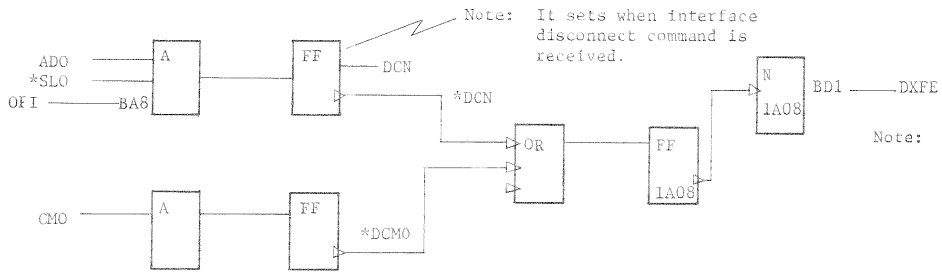
(2) When interface disconnect specified by halt I/O.



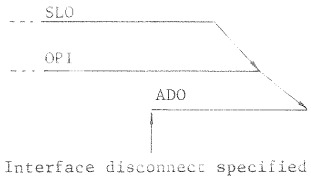
° Initial selection and data transfer sequence.



Word count zero occurs when DXFE signal becomes '1' before SVO response to initial SVI.



Note: Interface disconnect time chart

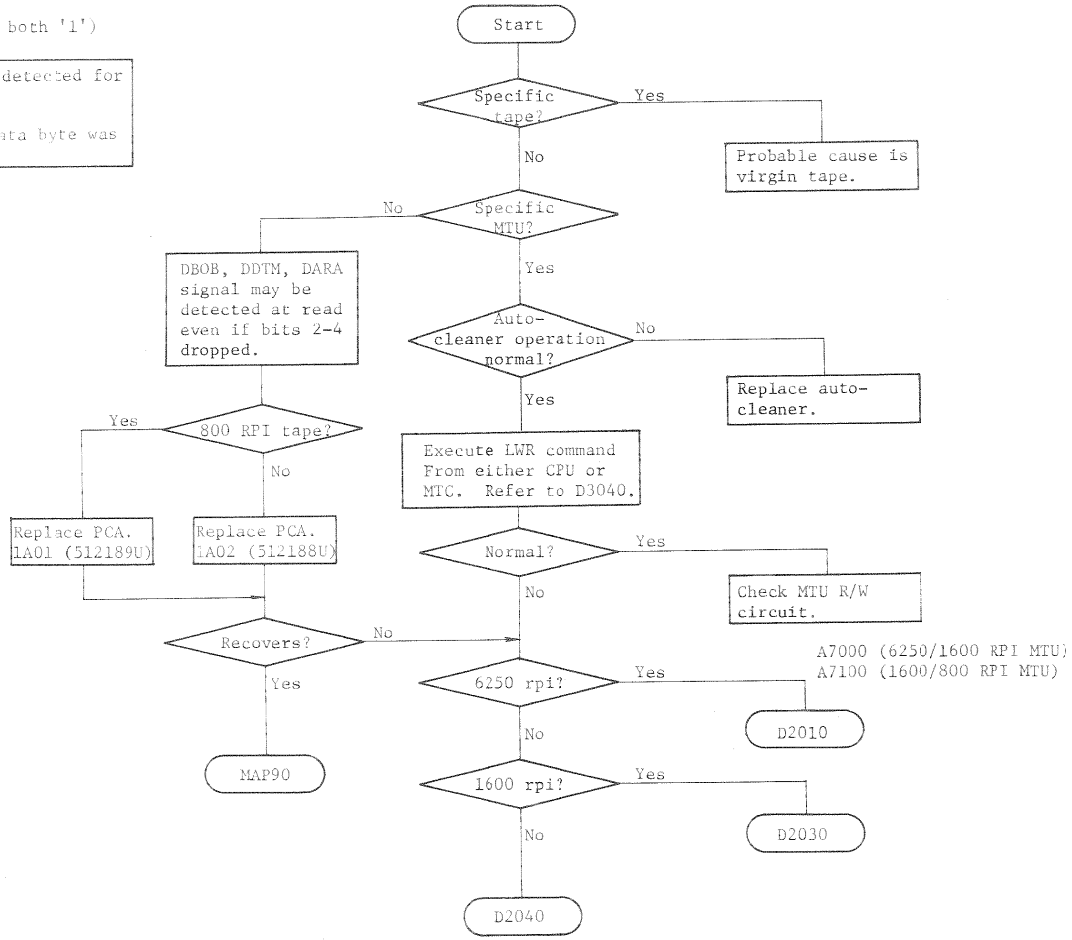


D0060	20 m Check (When TU status A, B both '1')

20 m Check (When TU status A, B both '1')

Generated when any data was not detected for more than 20 m at read command.

(Any of BOB, DTM, ARA, or NRZ data byte was not detected.)



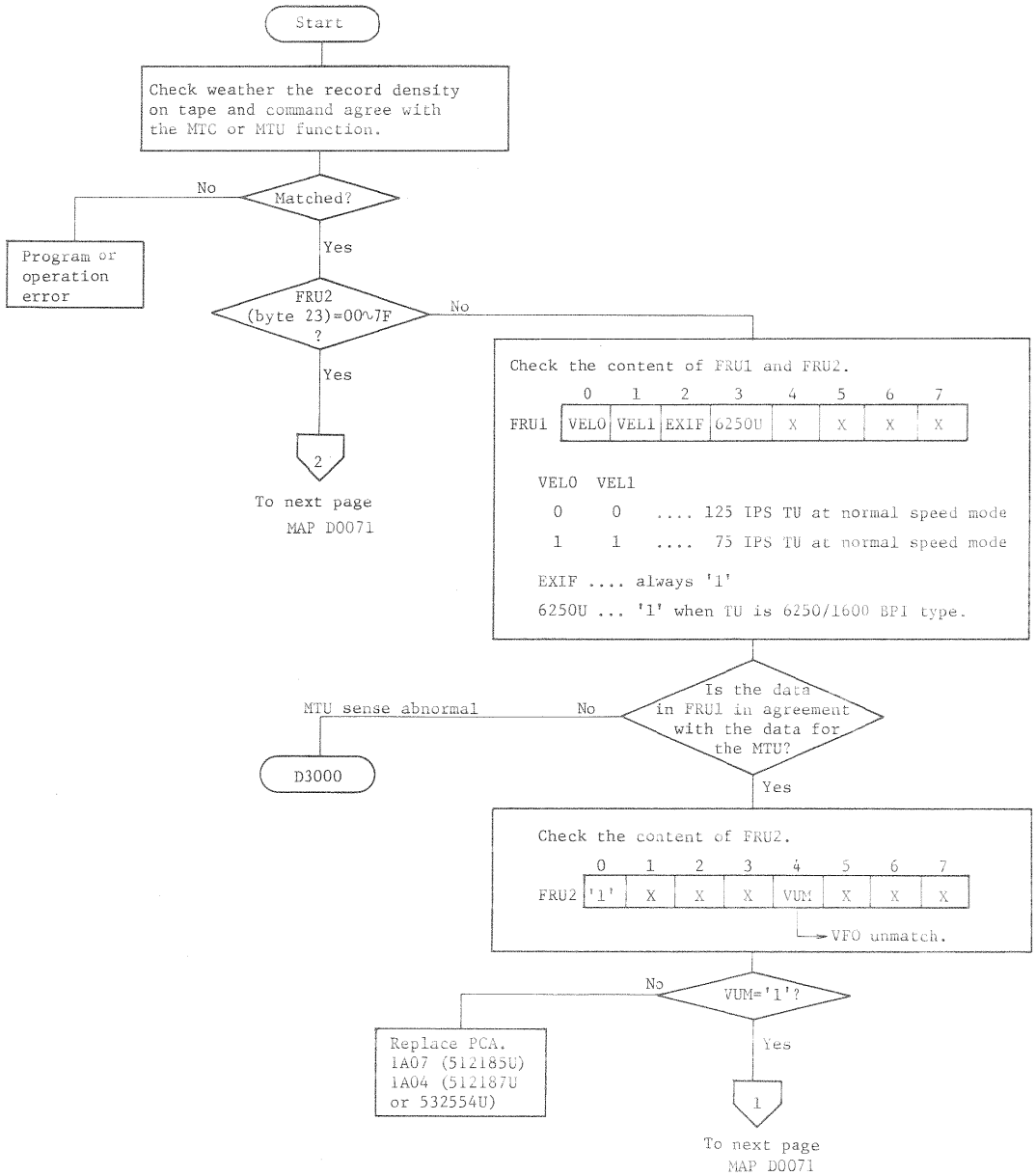
D0070	Not Capable-1

Not capable is generated;

(1) If an attempt is made to read 800 BPI tape through the MTC or MTU without 800 BPI feature or function.

(2) If an attempt is made to read 6250 BPI tape with the MTU without 6250 BPI function.

(3) If the specification for the maximum possible processing speed of the demodulation circuit is not in agreement with that for the speed of the MTU. (In this case, FRU2 = 80 ∿ FF).



D0071	Not capable-2

From D0070

2

Check whether the MTU sense bits in the sense byte is correct.

6250 TU (byte 6, bit 4)
800 OPTION (byte 17, bit 1)

Are the MTU sense bits correct?

No → MTU sense abnormal → D3000

Yes

ID Burst read error

CHECK AUTO CLEANER

Normal?

No → Replace the auto cleaner

Yes → Try to execute a LWR command.

Has the execution normally ended?

Yes → Check the R/W circuit of MTU. Check the condition around the head.

No

Is the abnormal ending of LWR for a particular device?

Yes → Check the R/W circuit of MTU. Check the condition around the head.

No

Replace PCA. 1A02 (512188U)

Recover?

Yes → MAP90

No

Replace PCA. 1A03 (550087U/550088U)

Recover?

Yes

No

Check the cable connection between the distributor and the TU interface PCA (512187U or 532554U). If there is no problem, make an attempt to execute various commands in the MTC offline mode to analyze them by another sense bit.

From D0070

1

Check VFOH/M/L bit of FRU2.

	0	1	2	3	4	5	6	7
FRU1	VEL0	VEL1	DX1F	6250U	X	VFOH	VFOM	VFOL

Allowable processing speed of VFO

VFOH ... 200 IPS
VFOM ... 125 IPS
VFOL ... 75 IPS

Is the correspondence correct between PCB of 1A03 and VFOH/M/L?

Yes

	VFOH	M	L
550087U ..	0	1	1
550088U ..	1	1	0

No

Replace PCA 1A03 (550087U) or 550088U)

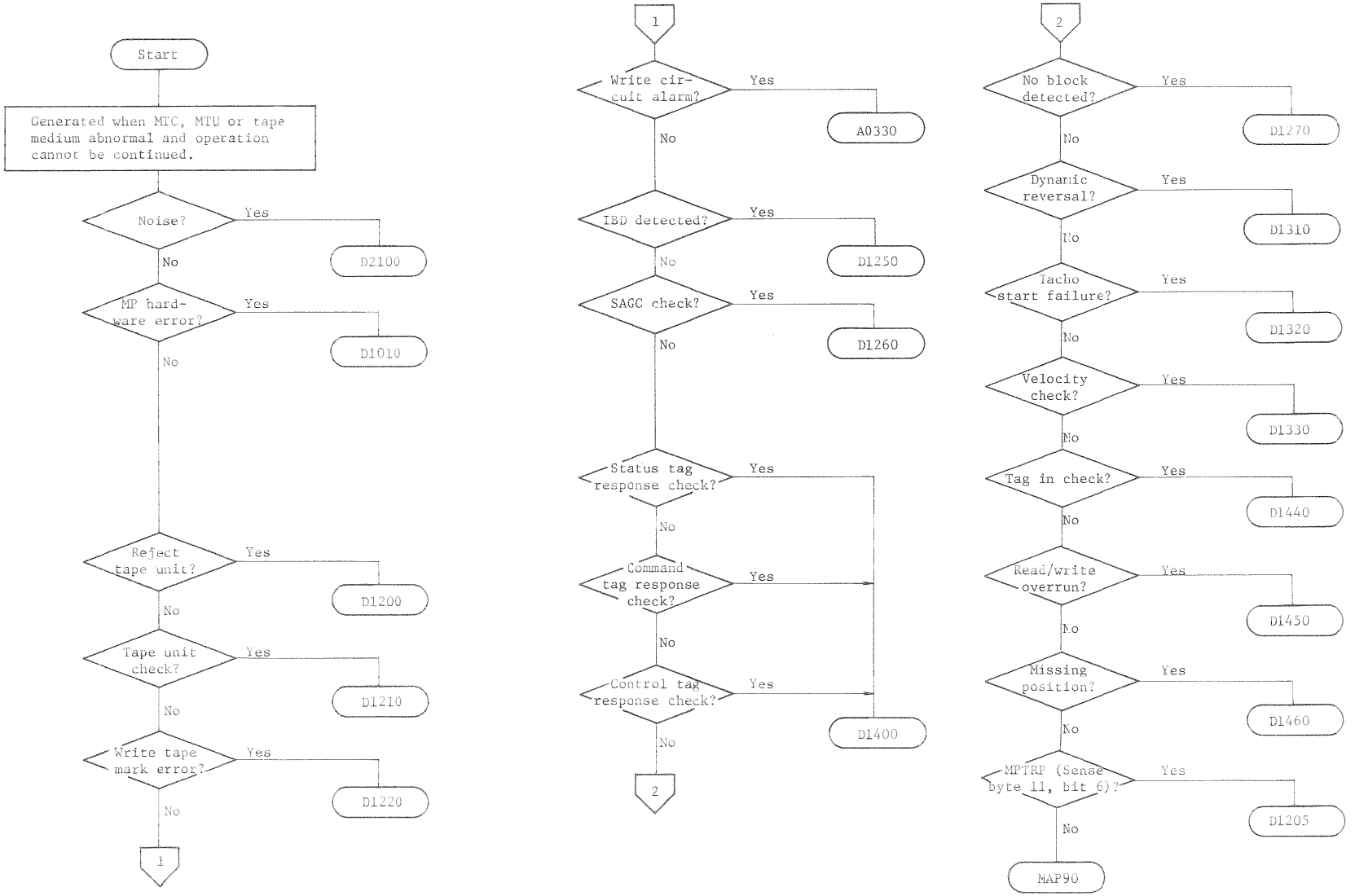
Is the speed of the MTU in agreement with the possible processing speed of PCA of 1A03 (VFO)?

No → Make sure the installation has been completed.

Yes

Replace PCA. 1A 08 (512184U)

D1000	Equipment Check



D1010	MP Hardware Error

ROM parity error
Register parity error
MP detect error

MPHE (Sense byte 4, bit 0) is generated in following cases:

(1) When parity error of MTC's microprogram control storage occurs

In this case, bit 5 of sense byte 11 (MTC ROM parity error) is set.

(2) When parity error of MTC's local storage (register) occurs

In this case, bit 3 of sense byte 11 (register parity error) is set.

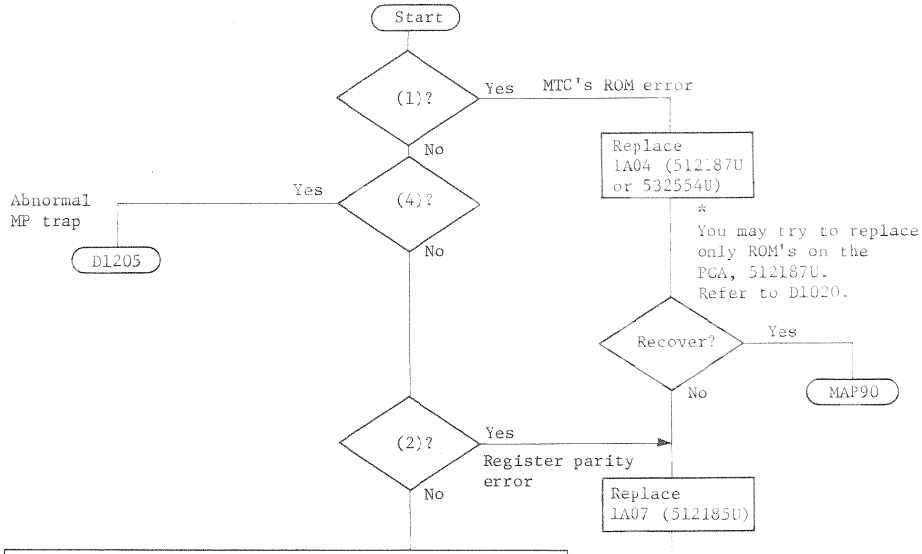
(3) When an error is detected during the idle diagnosing or in the TEST MTC (MPDE-Sense byte 11, bit 4 is set), an error is detected during the power-on-diagnosing and the disconnect-in-sequence has been executed for channel during the preceding operation.

Note: The case where the MPHE is accompanied by BOC

Error must have actually occurred during the operation immediately preceding the operation and the disconnect-in-sequence must have occurred. Namely, the ICC (Interface Control Check) takes place in the channel. The BOC which is accompanied by the above MPHE responds to the command first appearing after the selective reset is carried out. The above three cases point out the cause of ICC and they can be considered temporary hardware failures. The command execution answered by the BOC is retried in accordance with the usual error recovery procedure.

(4) When an unknown trap occurs

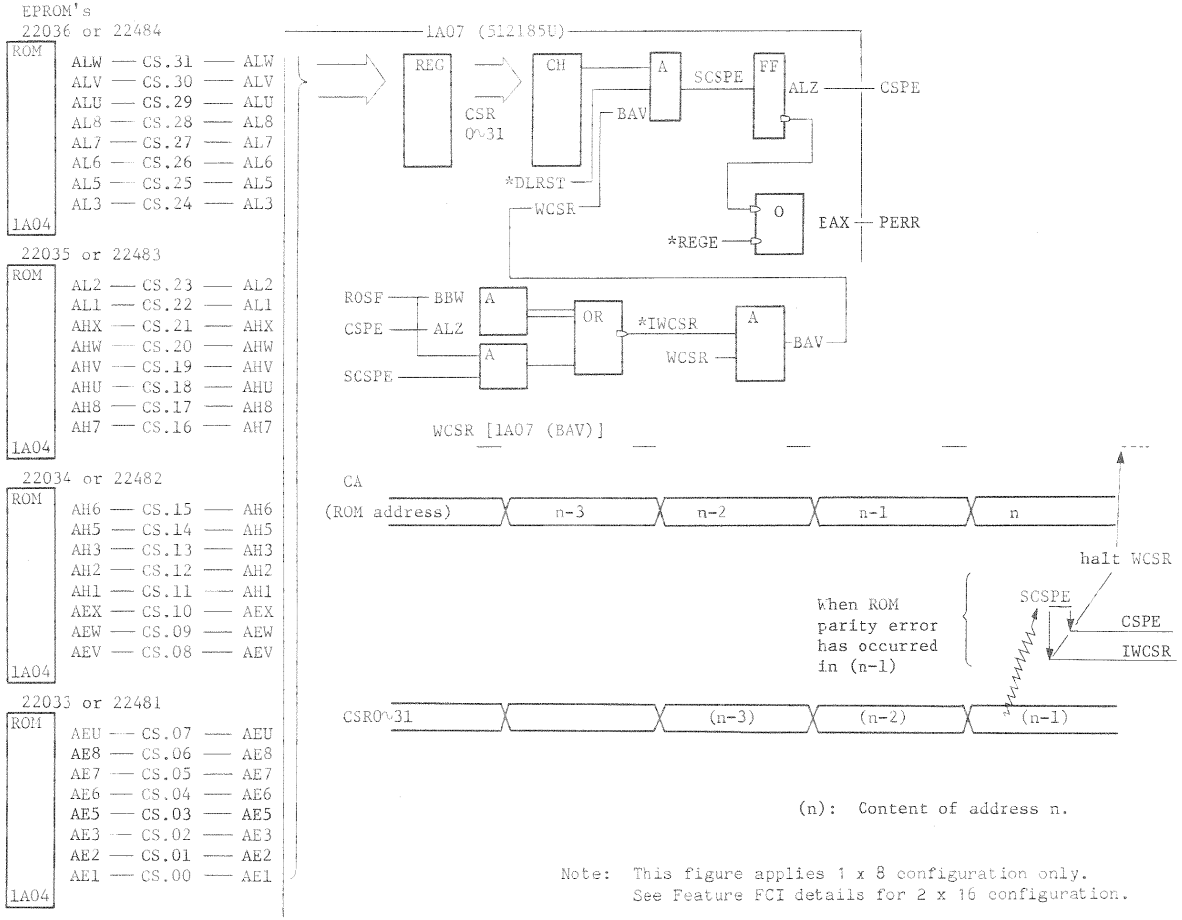
FRU1 (Sense byte 22) = 78



The content of FRU1 (Sense byte 22) is checked and the PCBs shown below corresponding to individual codes are replaced.

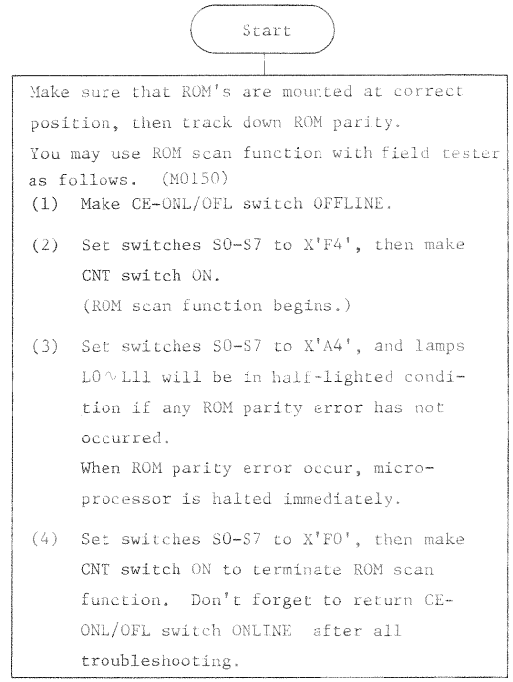
40 ∿ 47	[1A04 (512187U or 532554U)]
48 ∿ 4F	[1A05 (512186U)]
54 ∿ 57	[1A01 (512189U)]
58 ∿ 5F	[1A08 (512184U)]
70 ∿ 77	[1A04 (512187U or 532554U)]
79 ∿ 7F	[1A05 (512186U)]
80 ∿ 87	[1A01 (512189U)]
88 ∿ 8F	[1A08 (512184U)]
98, 99	[1A05 (512186U)]
D0 ∿ D8	[1A04 (512187U or 532554U)]
DA	[1A05 (512186U)]
DB	[1A02 (512188U)]
F1,F2,F8,F9,FE	[1A07 (512185U)]
F7	[1A04 (512187U or 532554U)]
FB, FC	[1A08 (512184U)]
Others	[1A07 (512185U), 1A04 (512187U or 532554U)]

D1011	ROM Parity Error



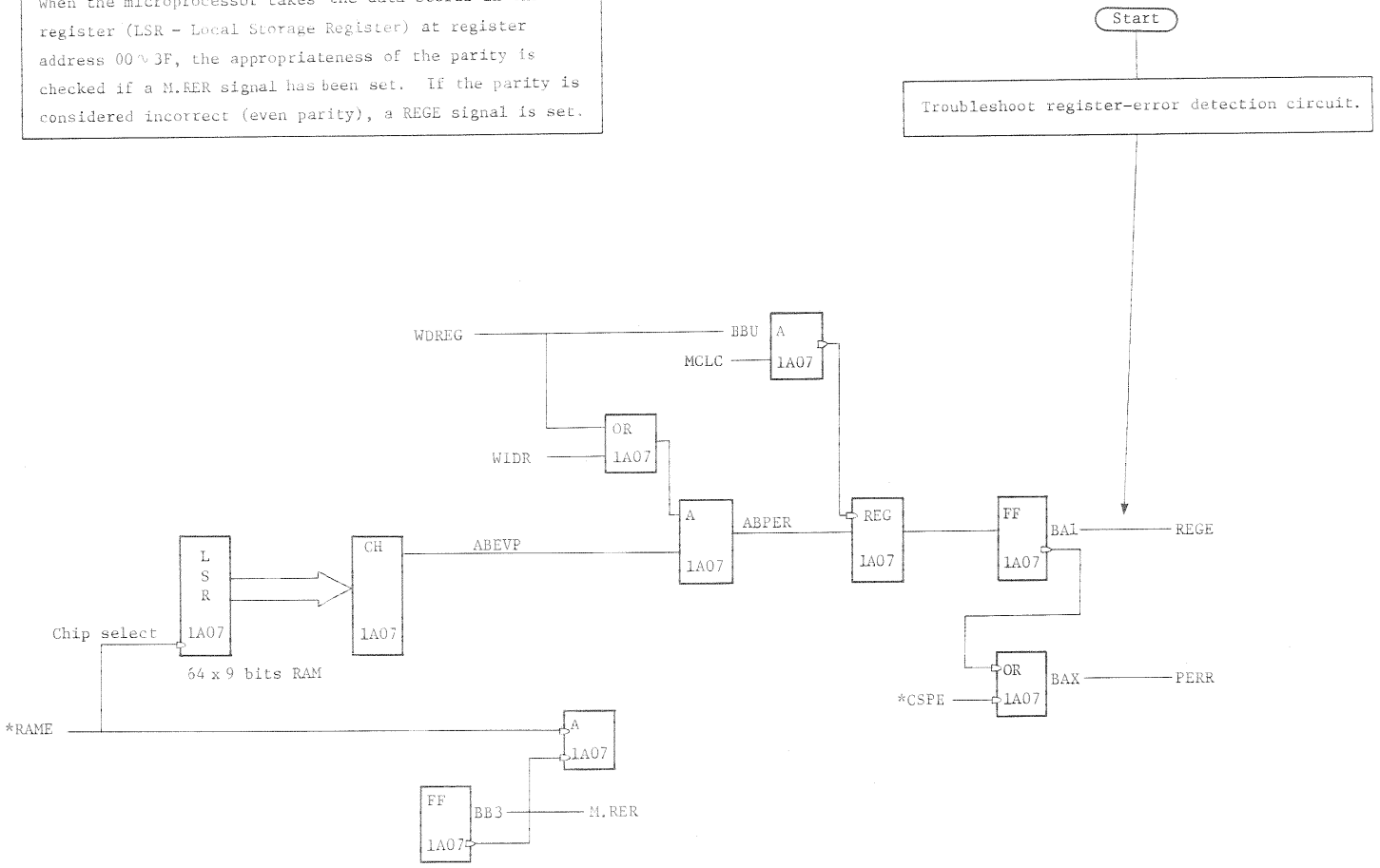
(n): Content of address n.

Note: This figure applies 1 x 8 configuration only.
See Feature FCI details for 2 x 16 configuration.



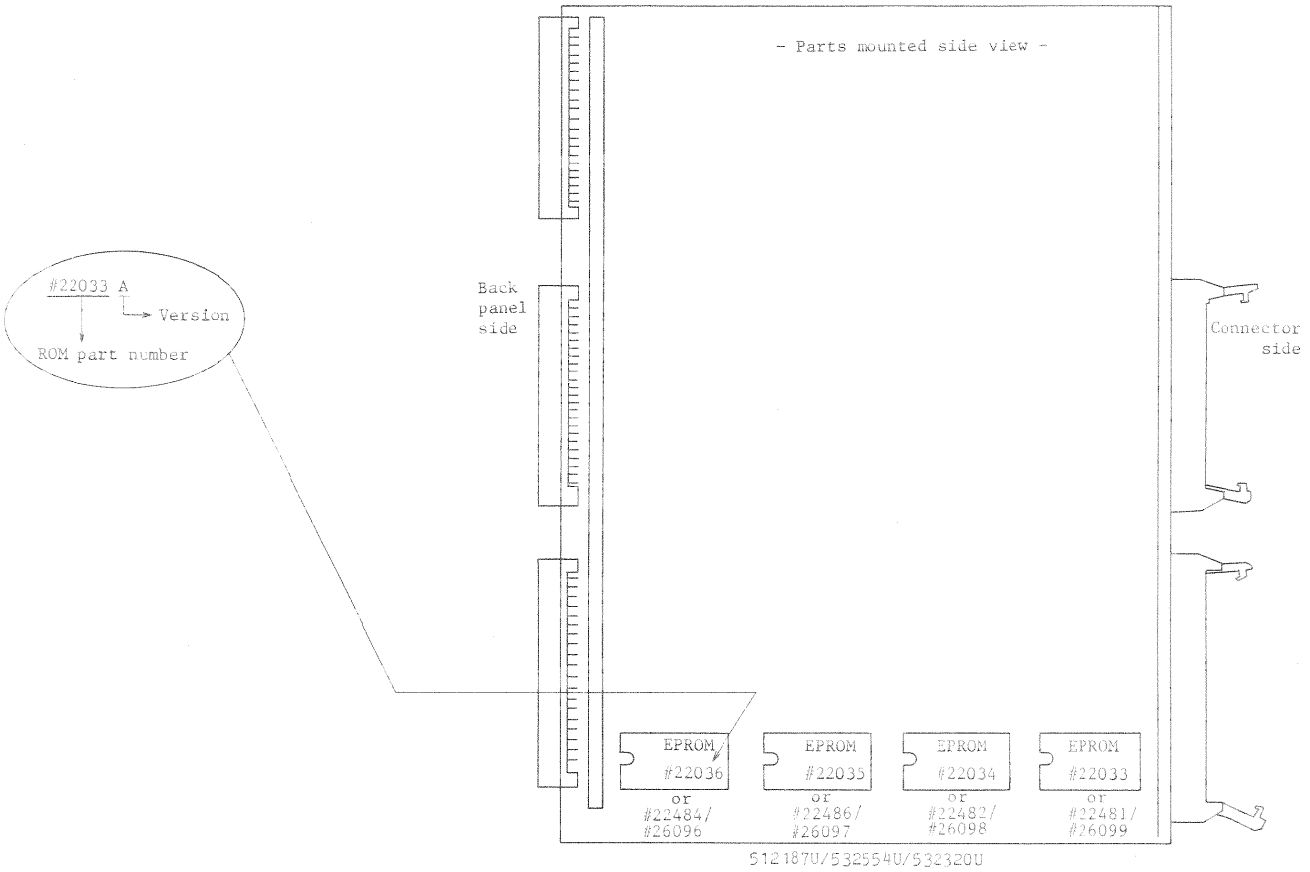
D1012	Register Parity Error

When the microprocessor takes the data stored in the register (LSR - Local Storage Register) at register address 00∿3F, the appropriateness of the parity is checked if a M.RER signal has been set. If the parity is considered incorrect (even parity), a REGE signal is set.



D1020	ROM Mounting Position

1. Compare each ROM part number with following figure.



D1200	Reject Tape Unit

Reject Tape Unit

Generated in the following cases:

(1) When capstan tacho pulse stopped during drive. .... Tacho start failure
FRU1 (Sense byte 22) = 74
TCSF (Sense byte 10, bit 5) = ON

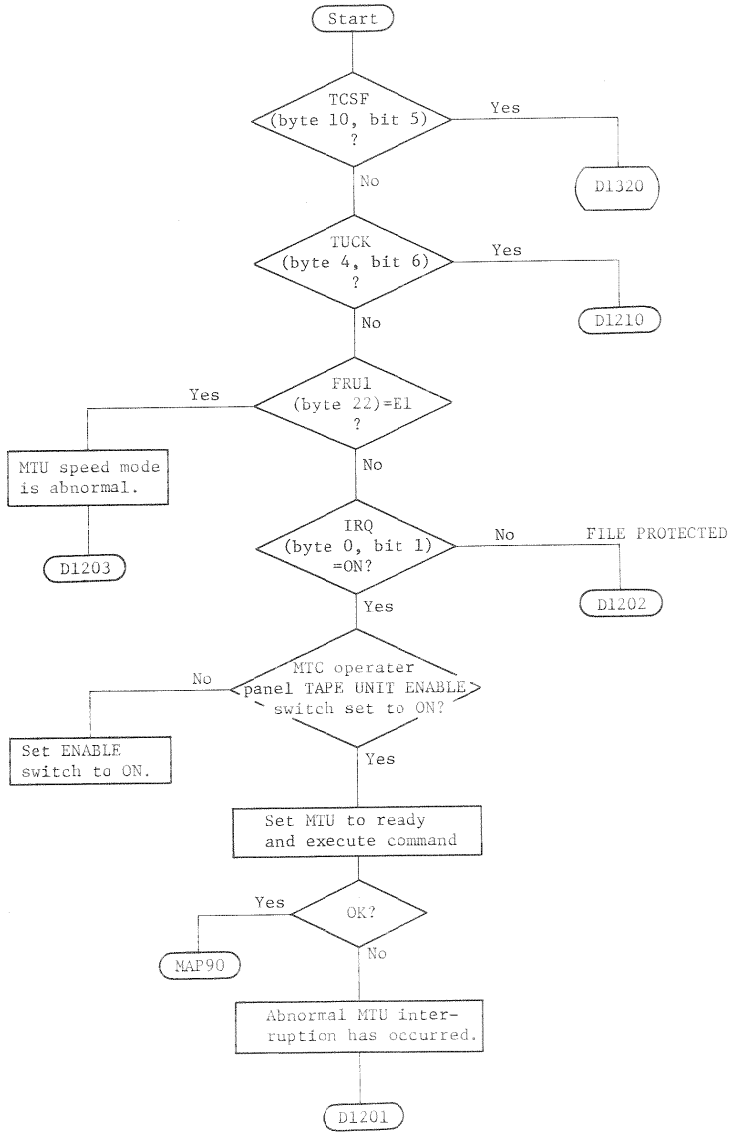
(2) When MTU has become abnormal condition while MTU connected to MTC and

1) TUCK (tape unit check) has occurred during operation.
FRU1 (Sense byte 22) = 70
FRU2 (Sense byte 23) = Tape unit sense byte 0
TUCK (Sense byte 4, bit 6) = ON

2) MTU has become 'not ready' or 'not online' condition.
FRU1 (Sense byte 22) = 70
FRU2 (Sense byte 23) = Tape unit sense byte 0
IRQ (Sense byte 0, bit 1) = ON

3) MTU has become 'file protected' condition during write, write tape mark, erase operation.
FRU1 (Sense byte 22) = 70
FRU2 (Sense byte 23) = Tape unit sense byte 0
FP (Sense byte 1, bit 6) = ON

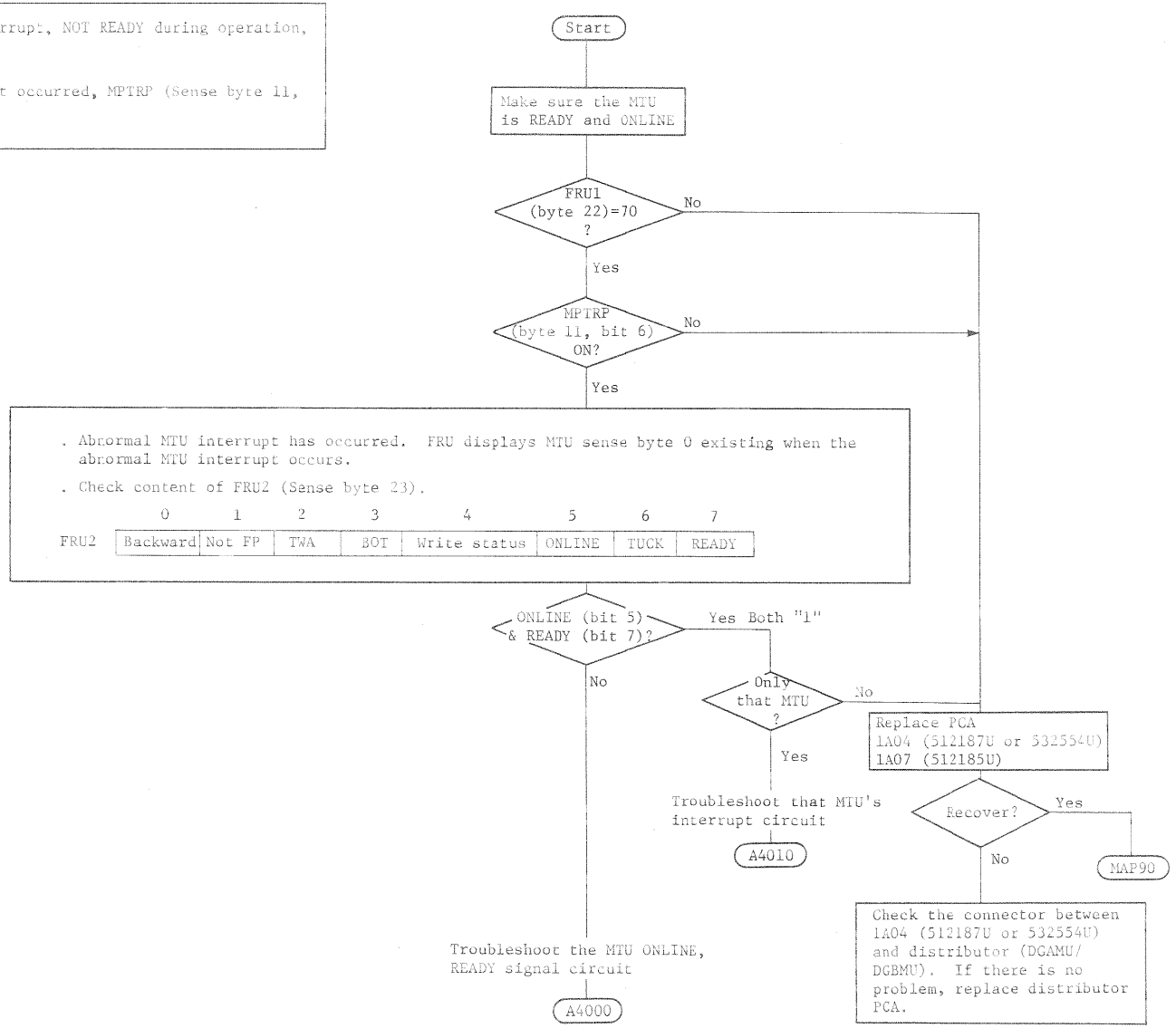
4) MTU, in 800 BPI mode and not at BOT, has become 'high speed' mode.
FRU1 (Sense byte 22) = E1



D1201	Abnormal MTU Interruption - 1

Abnormal MTU interrupt, NOT READY during operation, is suspected.

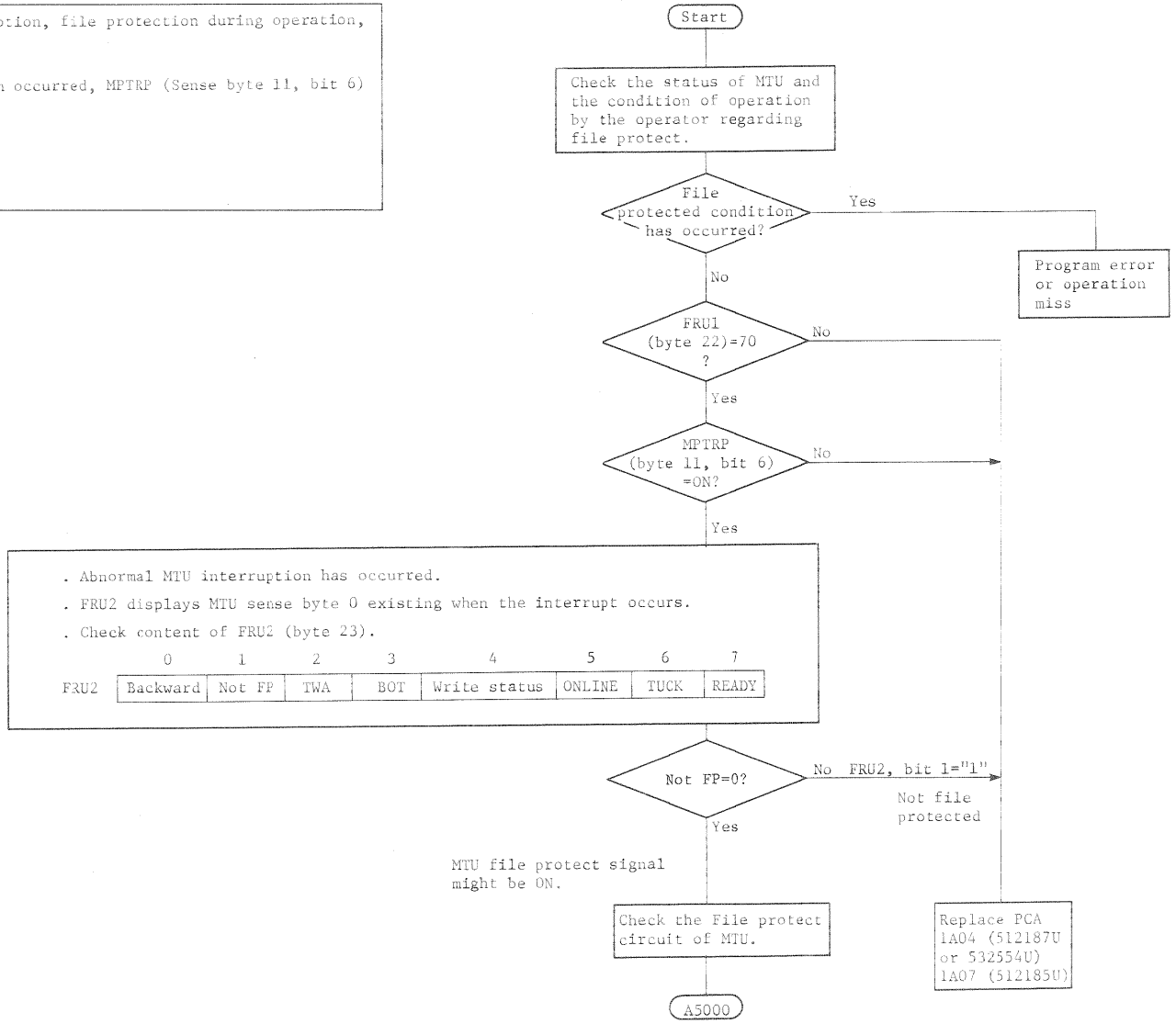
When MTU interrupt occurred, MPTRP (Sense byte 11, bit 6) was set.



D1202	Abnormal MTU Interruption - 2

Abnormal MTU interruption, file protection during operation, is suspected.

When MTU interruption occurred, MPTRP (Sense byte 11, bit 6) was set.

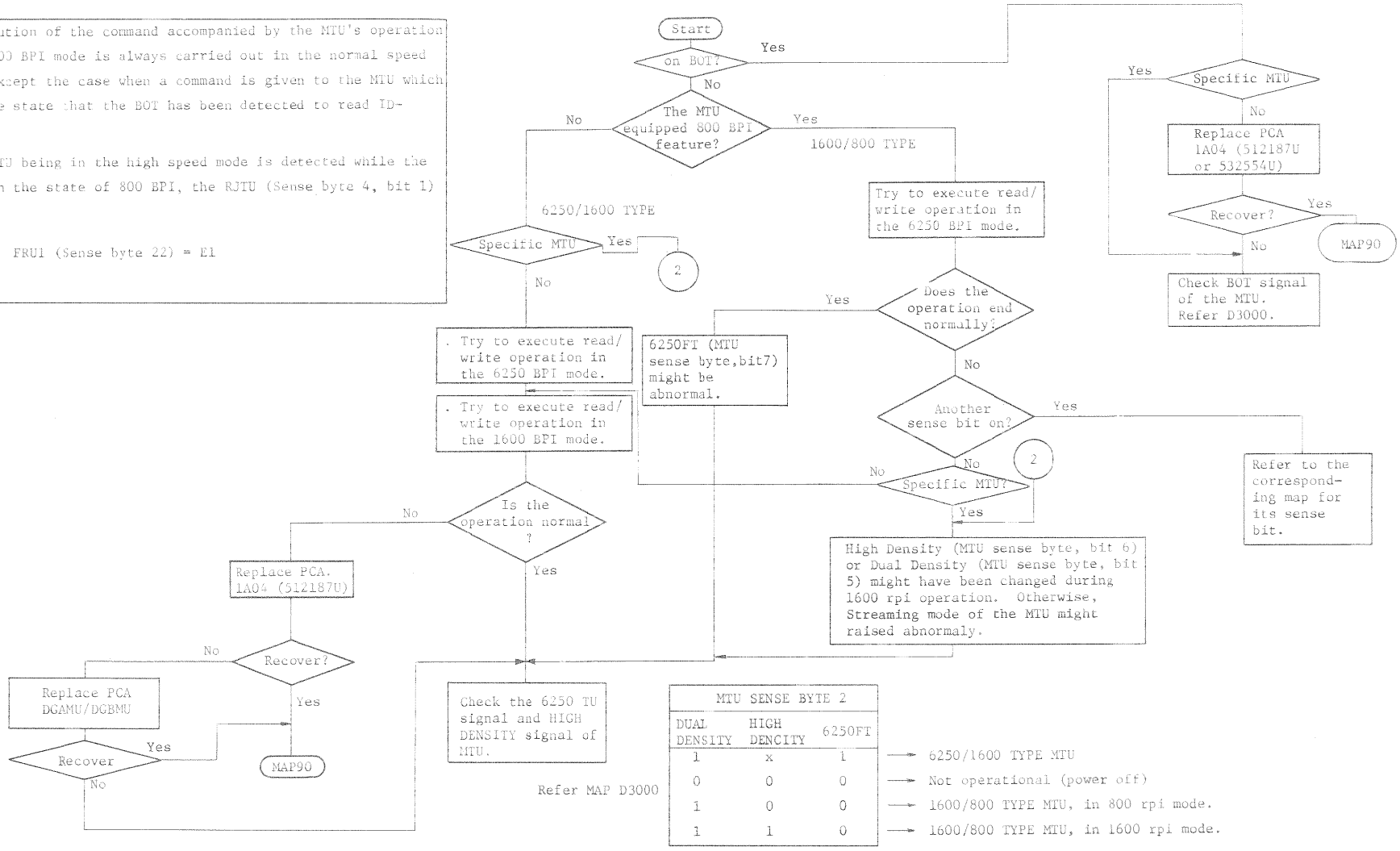


D1203	Abnormal Speed Mode

The execution of the command accompanied by the MTU's operation in the 800 BPI mode is always carried out in the normal speed mode, (except the case when a command is given to the MTU which is in the state that the BOT has been detected to read ID-burst).

When a MTU being in the high speed mode is detected while the MTU is in the state of 800 BPI, the RJTU (Sense byte 4, bit 1) is set.

FRU1 (Sense byte 22) = E1



MTU SENSE BYTE 2			
DUAL DENSITY	HIGH DENCITY	6250FT	
1	x	1	→ 6250/1600 TYPE MTU
0	0	0	→ Not operational (power off)
1	0	0	→ 1600/800 TYPE MTU, in 800 rpi mode.
1	1	0	→ 1600/800 TYPE MTU, in 1600 rpi mode.

D1205	MP Trap

. MPTRP (Sense byte 11, bit 6) is set when a trap occurs in the MTC microprocessor due to any cause other than the start of the initial-selection-sequence from the channel. When the cause of the trap is not made clear, an equipment check (EQC) error is posted.

(1) When the microprocessor receives an unknown MTU interrupt.

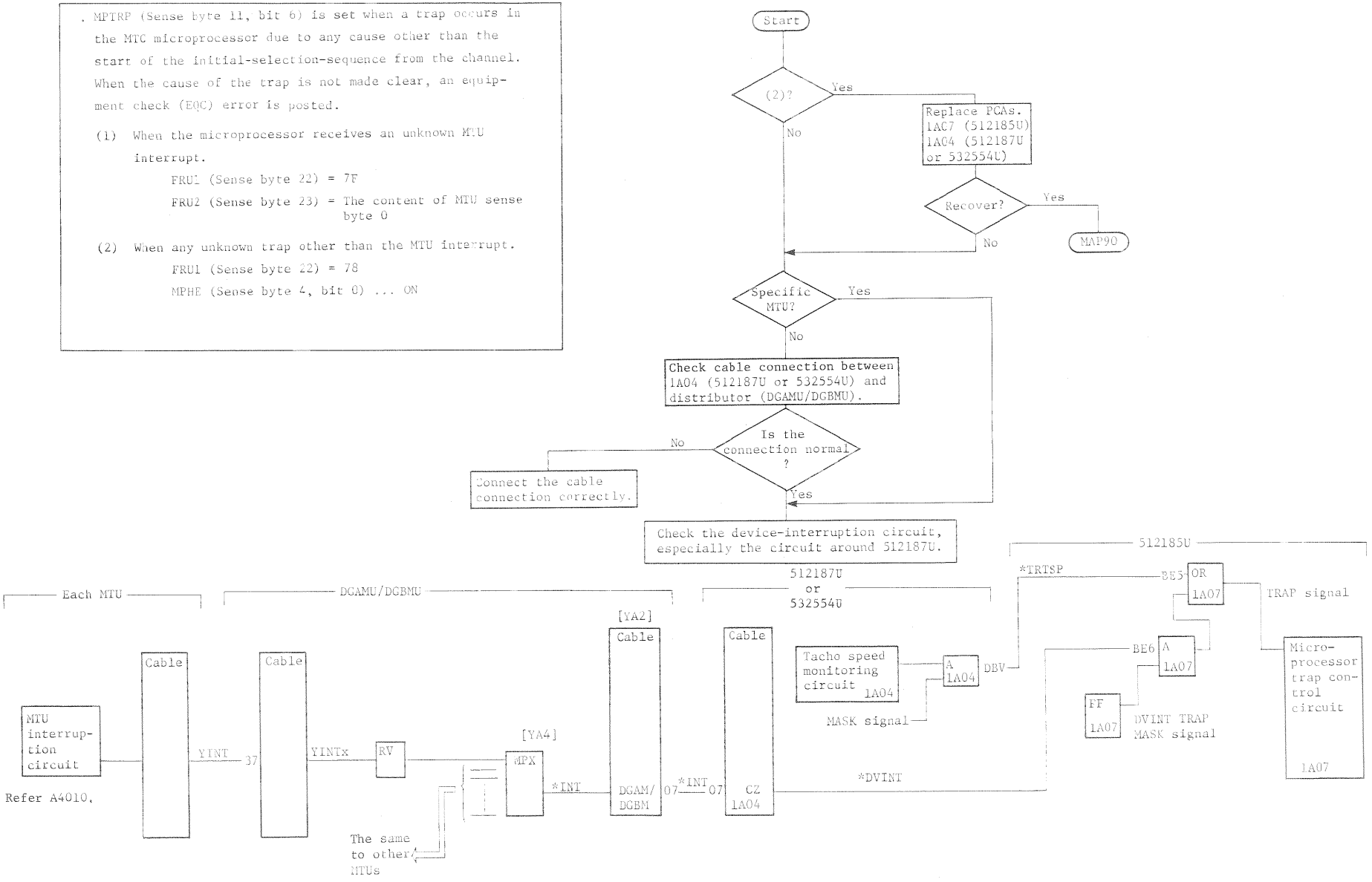
FRU1 (Sense byte 22) = 7F

FRU2 (Sense byte 23) = The content of MTU sense byte 0

(2) When any unknown trap other than the MTU interrupt.

FRU1 (Sense byte 22) = 78

MPHE (Sense byte 4, bit 0) ... ON

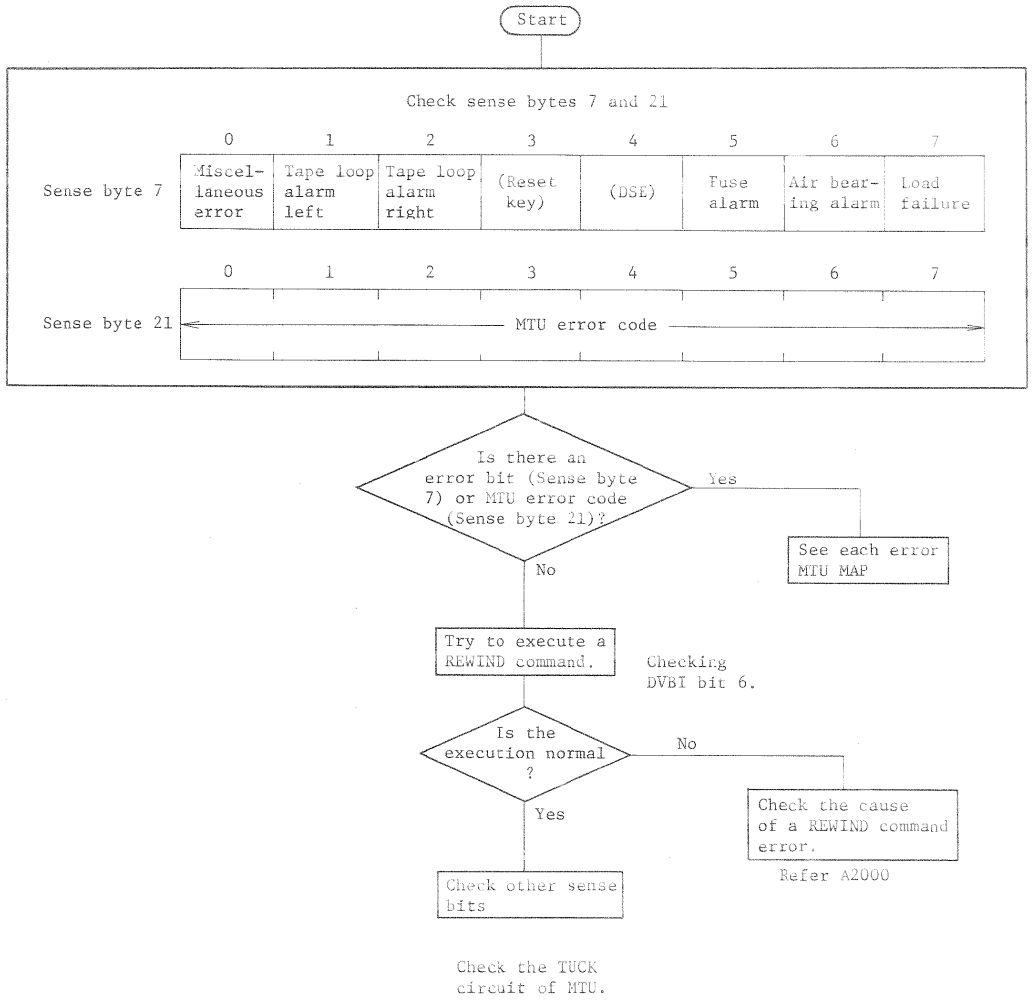


D1210	Tape Unit Check

. Tape Unit Check (Sense byte 4, bit 6) is set when the MTC detects an abnormal state of the selected tape unit. More detailed error information is displayed on Sense bytes 7 and 21.

. When the cause of tape unit check is laid only in load failure (Sense byte 7, bit 7), the EQC is not set. Otherwise, the EQC is set.

. Sense byte 21 (MTU error code) is displayed as an error code on the MTU operation panel.



D1220	Write Tape Mark Error - 1

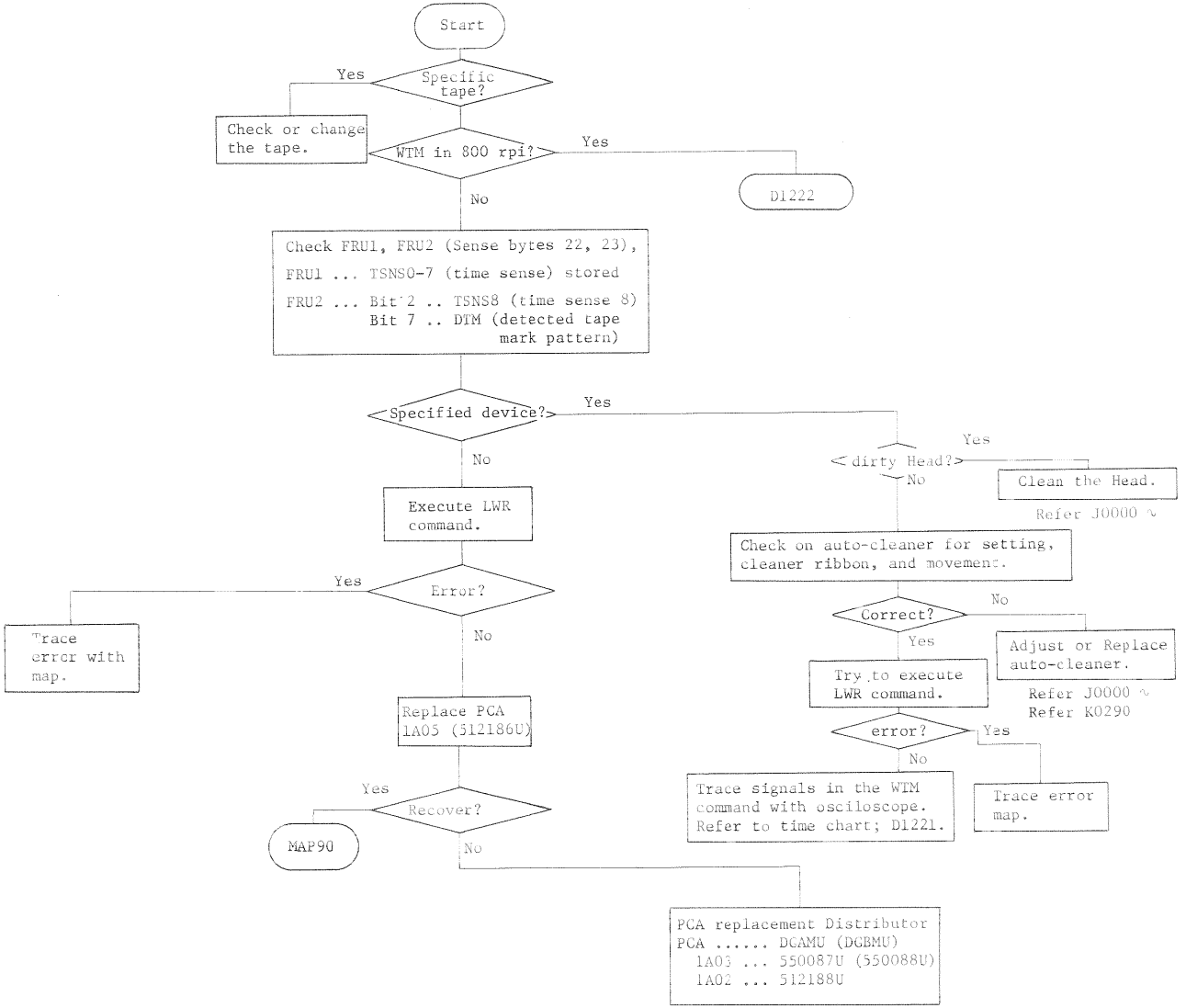
This error occurs when TM (Tape Mark) is not properly written.

(1) When the TM pattern cannot be detected within the specific length from the end of recording the TM block in 6250/1600 rpi operation.

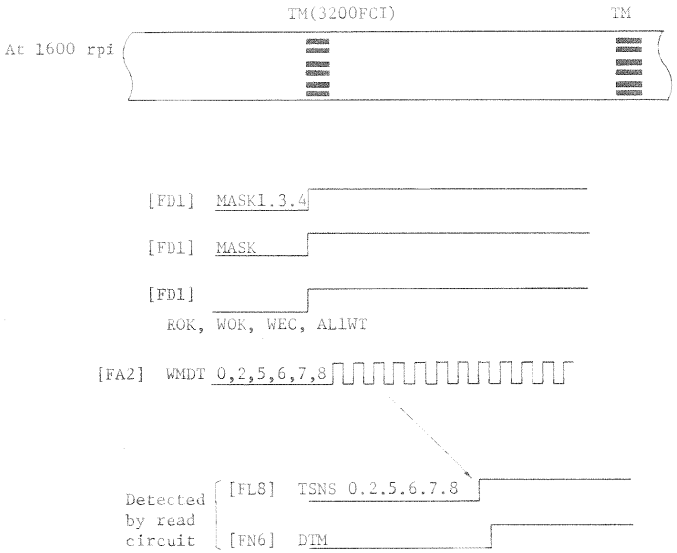
(2) When IBG cannot be detected within the specific length from the end of the TM block in 6250/1600 rpi operation.

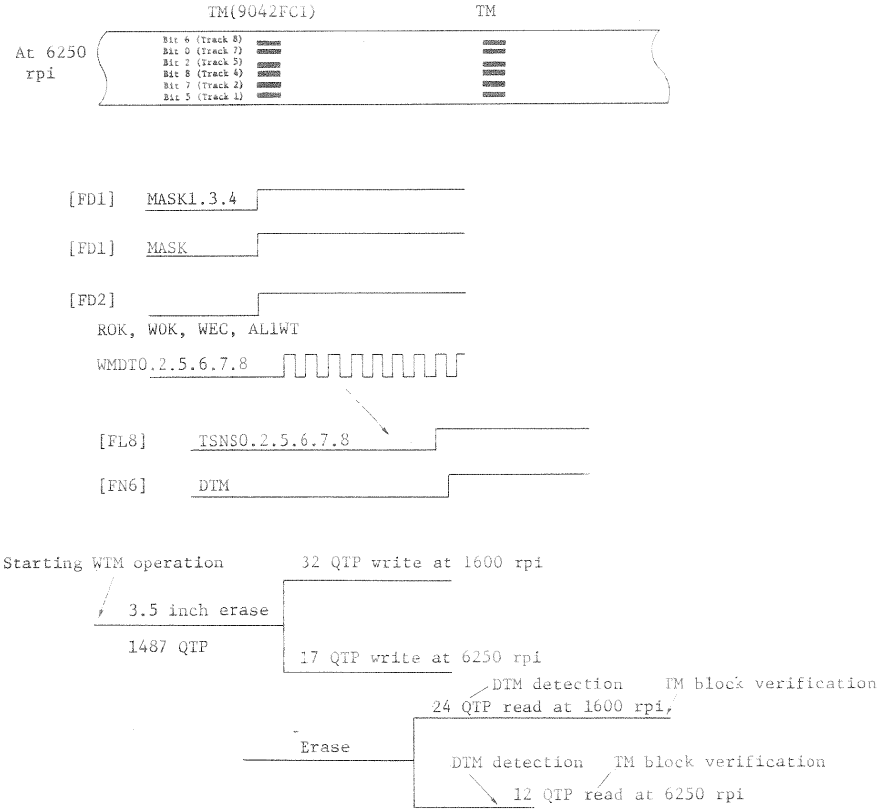
(3) When the TM code cannot be detected in 800 rpi operation.

At this time, the contents of time sense are stored in FRU1 (Sense byte 22) in 6250/1600 rpi. Time sense data is the actual data bit pattern.

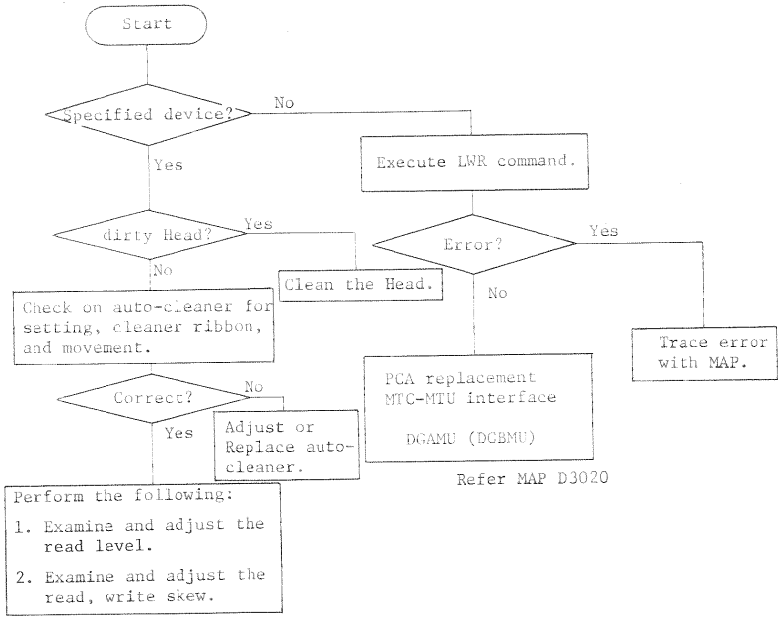


D1221	Write Tape Mark Error - 2

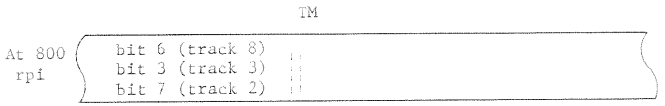


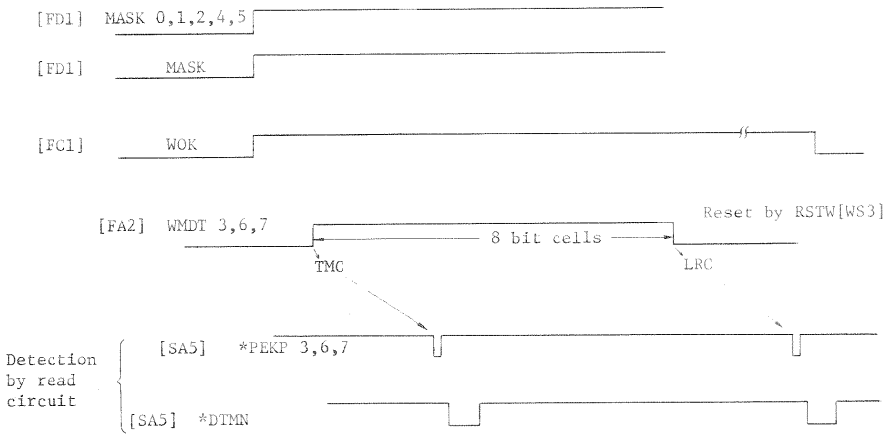


D1222	Write Tape Mark Error - 3



A7000 (6250/1600 RPI MTJ)
A7100 (1600/800 RPI MTU)





D1230	ID Burst Check - 1

ID Burst Check

Generated when recording density identification (ID), ARA and IVTM (ARA ID) are not written correctly on the load point.

1. ID Burst could not be detected.

   6250 rpi - Track 6 (bit 1)
   1600 rpi - Track 4 (bit 8)

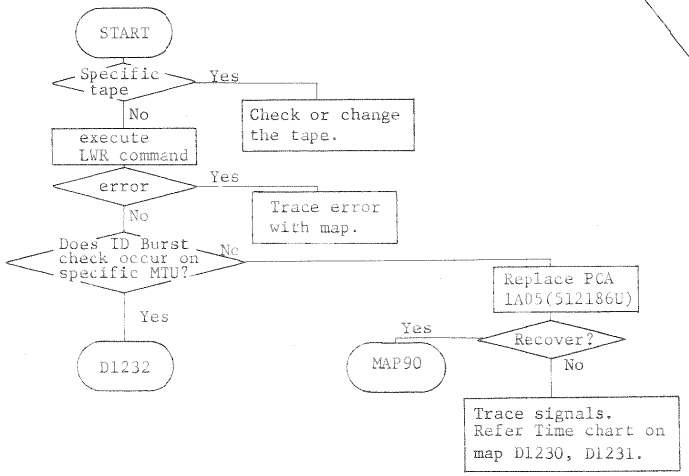
2. ARA Burst was not written correctly. (Refer to D1260.)

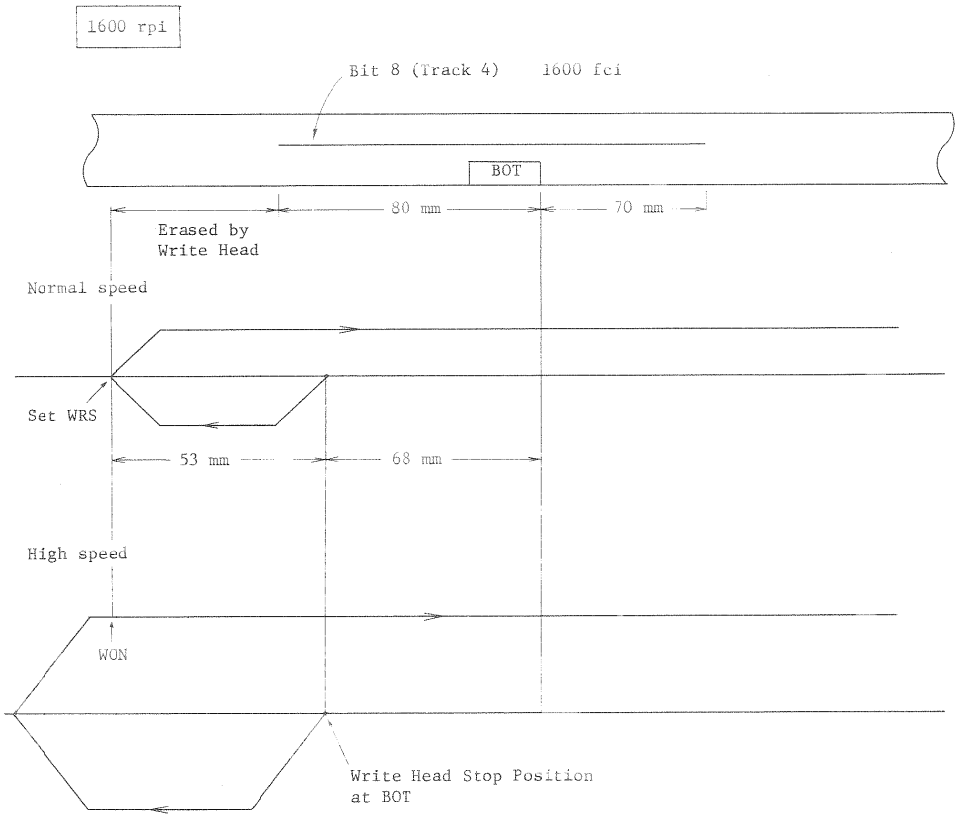
   SAGC check (sense byte 8, bit 4) is set.

3. IVTM could not be detected.

Case 1, 2 and 3, the contents of time sense are stored in FRU1 (Sense byte 22) and FRU2 (Sense byte 23).

FRU1	bit 0	TSNS0
	bit 1	TSNS1
	:	:
	bit 7	TSNS7
FRU2	bit 1	TSNS8





[FC1, FD1]

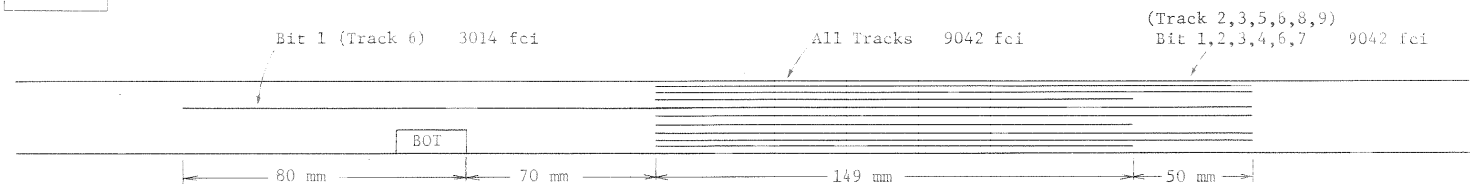
WOK, IBW, WEC, ALlWT, ROK
MASK, MASK0 ~ 7

[FA2] 1A05 AEV
WMDT8

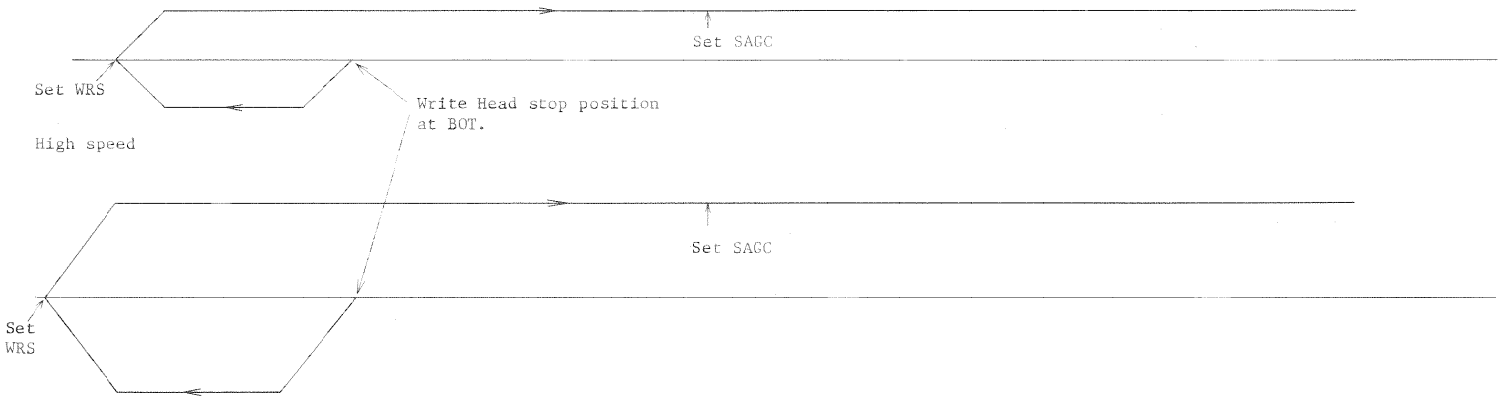
[FL8] 1A02 BB2
TSNS8 Detected at read circuit.

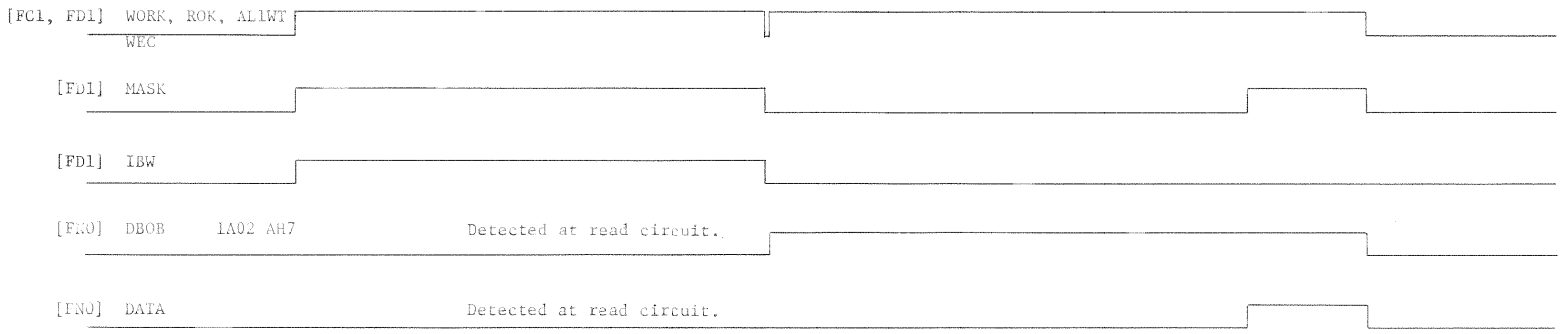
D1231	ID Burst Check - 2

6250 rpi

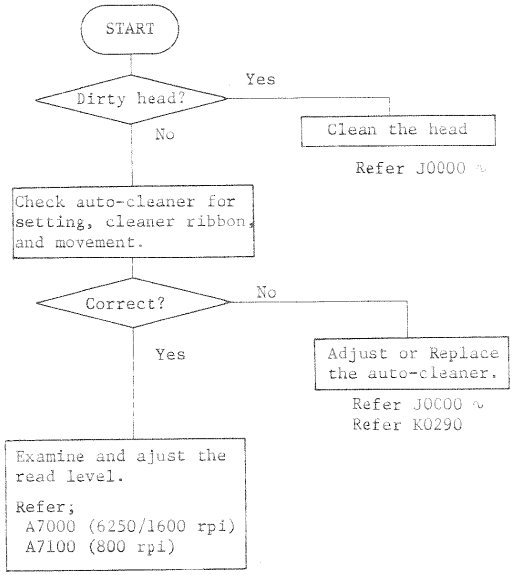


Normal speed





D1232	ID Burst Check-3



D1250	IBG Detected

Generated when;

(1) IBG was detected during write or Loop write to Read operation. Data Check bit (Sense byte 0, bit 4) is set together in this case. EVC (Sense byte 3, bit 4) may also be set in 6250/1600 rpi write operation. Following FRMs may be indicated on sense byte 22, 23.

FRU1 (Sense byte 22) ..... 'A8'

FRU2 (Sense byte 23) ..... Content of RDSNS Register.

FRU2:	0	1	2	3	4	5	6	7
	HNOIS	HBLK	HTM	(WIND)	PHOK	PREA	POSA	EPOSA

'1' when noise block has detected.

'1' when data block has detected.

'1' when tape mark block has detected.

'1' when phase OK bit has turned on.

'1' when preamble has detected.

'1' when postamble has detected.

'1' when complete postamble has detected.

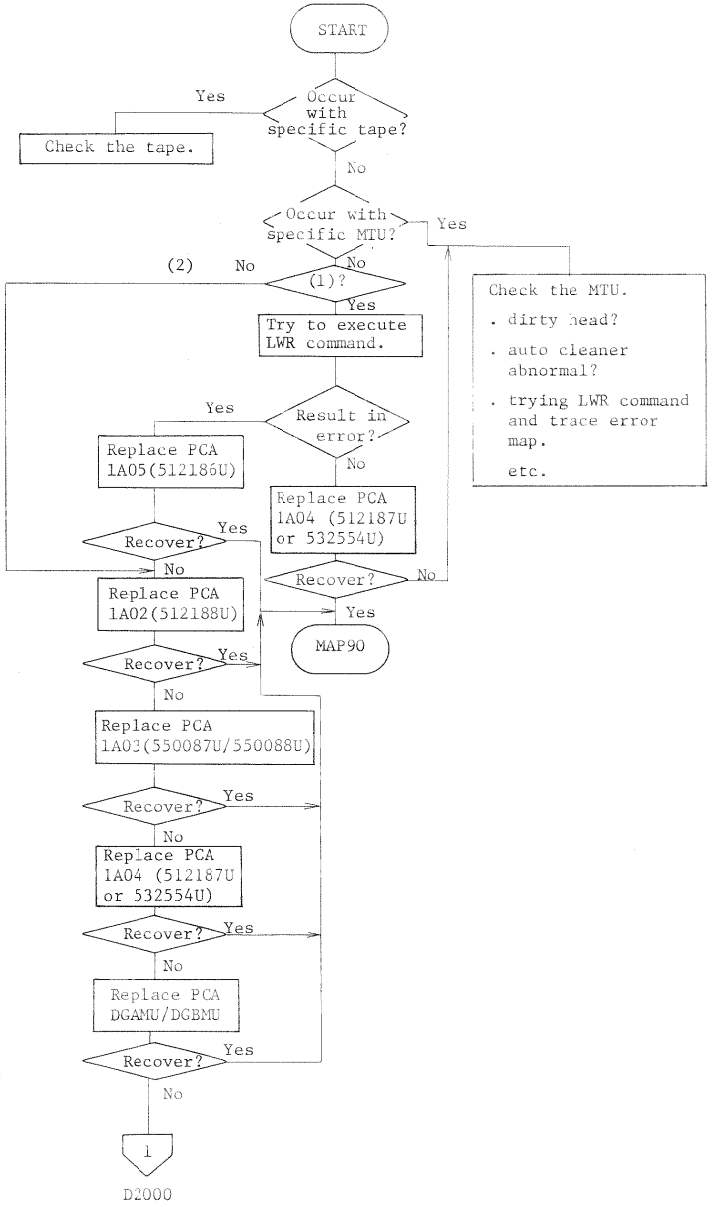
(2) IBG was not detected within the prescribed time from a point ARA on ID burst had recognized successfully in 6250 or 1600 rpi read operation respectively. Equipment Check (Sense byte 0, bit 3) is set together in this case. FRU1,2 give TSNS information as follow.

FRU1 (Sense byte 22)

0	1	2	3	4	5	6	7
TSNS0	TSNS1	TSNS2	TSNS3	TSNS4	TSNS5	TSNS6	TSNS7

FRU2 (Sense byte 23) ....

0	1	2	3	4	5	6	7
(1O2CR)	(DET8)	TSNS8	(OIBG)	(DNOIS)	(DBOB)	(DARA)	(DTM)

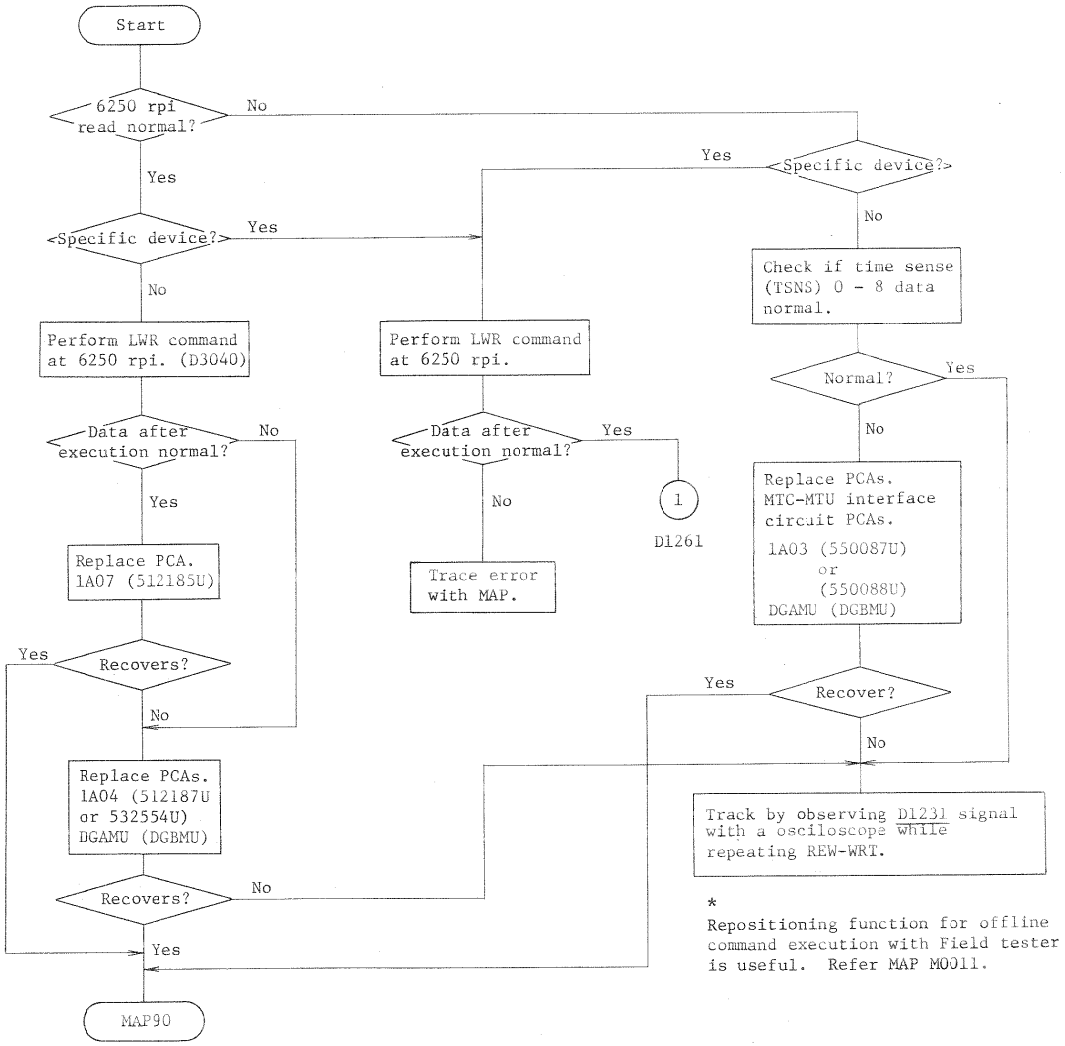


D1260	SAGC Check - 1

SAGC Check - 1

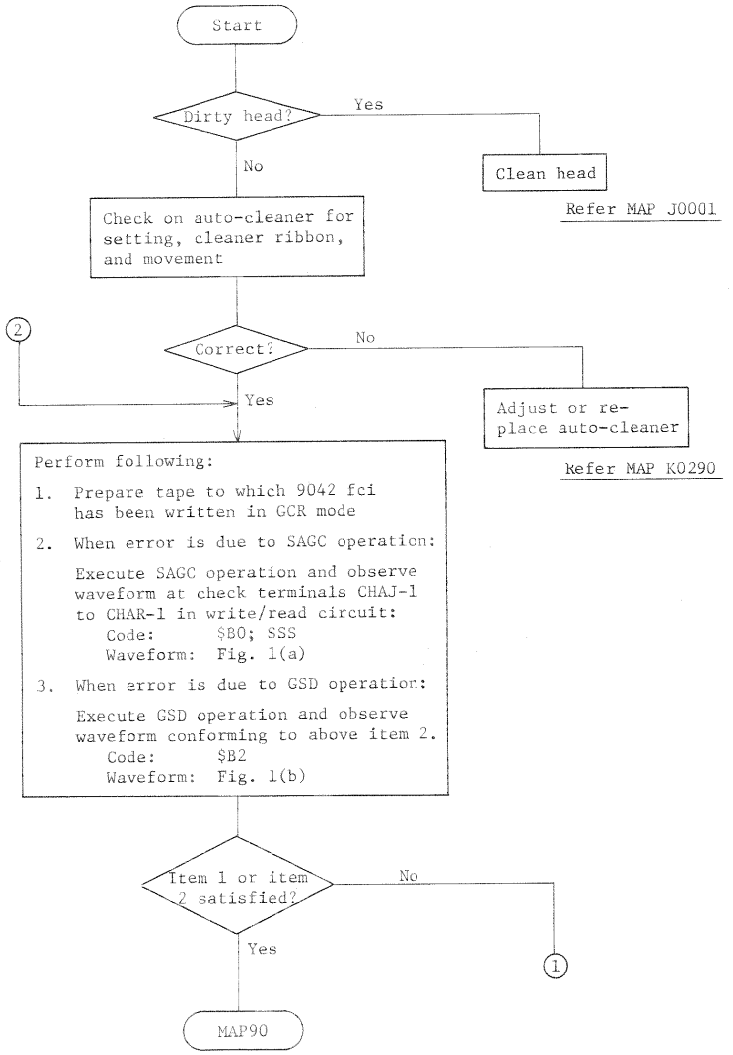
Generated in the following cases:

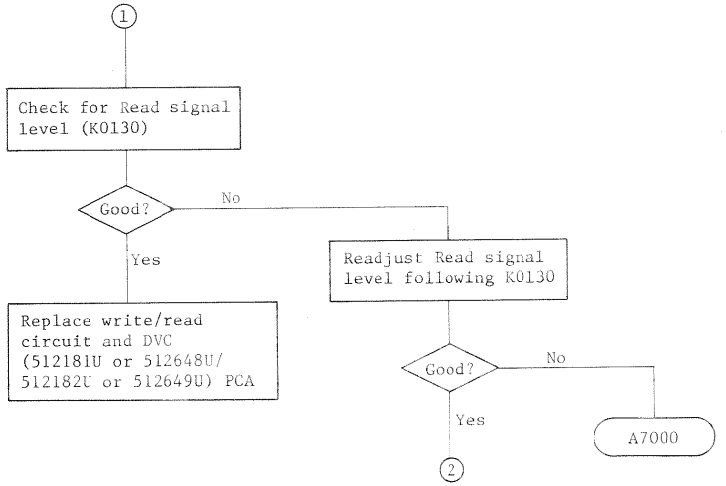
1. When ARA burst read or write was not performed normally at 6250 rpi operation.



* Repositioning function for offline command execution with Field tester is useful. Refer MAP M0011.

D1261	SAGC Check - 2





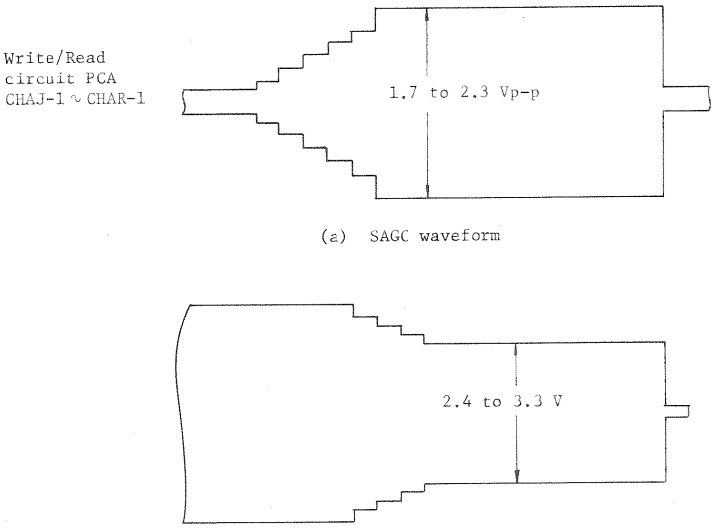


Fig. 1

D1270	No Block Detect

No Block Detect

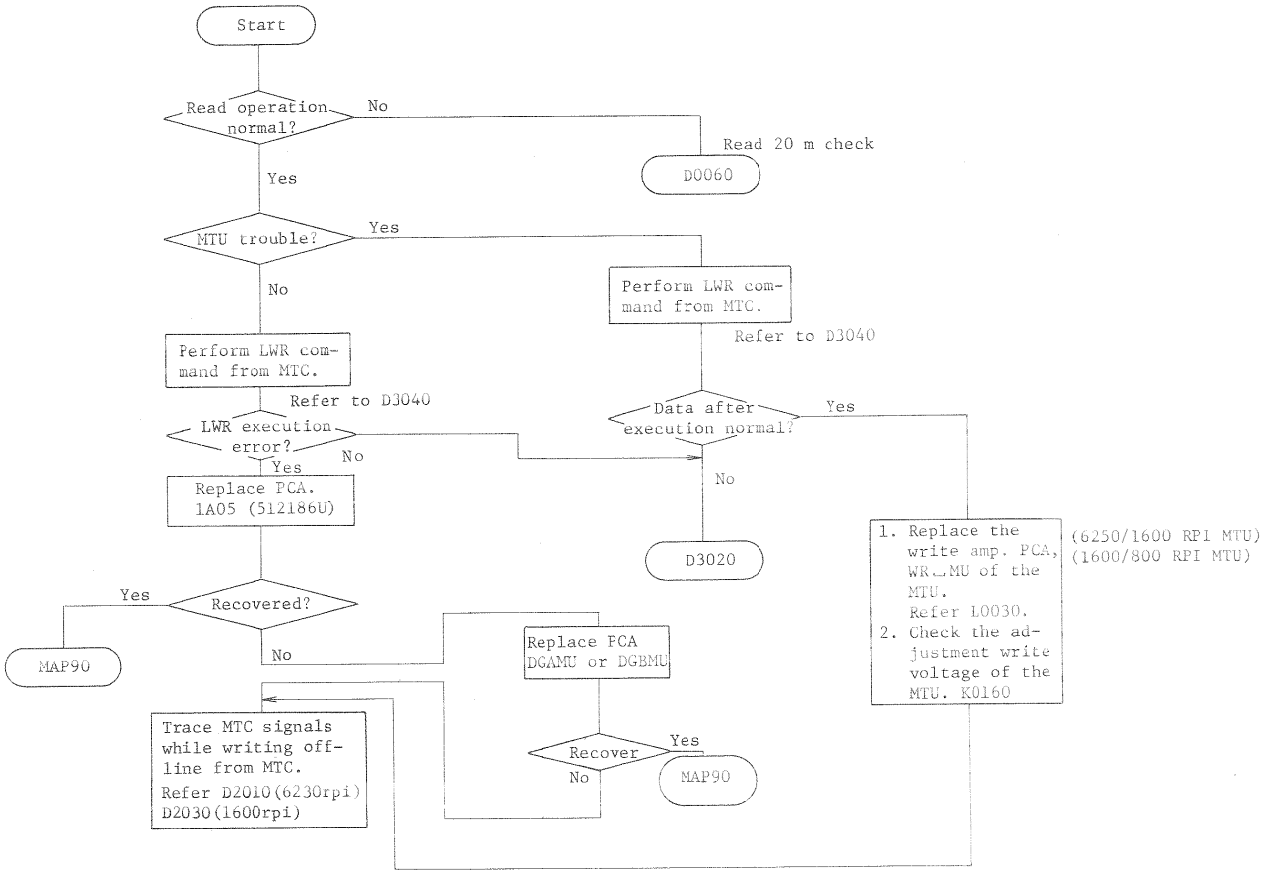
Generated when writing is started and data block cannot be detected within the prescribed length after the writing is ended at write command.
(Detected at 70 QTP)

When DNIS (Detection of Noise pattern) signal continues as long as 46 bit cell in 6250 rpi mode or 22 bit cell in 1600 rpi mode, HNOIS signal is generated.

Detection of data block depends on whether HNOIS signal is generated or not.

DNOIS Detection Pattern at 6250/1600 rpi Write

$0 \cdot 4 \cdot 6 + 1 \cdot 2 \cdot 8 + 3 \cdot 5 \cdot 7 + (0+4+6)(1+2+8)(3+5 \cdot 7)$



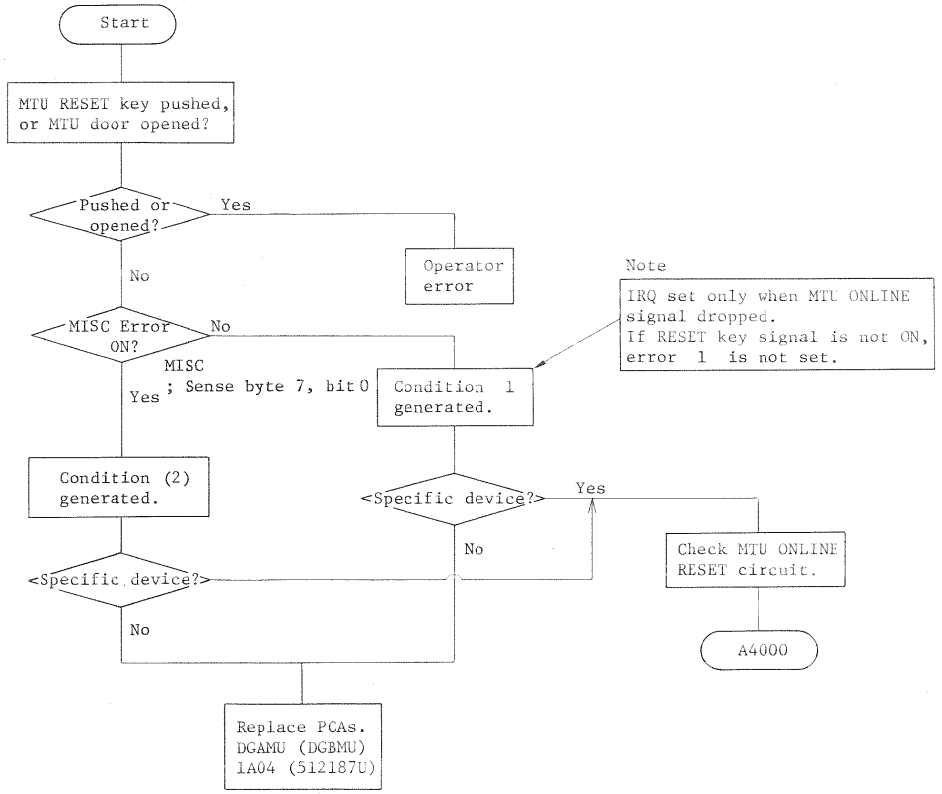
D1300	Reset Key

Reset Key

Generated in the following cases:

(1) When MTU RESET key pushed mistakenly during MTU drive.
(IRQ, RJTU also set)
FRU1 (Sense byte 22) 70

(2) When MTU door opened mistakenly during operation.
(IRQ, RJTU, Miscellaneous Error also set)
FRU1 (Sense byte 22) 70



D1310	Dynamic Reversal

Dynamic Reversal

Generated in the following cases:

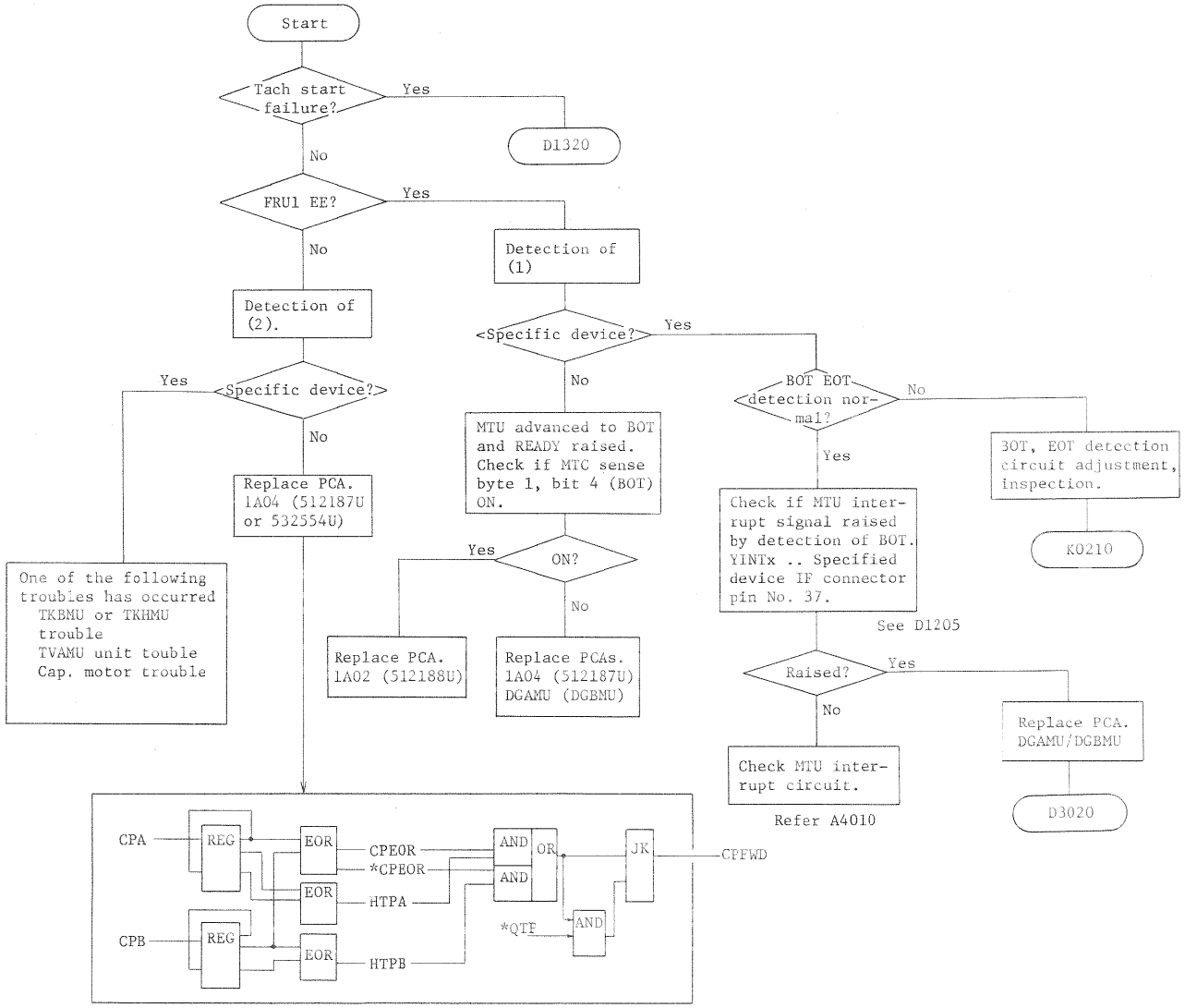
(1) IVTM block detected, but BOT not detected within the prescribed length at backward operation at 6250 rpi.

- o FRU1 (sense byte 22) .... EE
- o FRU2 (sense byte 23) .... Time sense 0 - 7
- o IVTM detection detected at 28TP (6.7 mm)
- o BOT must be detected within 2304FTP (550 mm) after IVTM detection.

(2) Operated more than the prescribed QTP number in reverse direction at MTU starting.

- o FRU1 (sense byte 22) CC
- o FRU2 (sense byte 23) .... TQP count number (length of running in drive direction)

Error when operated 108TP in reverse direction.



Reverse or Forward Direction Detect Circuit

D1320	Tach Start Failure - 1

Generated in the following cases:

(1) When prescribed QTP length within the prescribed time at MTU starting.

FRU1 (sense byte 22) ... 108-QTP count total (Drive direction and Reverse direction)

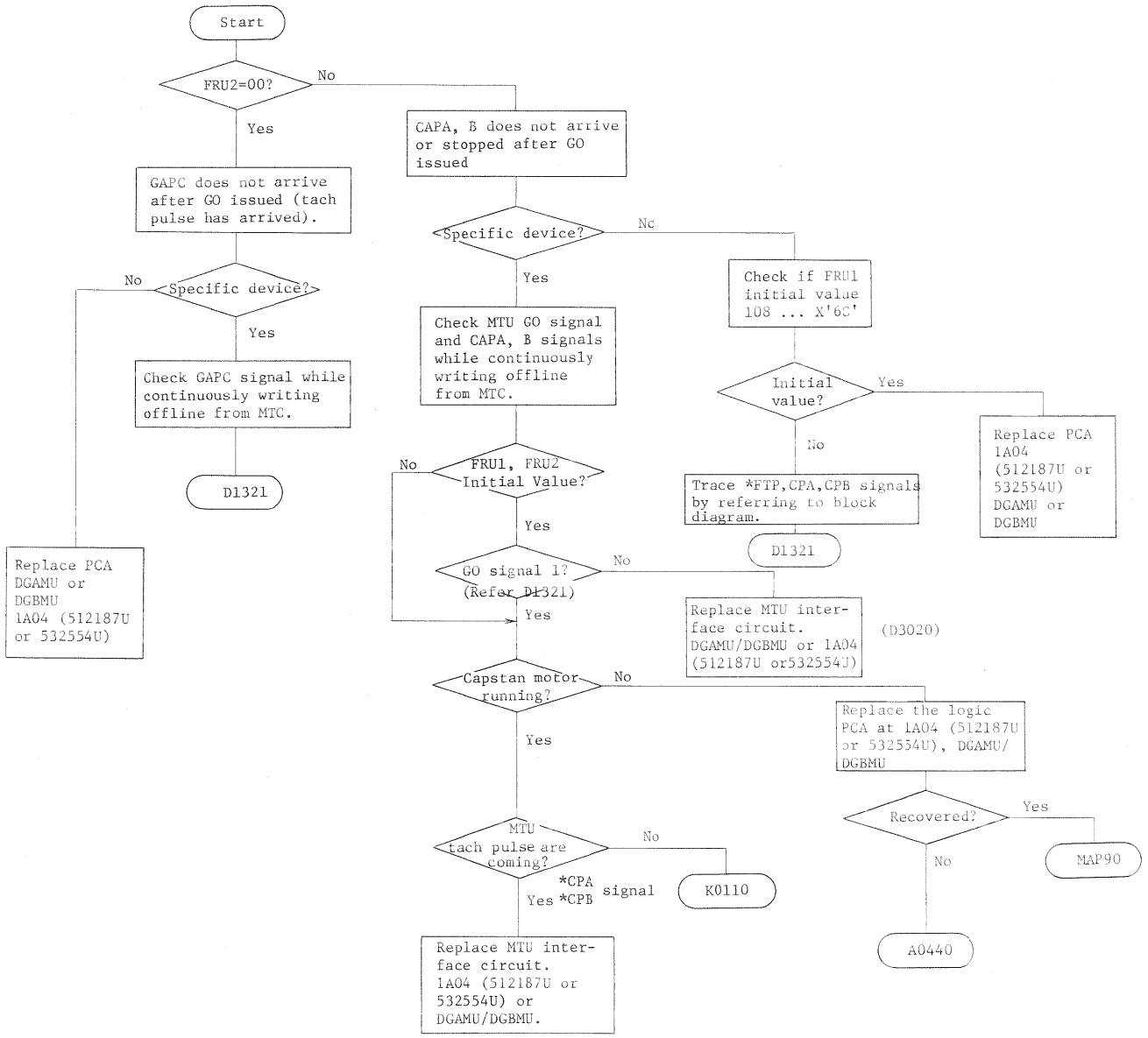
FRU2 (sense byte 23) ... 20-Drive direction QTP count

(2) When GAP CTL was not raised within prescribed time at MTU starting.

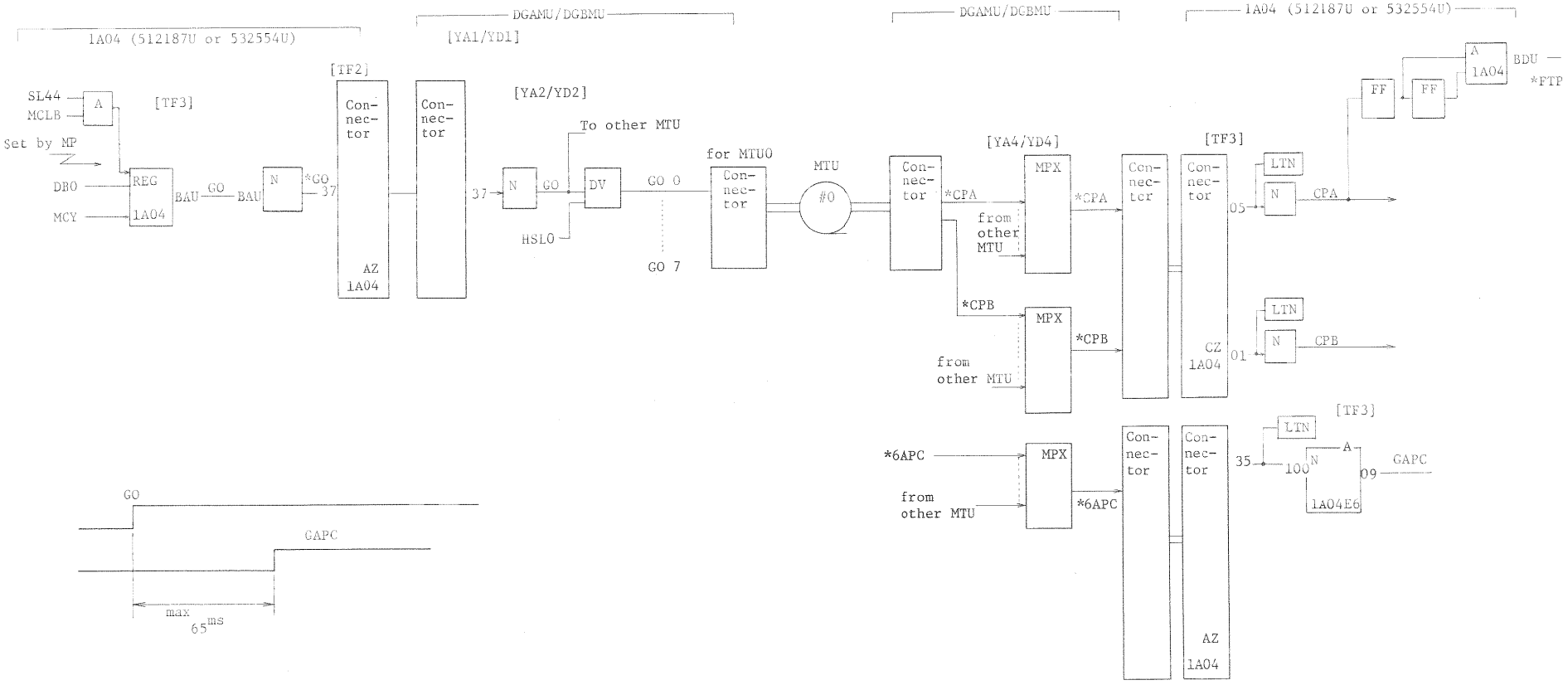
FRU1 ... 108-QTP spacing at that time

FRU2 ... 00

Prescribed time ..... 65 ms



D1321	Tach Start Failure - 2



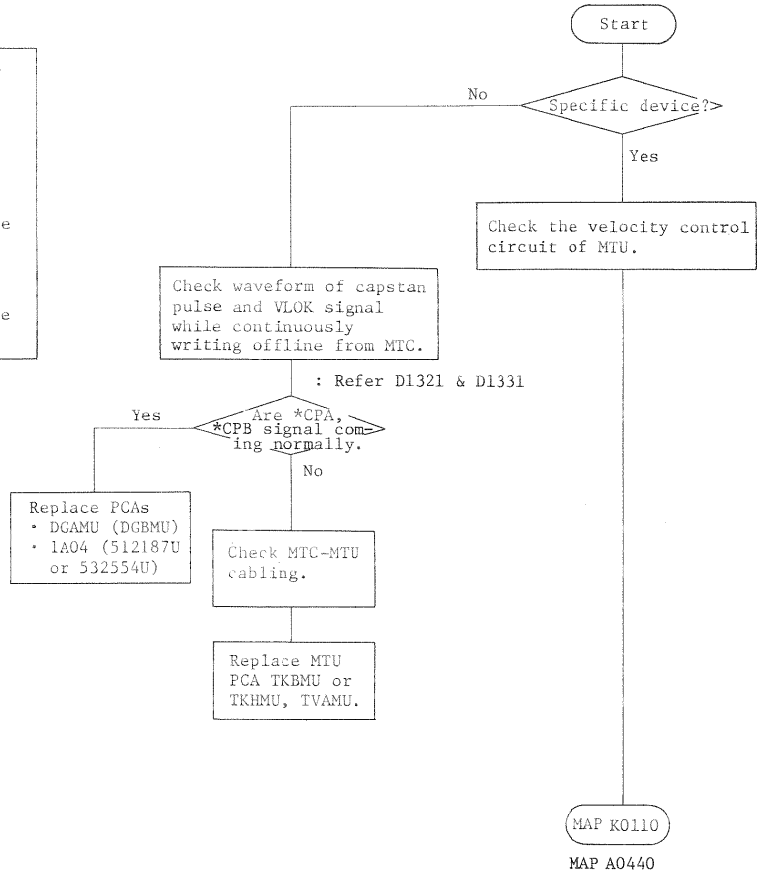
D1330	Velocity Check

Velocity Check

Generated when Velocity retry over (16 times) has occurred during write operation.

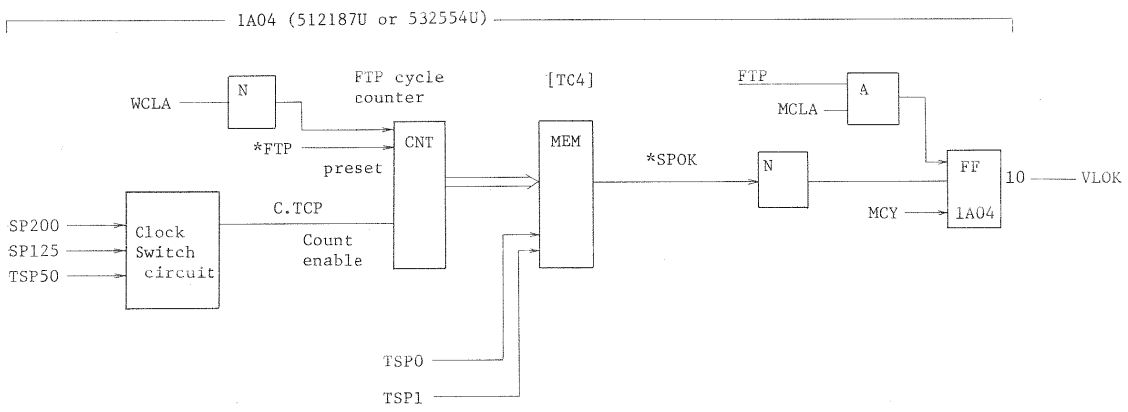
o Velocity retry:

Write start was late because capstan speed was not prescribed value.
(Not within prescribed value ±7%)



D1331	Velocity Check - 2

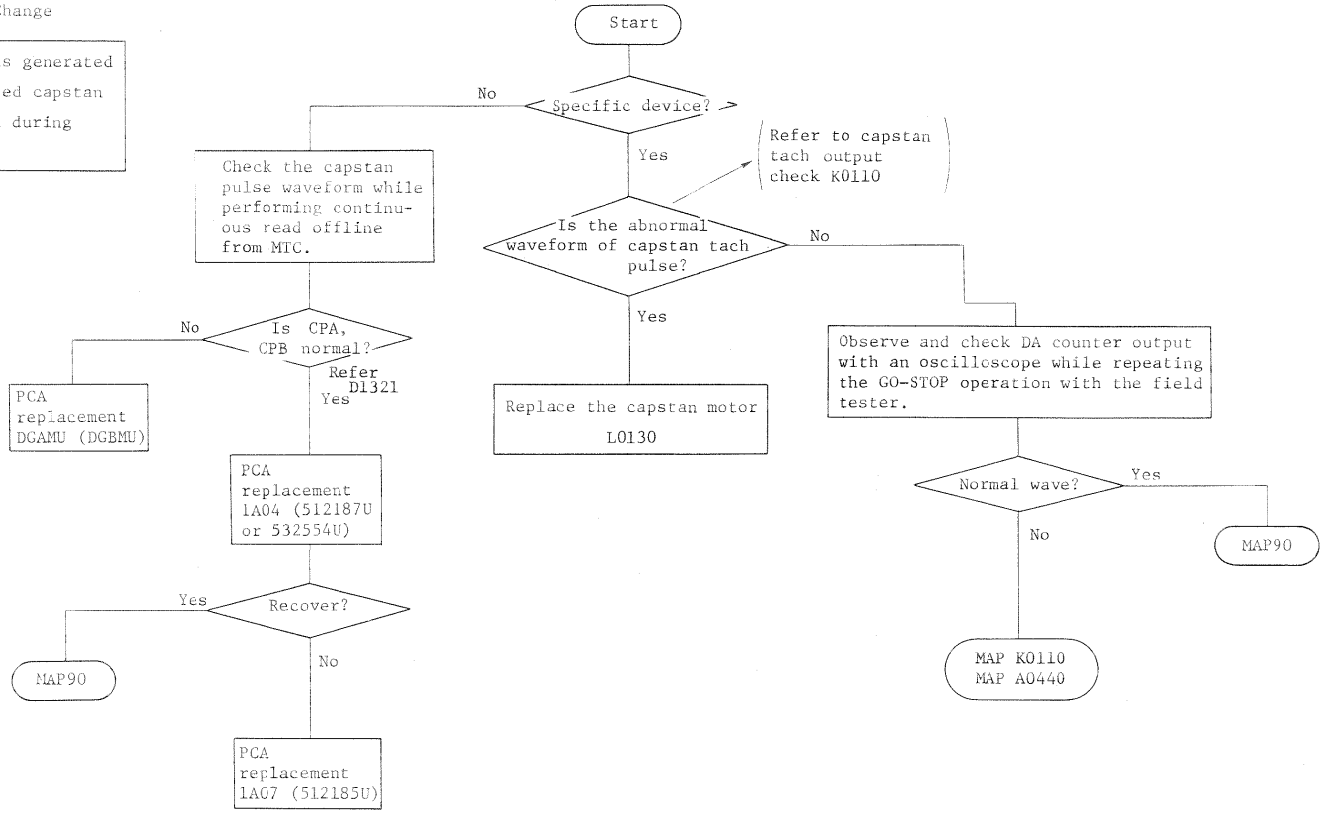
Velocity check circuit



D1340	Velocity Change

Velocity Change

Velocity change is generated when the designated capstan speed is exceeded during write operation.



D1350	Early begin read back check, Slow begin read back check, Slow end read back check

o Early begin read back check

These are generated in the following cases:

(1) When data-byte (800 bpi) or DBOB pattern (1600/6250 rpi) is detected within (a) shown at Fig. 1 at write command execution.
(When data is detected too early.)

(2) When IBG is detected during writing (WOK signal on) at write command of 800 rpi.
(When IBG is detected too early.)

o Slow begin read back check

Generated when data-byte (800 bpi) or No. 5 pattern (1600/6250 rpi) is detected within (b) shown in Fig. 1.
(When data is detected too slow.)

o Slow end read back check

Generated when IBG detected at over 700TP after block end detected after write end.

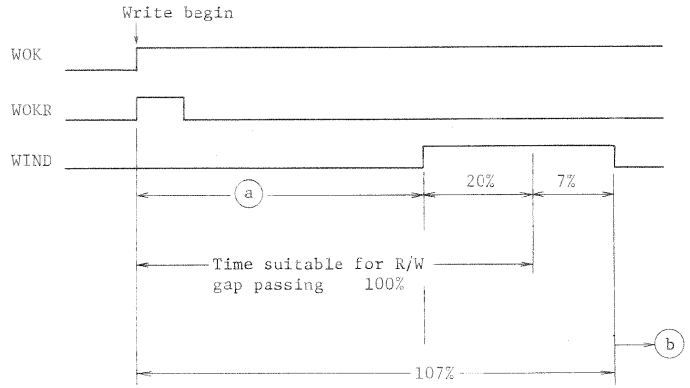
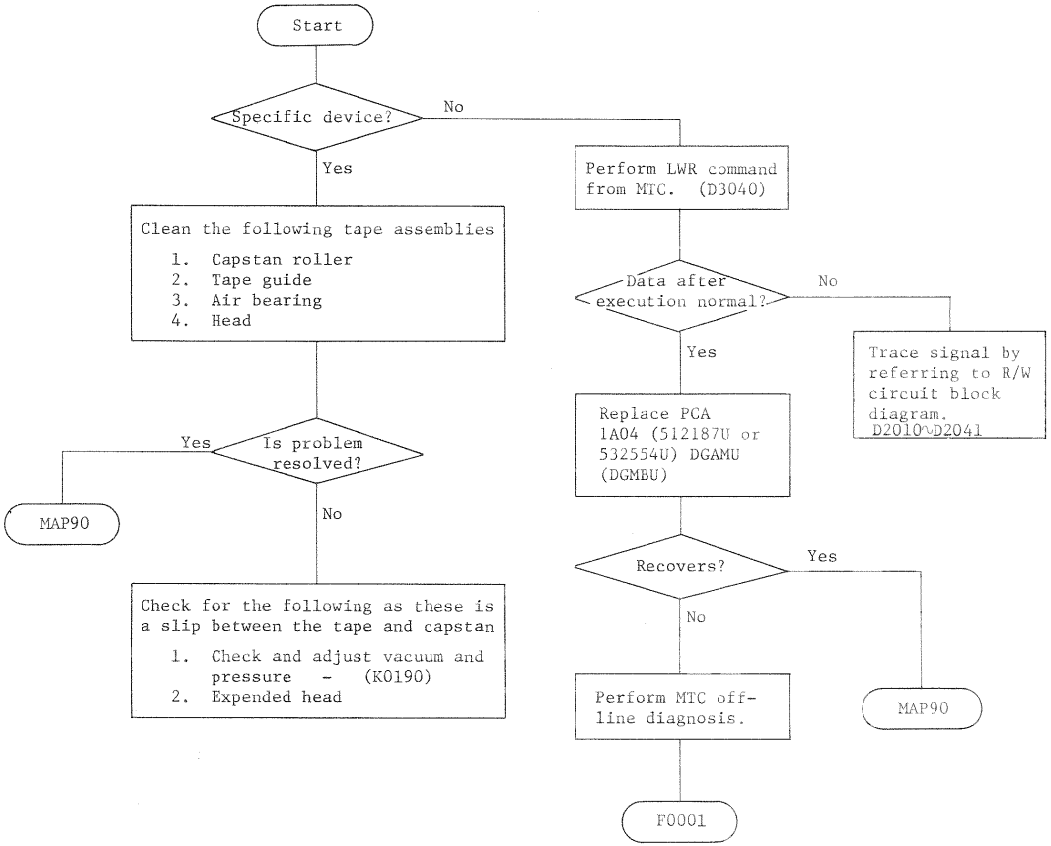


Fig. 1 Slip check timing



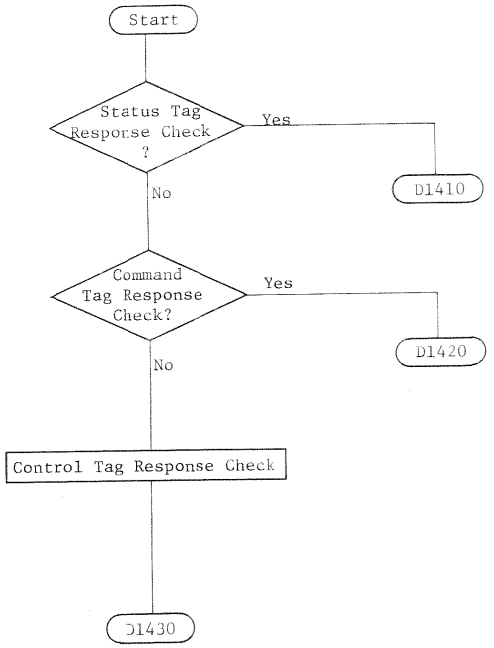
D1400	Status Tag Response Check Command Tag Response Check Control Tag Response Check

The MTC uses three tag signal lines (Status tag, Control tag, and Go tag) to carry out control on the MTU. Further, the MTC uses the status tag line in conjunction with the control tag line as a command tag line when both the status and the control tag lines are activated.

When the MTC uses the status tag, control tag, and command tag lines to control the MTU, the MTC receives a response from the MTU. When the response is not normal, the Status Tag Response Check, Control Tag Response Check, and Command Tag Response Check are set.

FRU1 (Sense byte 22) ..... Control data
(Content of DVEO register)

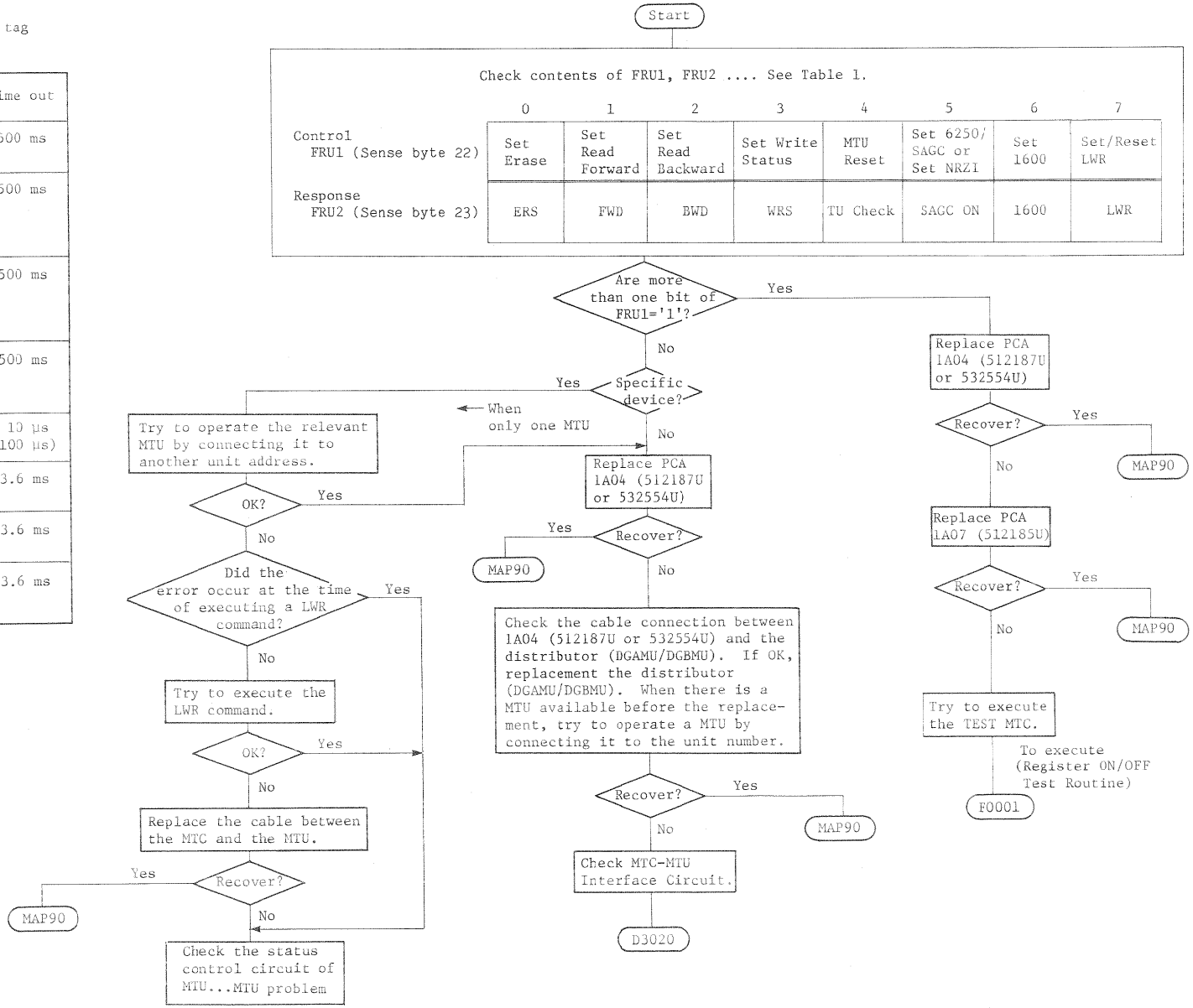
FRU2 (Sense byte 23) ..... Response data
(Content of DVEO register)



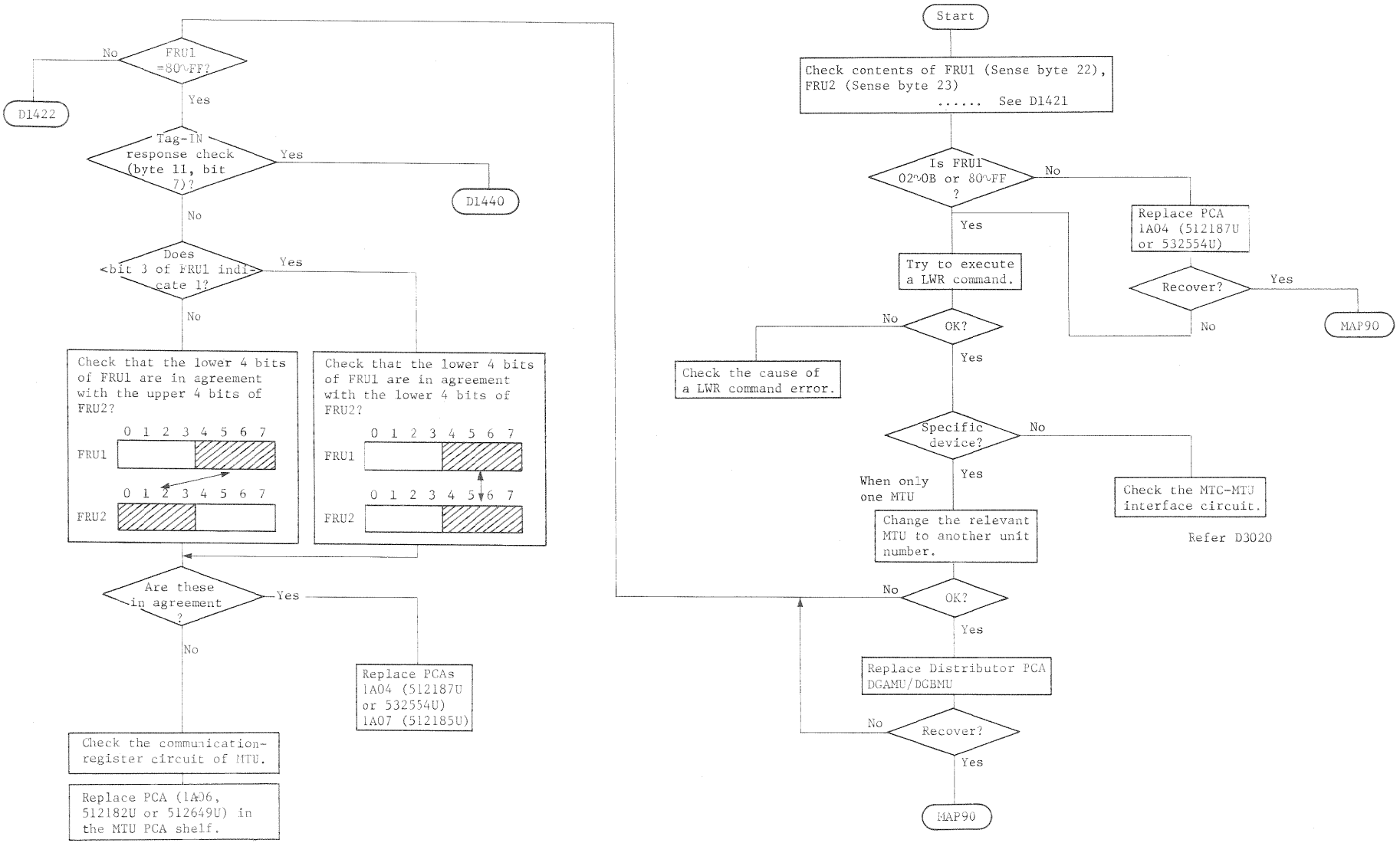
D1410	Status Tag Response Check

Table 1 Response check with status tag control

Control (FRU1) bit	Function	Response (FRU2) checked	Time out
bit 0	Set ERASE ("1")	ERS=1, LWR=0 FWD=1, BWD=0	500 ms
bit 1	Set Read Forward ("1")	FWD=1, ERS=0 BWD=0 WR=0 LWR=0	500 ms
bit 2	Set Read Backward ("1")	BWD=1, ERS=0 FWD=0 WRS=0 LWR=0	500 ms
bit 3	Set Write Status ("1")	ERS=1, BWD=0 FWD=1, LWR=0 WRS=1	500 ms
bit 4	Reset MTU ("1")	TU check = 0 (DVINT=0)	10 µs (100 µs)
bit 5	Set GCR/NRZI ("1")	1600=0	13.6 ms
bit 6	Set PE ("1")	1600=1 SACC=0	13.6 ms
bit 7	Set LWR Reset LWR ("1")	LWR=1 LWR=0	13.6 ms



D1420	Command Tag Response Check-1



D1421	Command Tag Response Check - 2

FRU1 (Sense byte 22)

bit 0 1 2 3 4 5 6 7		Function	Response (FRU2)	Time out
0	2	Set streaming mode	Streaming mode = 1	1513 ms
0	3	Reset streaming mode	Streaming mode = 0	
0	4	Space file	READY = 0	
0	5	Backspace file	READY = 0	
0	6	(Spare)		
0	7	(Spare)		
0	8	Set LWR2	LWR2 = 1	13.6 ms
0	9	Reset LWR2	LWR2 = 0	
0	A	Set low slice	Low slice = 1	
0	B	Reset low slice	Low slice = 0	

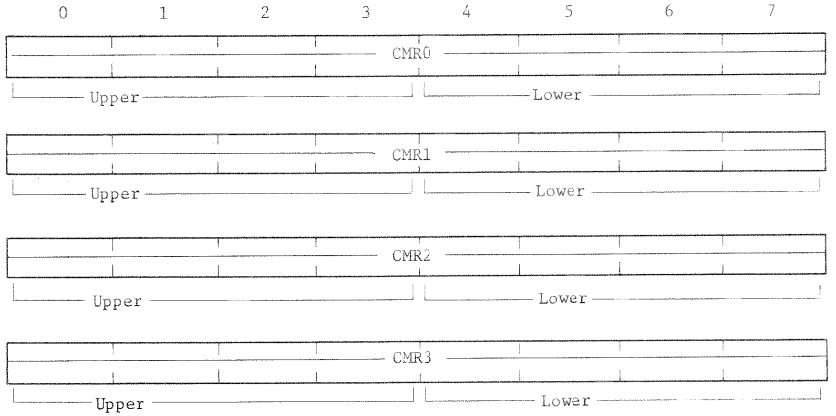
FRU2 (Sense byte 23)

bit 0	1	2	3	4	5	6	7
Streaming feature	Skip file feature	(Spare)	Low sloce	Streaming mode	LWR2	Handler action	READY

FRU1 (Sense byte 22)

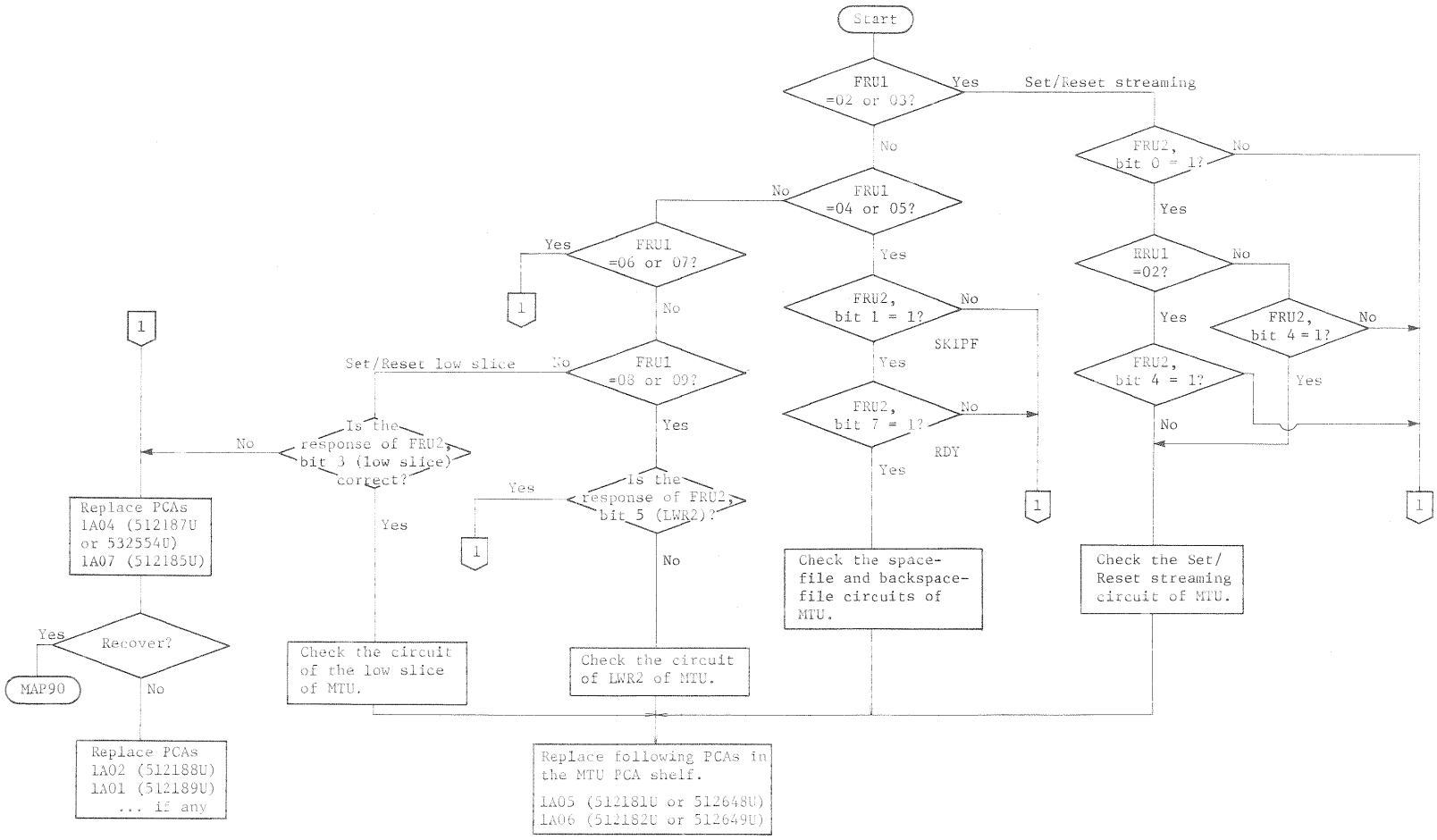
bit 0 1 2 3 4 5 6 7		Function	Response/Time out
8	0 ∿ F	Set CMR0 upper	The upper and lower values of CMR are in agreement with those intended to be set. Time out = 700 μs
9	0 ∿ F	Set CMR0 lower	
A	0 ∿ F	Set CMR1 upper	
B	0 ∿ F	Set CMR1 lower	
C	0 ∿ F	Set CMR2 upper	
D	0 ∿ F	Set CMR2 lower	
E	0 ∿ F	Set CMR3 upper	
F	0 ∿ F	Set CMR3 lower	

FRU2 (Sense byte 23)



CMR0 ∿ 3: Communication register 0 ∿ 3.

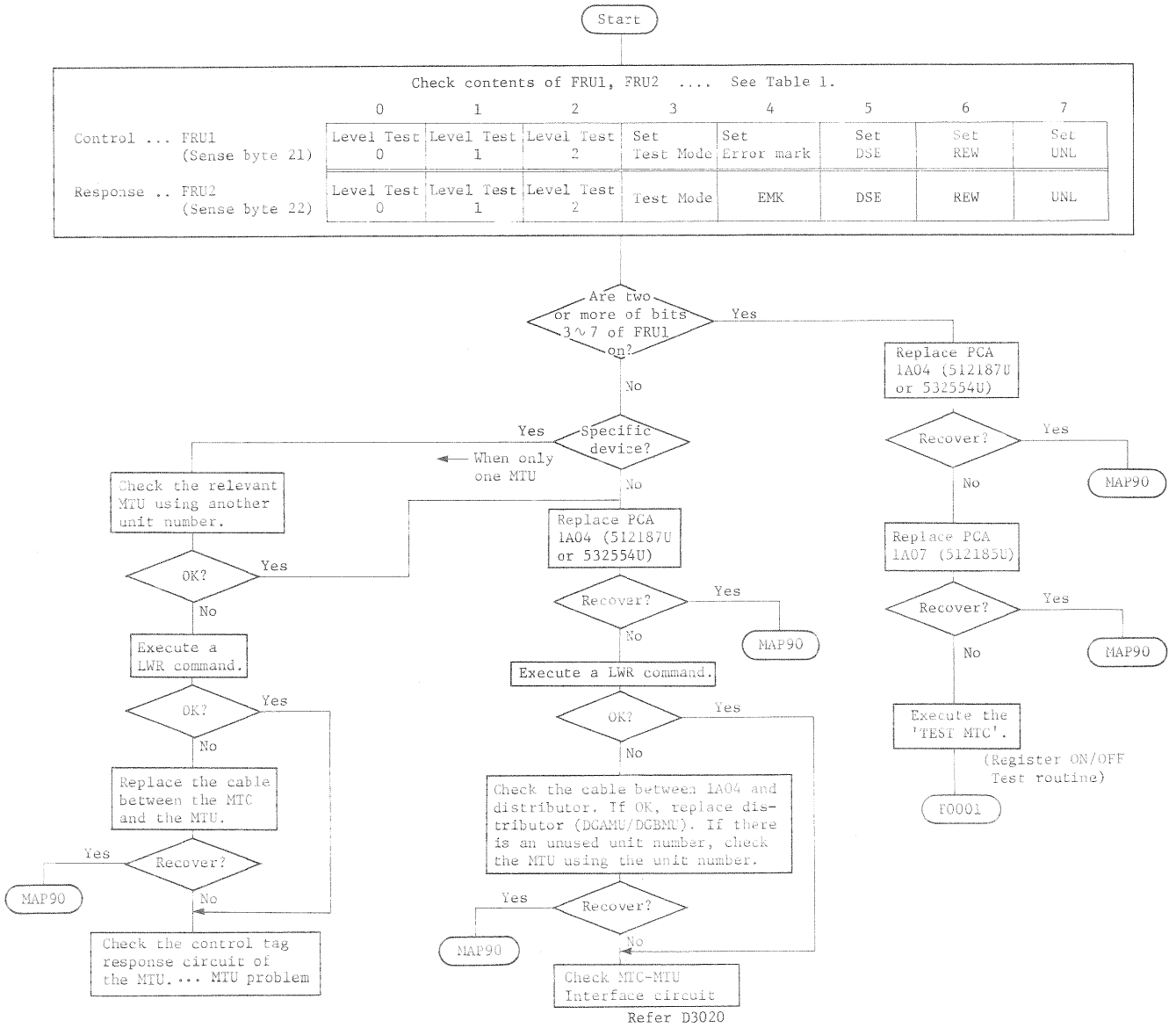
D1422	Command Tag Response Check - 3



D1430	Control Tag Response Check

Table 1 Response check with Control Tag

Control FRU1	Function	Response (FRU2)	Time out
bit 0 ∿ bit 2	Level set	Level Test 0∿2	500 ms
bit 3	Set Test-Mode	Test Mode	500 ms
bit 4	Set EMK	EMT = 1	500 ms
bit 5	Set DSE	DSE = 1 (also READY = 0)	500 ms
bit 6	Set REW	REW = 1 (also READY = 0)	500 ms
bit 7	Set UNL	UNL = 1 (also READY = 0)	500 ms

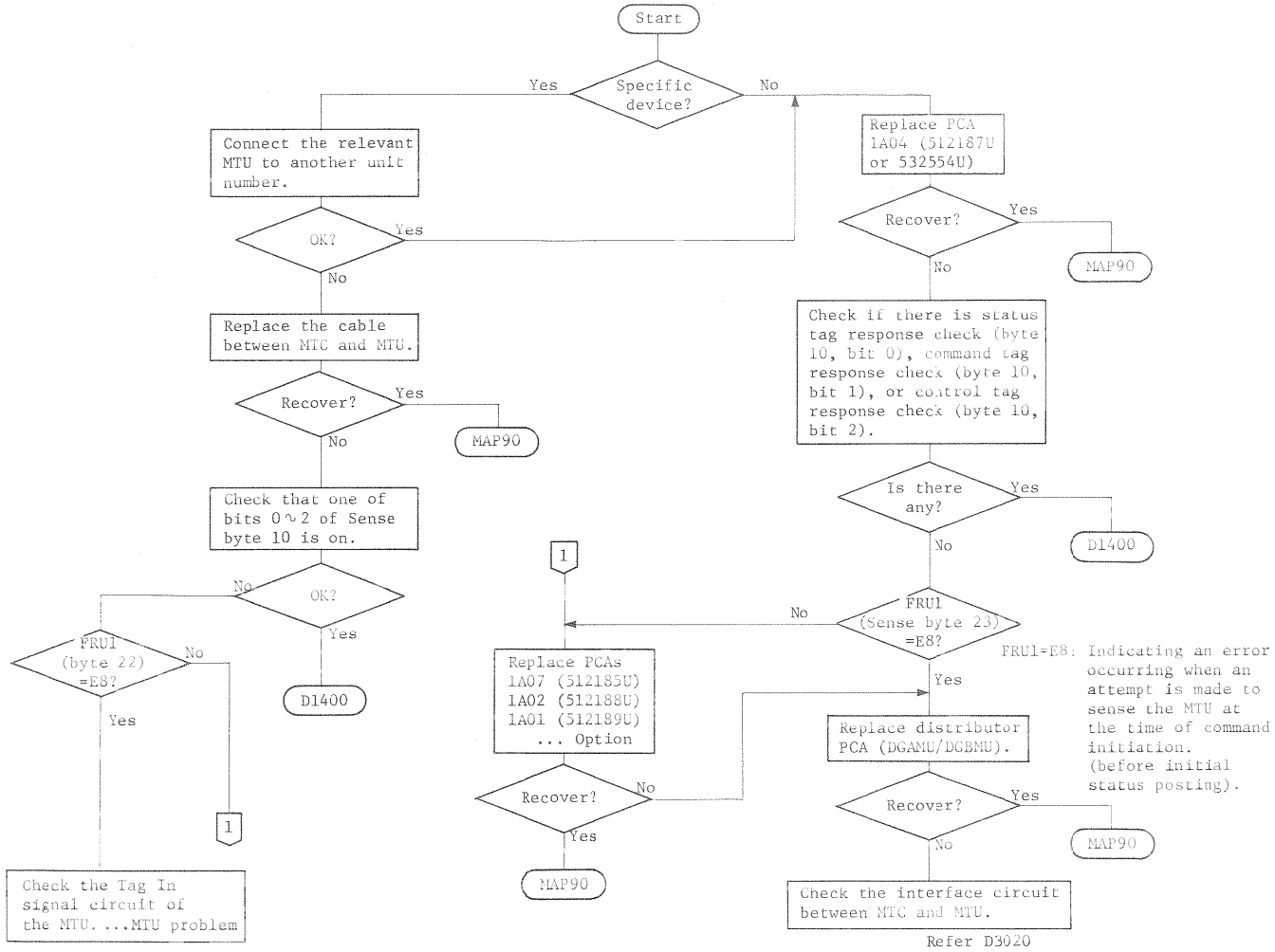


D1440	Tag In Check

Tag In Check

Generated when TAG-IN signal response does not arrive within the prescribed time from MTU for TU sense specified from MTC.

(Prescribed time = 3 ∿ 7 μs)



D1450	Read/Write Overrun

Read/Write Overrun (Read/write time-out)

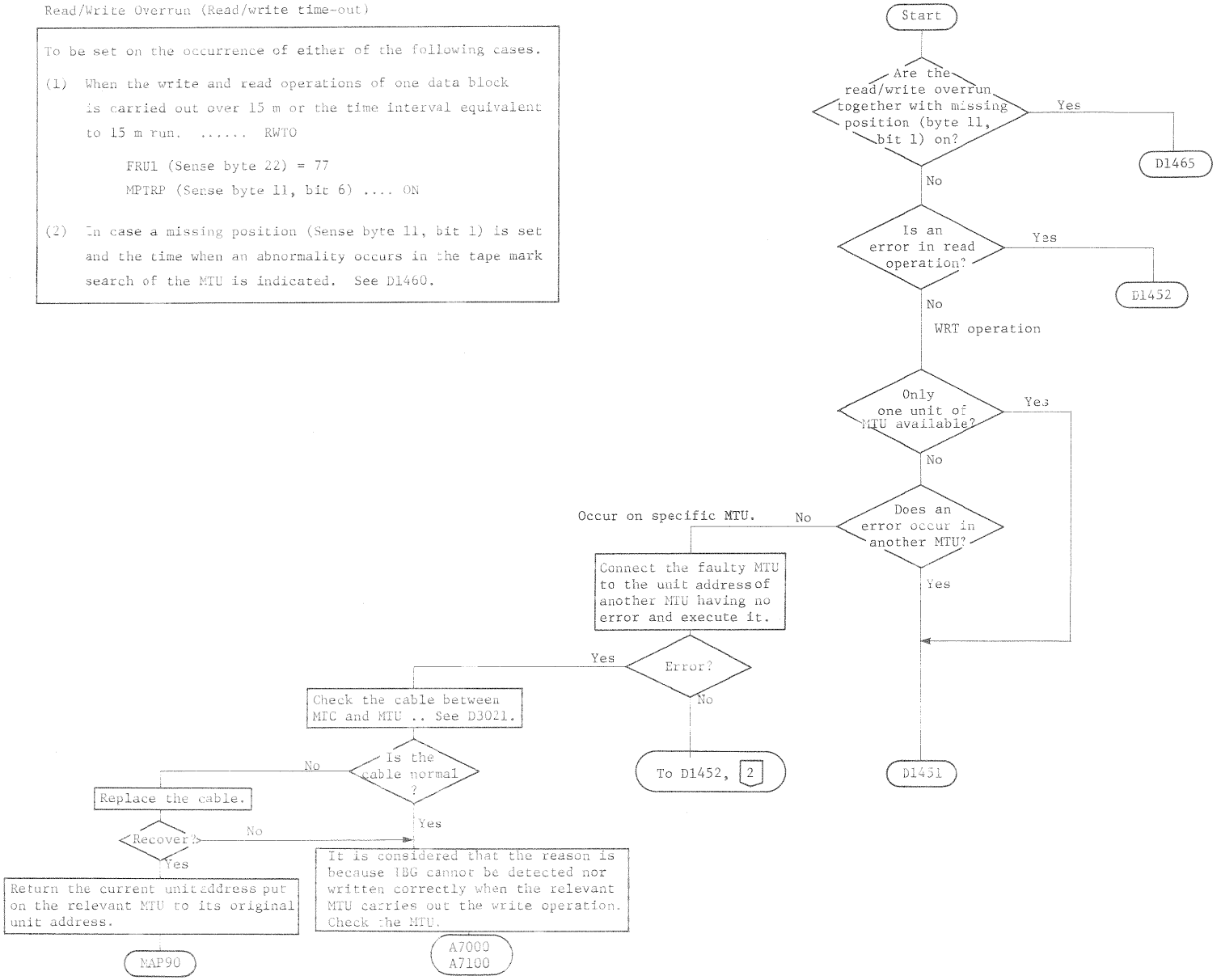
To be set on the occurrence of either of the following cases.

(1) When the write and read operations of one data block is carried out over 15 m or the time interval equivalent to 15 m run. ..... RWTO

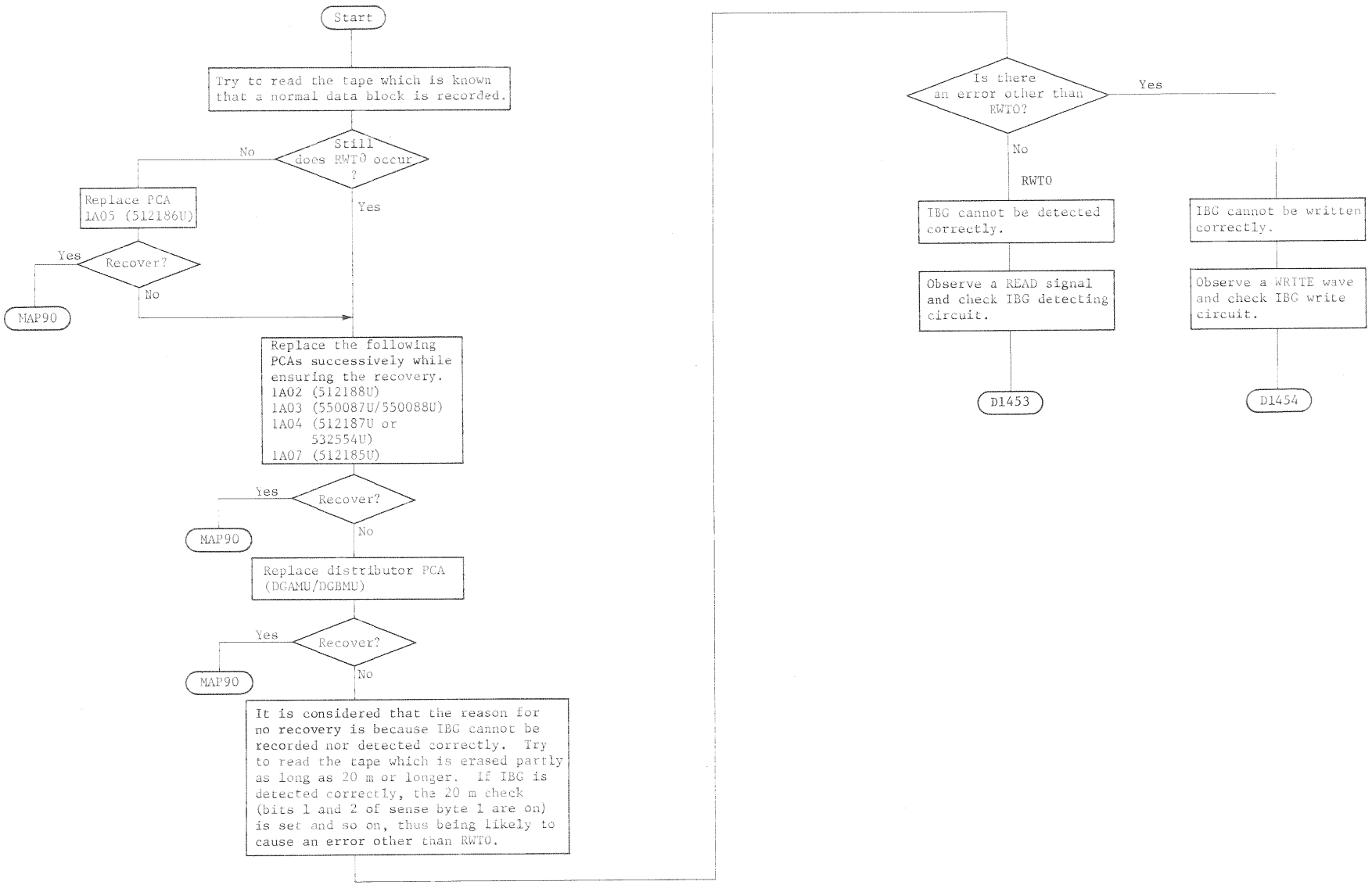
FRU1 (Sense byte 22) = 77

MPTRP (Sense byte 11, bit 6) .... ON

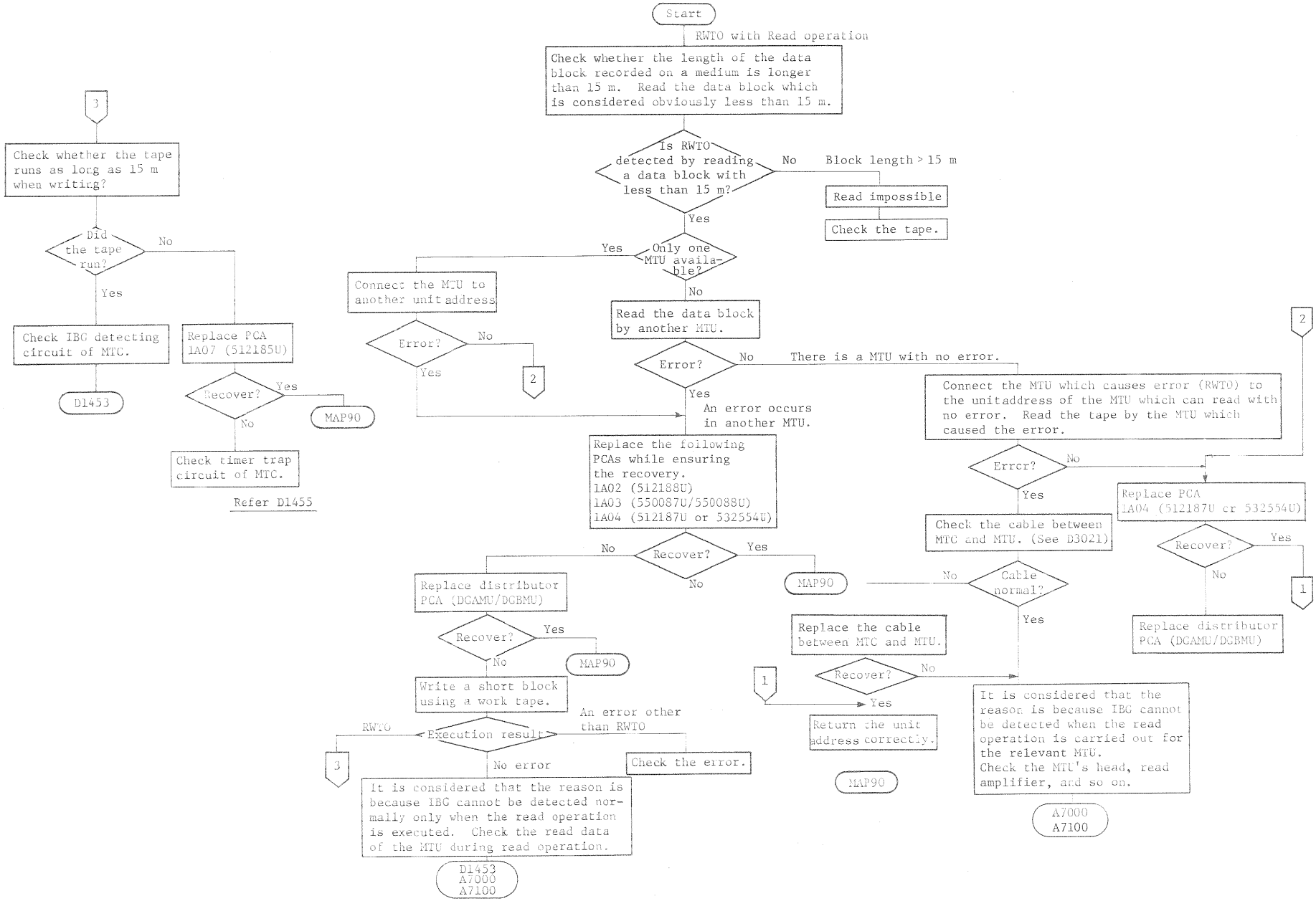
(2) In case a missing position (Sense byte 11, bit 1) is set and the time when an abnormality occurs in the tape mark search of the MTU is indicated. See D1460.



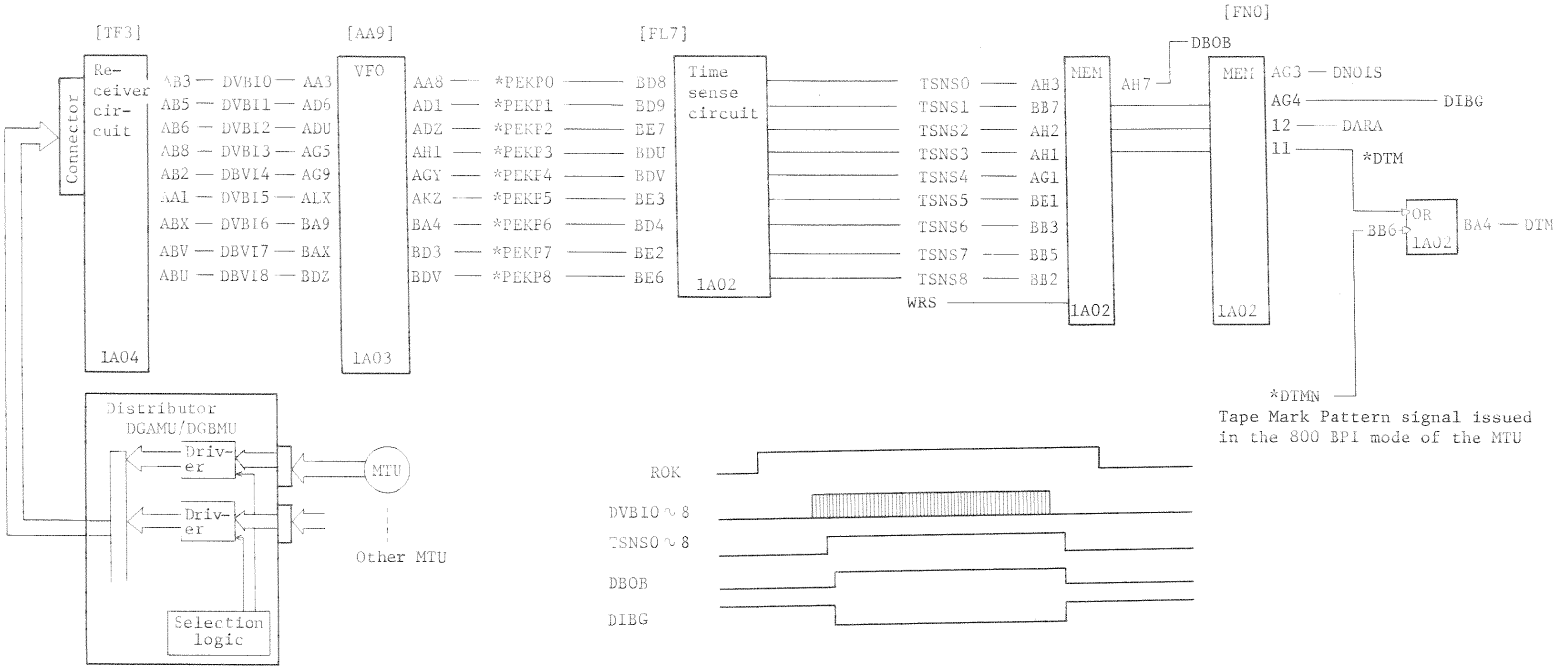
D1451	Read/Write Overrun - 2



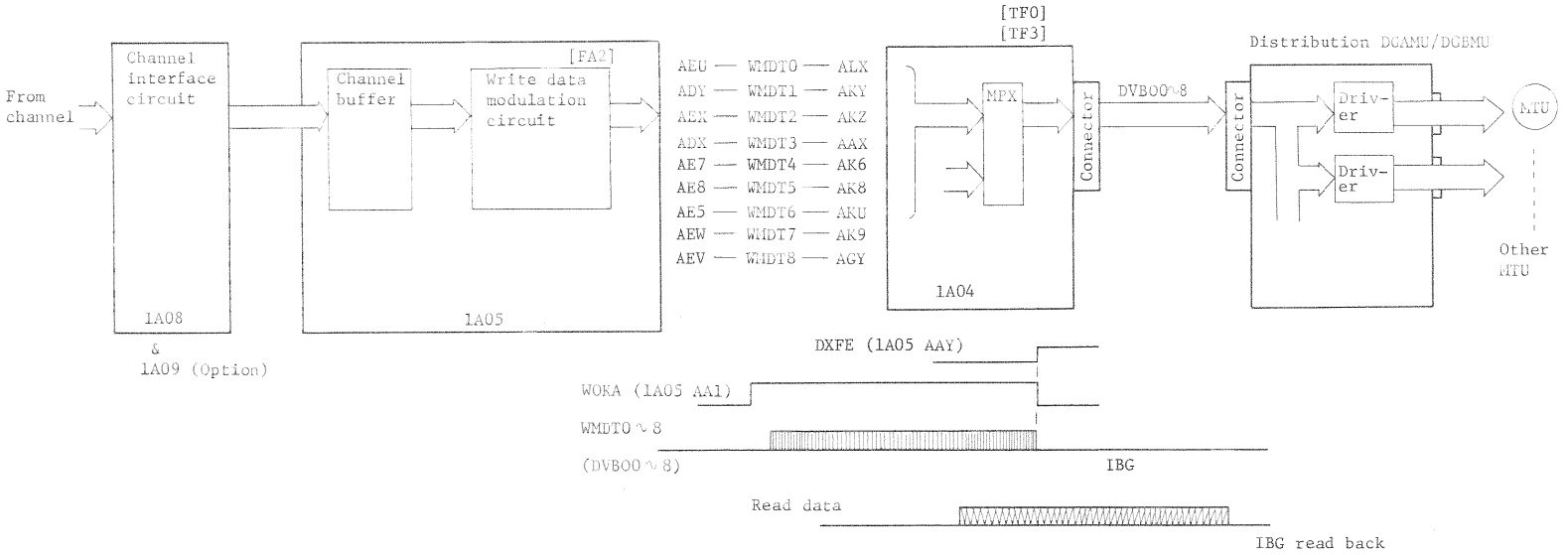
D1452	Read/Write Overrun - 3

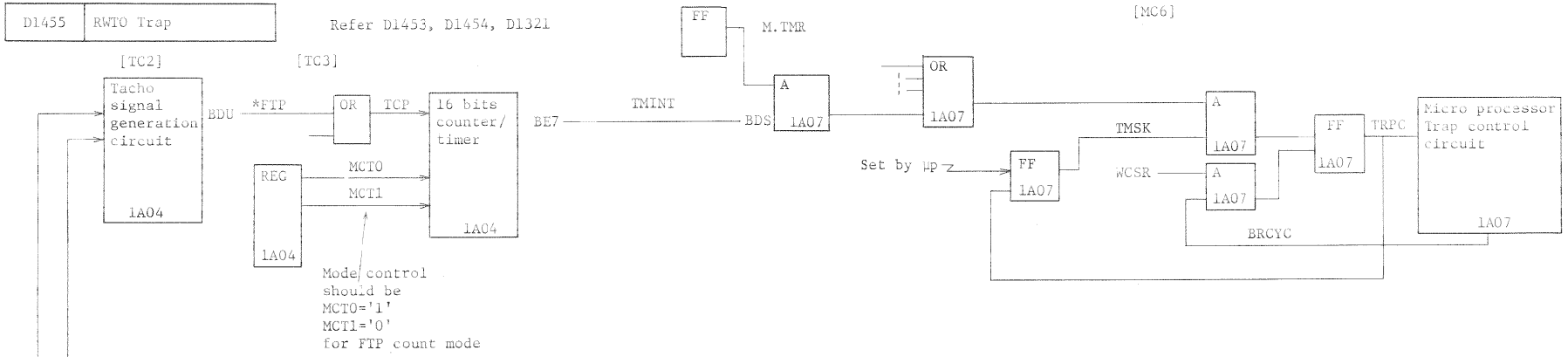


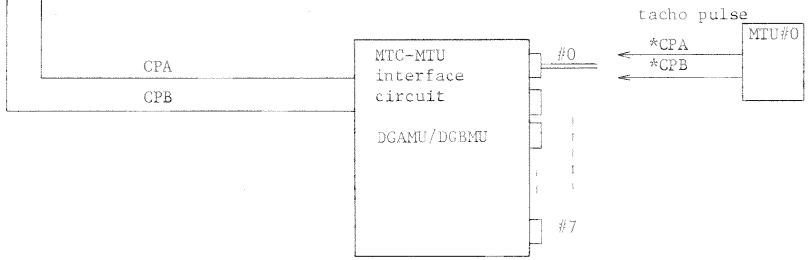
D1453	Time Sense Decode Circuit



D1454	Write Data Observation

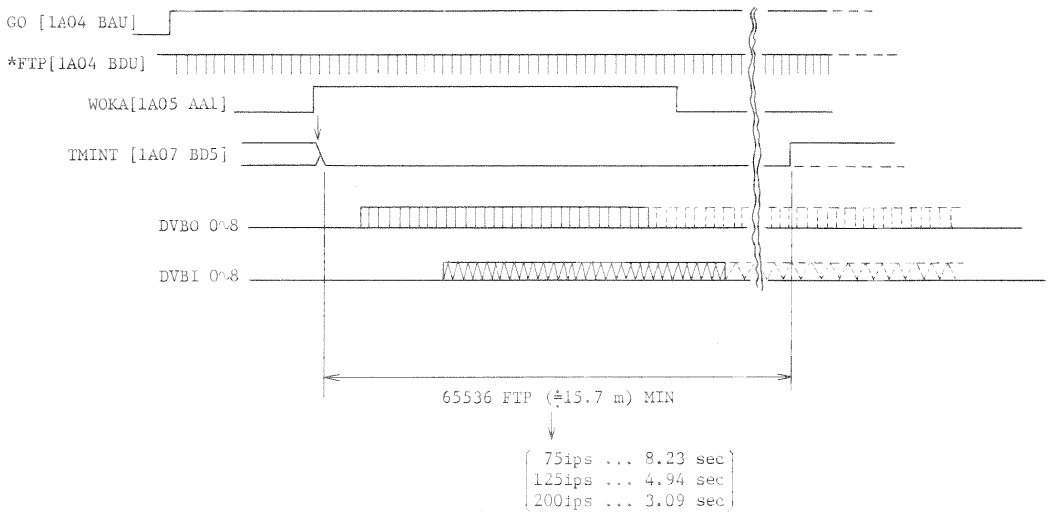






. FTP pulses, generated from CPA, CPB tacho signal, are counted by 16 bit counter. When the counter is overflow (65536 count), TMINT signal is generated and trap to the microprocessor occurs. If FTP signal has been generated correctly, the trap is taken place after 8.23/4.94/3.09 seconds elapsed in the 75/125/200 ips speed mode respectively.

Of course, GO signal to the MTU is turned off, if IBG has been detected before elapsing above seconds.



D1460	Missing Position - 1

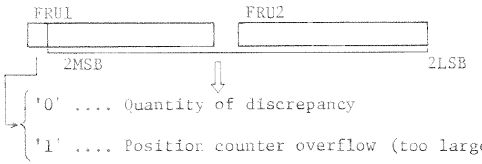
Generated in the following cases:

(1) When a data check error is generated in write, Read or Read Backward command operation, the information concerned with the length of block recorded in the operation is stored in communication register of MTU.

After that, for error recovery by retrying, the Back Space command corresponding to the Read and Write commands or the Space command corresponding to the Read Backward command is issued.

At that the space length associated with Space or Back Space command is compared with the error block length stored in communication register which is mentioned above. When the difference between both of the lengths is larger than the requirement, MISP (Sense byte 11, bit 1) is generated.

FRU1 (Sense byte 22) and FRU2 (Sense byte 23) provide a information of the length discrepancy.

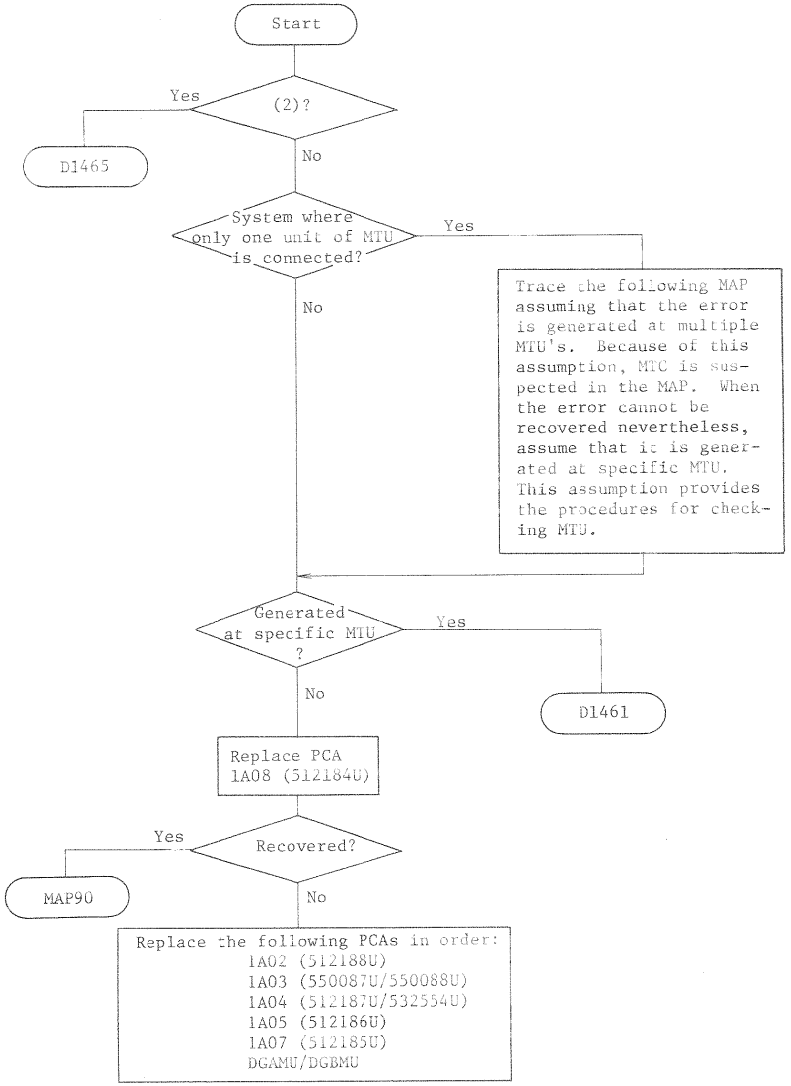


(2) After instructing MTU to search for Tape Mark Search in order to perform Space File or Back Space File command;

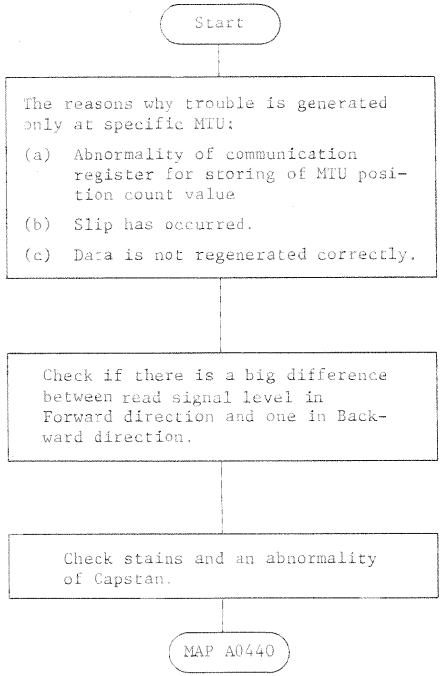
1) When Tape Mark block cannot be detected correctly, though MTU enters ready status.
(Bit 7 of TU Sense byte, Tape Mark, is 0.)

2) When MTU detects an interruption except BOT detecting and Tape overrun of the MTU.

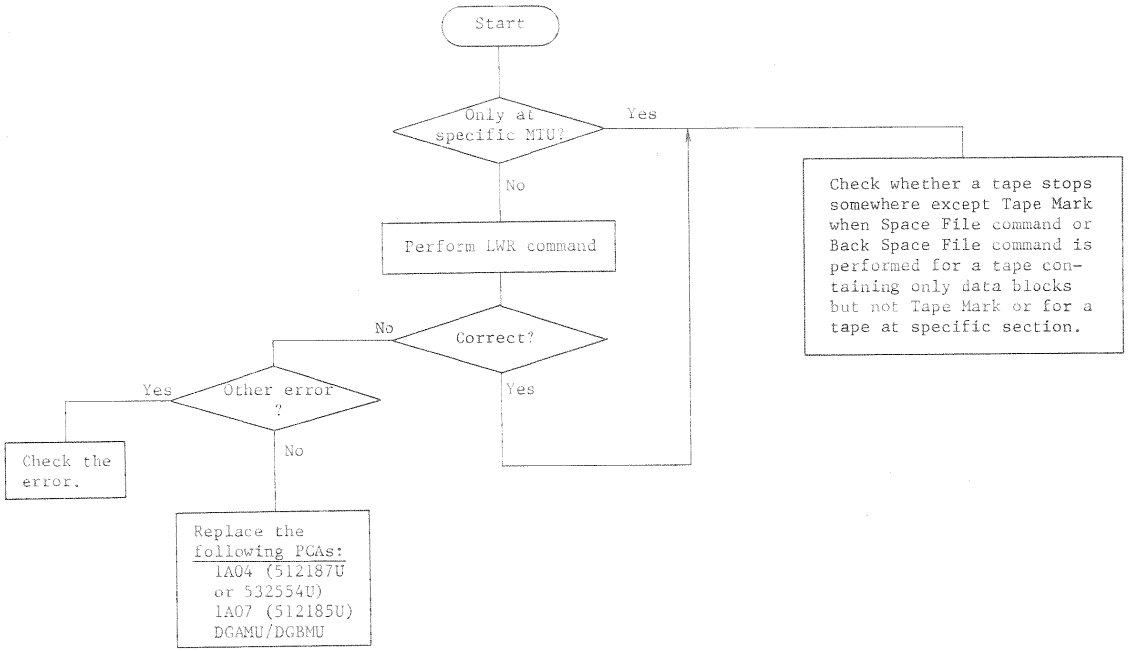
In this case, RWTO (Sense byte 11, bit 0) is also generated.



D1461	Missing Position - 2



D1465	Missing Tape Mark



D2000	Data Check

Data Check

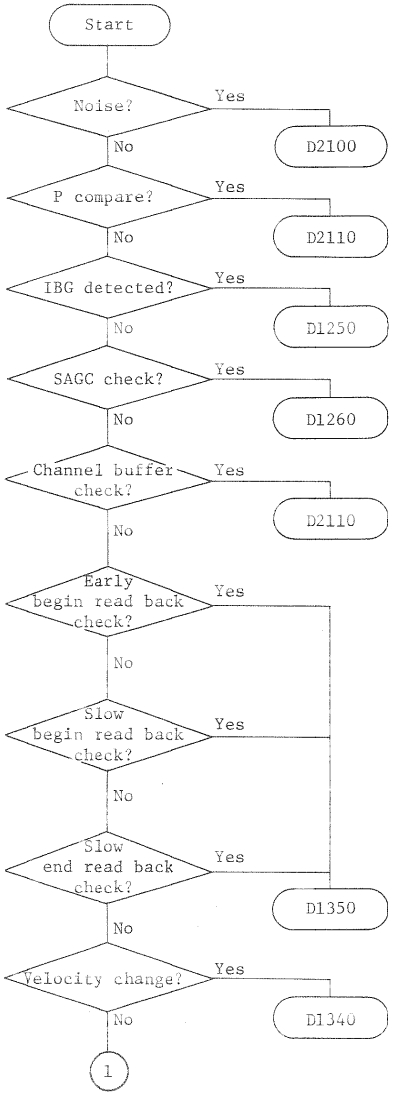
Data check occurs when the following error are detected:

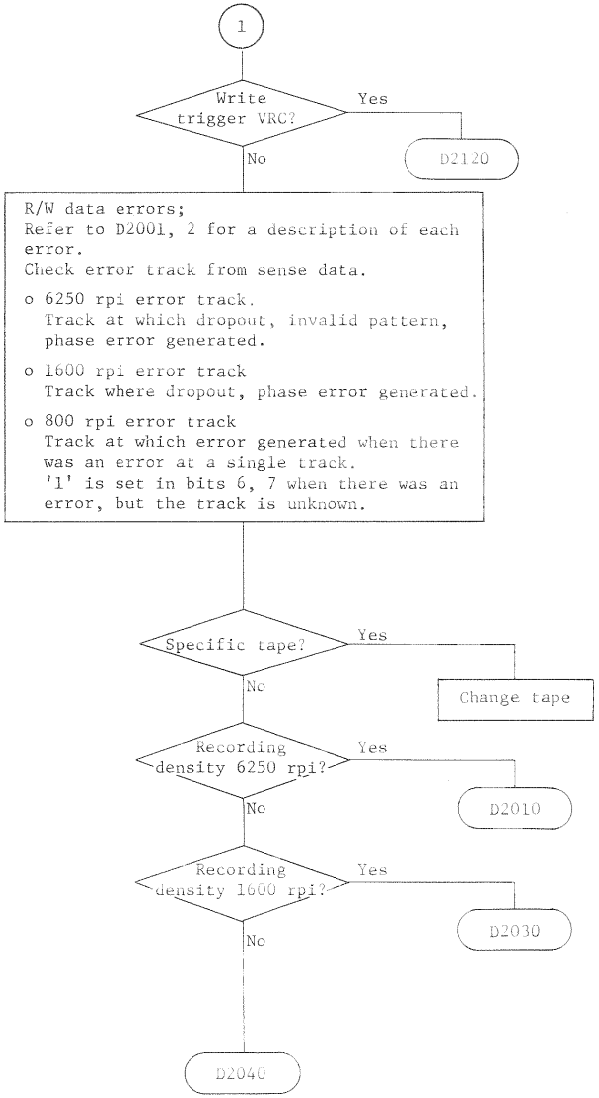
(1) R/W and internal circuit error

Noise	Sense byte	1 - 0
VRC error	"	3 - 0
Multiple track error/LRC error	"	3 - 1
Skew error	"	3 - 2
End data check/CRC error	"	3 - 3
Envelope check	"	3 - 4
P compare	"	3 - 7
Write trigger VRC	"	4 - 3
Start read check	"	5 - 4
Partial record	"	5 - 5
Postamble error	"	5 - 6
Error counter overflow	"	5 - 7
IBG detected	"	8 - 0
SAGC check	"	8 - 4
Channel buffer check	"	9 - 2
SRC III error	"	9 - 3

(2) Tape speed error

Early begin read back check	Sense byte	8 - 3
Slow begin read back check	"	8 - 5
Slow end read back check	"	8 - 6
Velocity change	"	9 - 1





D2001	Data Check Sense Byte Explanation - 1

o VRC error

(1) When recoverable VRC error generated at read, read backward command.

(2) When VRC error generated at write, LWR command.
(May have CRC error set also.)

o Multiple track error/LRC error

(1) When there is a pointer of 2 tracks or greater at 6250 rpi write, LWR command.

(2) When there is a pointer of 3 tracks or more at 6250 rpi read, read backward.

(3) When there is a pointer of 2 tracks or more at 1600 rpi read, read backward.

(4) When 800 rpi horizontal parity check error was generated.
(Error Track may have been reset by RESYNC at 6250 rpi read operation.)

o Skew error

(1) When excessive skew detected at 6250/1600 rpi read, read backward, write command.

6250 rpi write	RIC-ROC	2
1600 rpi write	RIC-ROC	14
6250 rpi read	RIC-ROC	30
1600 rpi read	RIC-ROC	15

(2) When excessive skew detected at 800 rpi write, write tape mark command.

o End data check/CRC error

(1) When postamble cannot be detected at 1600 rpi read operation. (No READEND)

(2) When CRC error detected at 6250/800 rpi read operation or read after write.

(3) When FORME (Format Error) detected at 6250 rpi operation.

o Envelope check

When drepout detected at 1600 rpi/6250 rpi write operation.

Note: Envelope check does not cause Data check at 6250 rpi operation.

Note: Use D2010 - D2020 for 6250 rpi
Use D2030 - D2032 for 1600 rpi
Use D2040 - D2041 for 800 rpi

D2002	Data Check Sense Byte Explanation - 2

- Start read check

  (1) When IBG encountered before data part detected after block detected at 6250/1600rpi operation.

  (2) When data part not detected within the prescribed time after block detected at 6250/1600rpi operation.

- Partial record
  When IBG encountered in data at 6250/1600rpi.

- Postable error
  When abnormality detected in postable at 6250/1600rpi.

- IBG detected
  When IBG detected while reading data part at 6250/1600rpi write command.

D2003	Explanation about CRC III Error

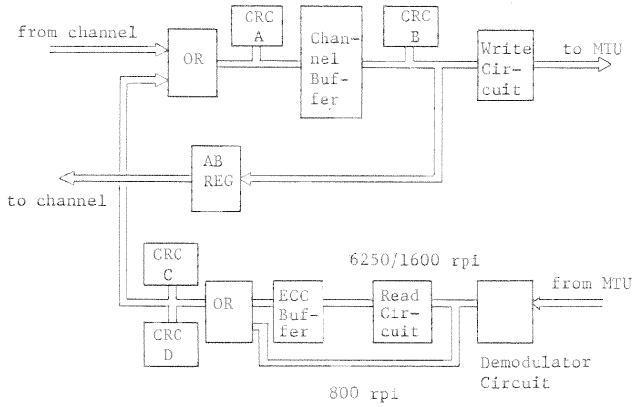
o CRC III error

(1) When CRC-B byte and CRC-D byte didn't match at 6250 rpi write, read command.

(2) When CRC-C byte not expected pattern at 6250 rpi read backward.

(3) When CRC-B byte and CRC-C byte didn't match at 1600/800 rpi write command.

-------- CRC error set --------



CRC Generation Circuit

MODE	6250 rpi	1600/800 rpi	Sense
Write	A ≠ B	A ≠ B	Channel Buffer Check
	B ≠ D	B ≠ C	CRC III Error
Read	A ≠ B	A ≠ B	Channel Buffer Check
	B ≠ D	-	CRC III Error
Read Backward	A ≠ B	A ≠ B	Channel Buffer Check
	C≠Match pattern	-	CRC III Error

° CRCA : A.CRC pattern is generated from channel buffer input.

° CRCB : A.CRC pattern is generated from channel buffer output.

° CRCC : A.CRC pattern is generated from read data.

° CRCD : Set A.CRC of read data at 6250 rpi.

o When CRCIII error or P Compare error is indicated in the sense bytes, FRU1 and FRU2 described below may be indicated together.

FRU1 (Sense byte 22)

0	1	2	3	4	5	6	7
'0'	'0'	'0'	'1'	(BOPC)	ABRPC	DBCK	(WVRC)

This code indicates that detailed CRC information stored on FRU1, bit 4~7, and FRU2 successfully.

A/B Reg parity error.

Deskewing buffer check

FRU2 (Sense byte 23)

0	1	2	3	4	5	6	7
*MCRC	*MCRCZ	EP≠CR	B≠D	B≠C	*MCRCC	A≠B	XBiC

content of CRCST register

o *MCRC

Not match CRC; "1" when CRC pattern generated as a result of read operation is not normal.

o *MCRCZ

Not match CRC zero; "1" when CRC pattern generated as a result of read operation is not all '0'.

o EP≠CR

"1" when CRC pattern does not match EP (error pattern) register.

o B≠D

"1" when CRCD does not match CRCB.

o B≠C

"1" when CRCB does not match CRCC.

o *MCRCC

Not match CRCC; "1" when CRC pattern obtained from read data excluding CRC byte is not normal.

o A≠B

"1" when CRCA does not match CRCB.

o XBIC

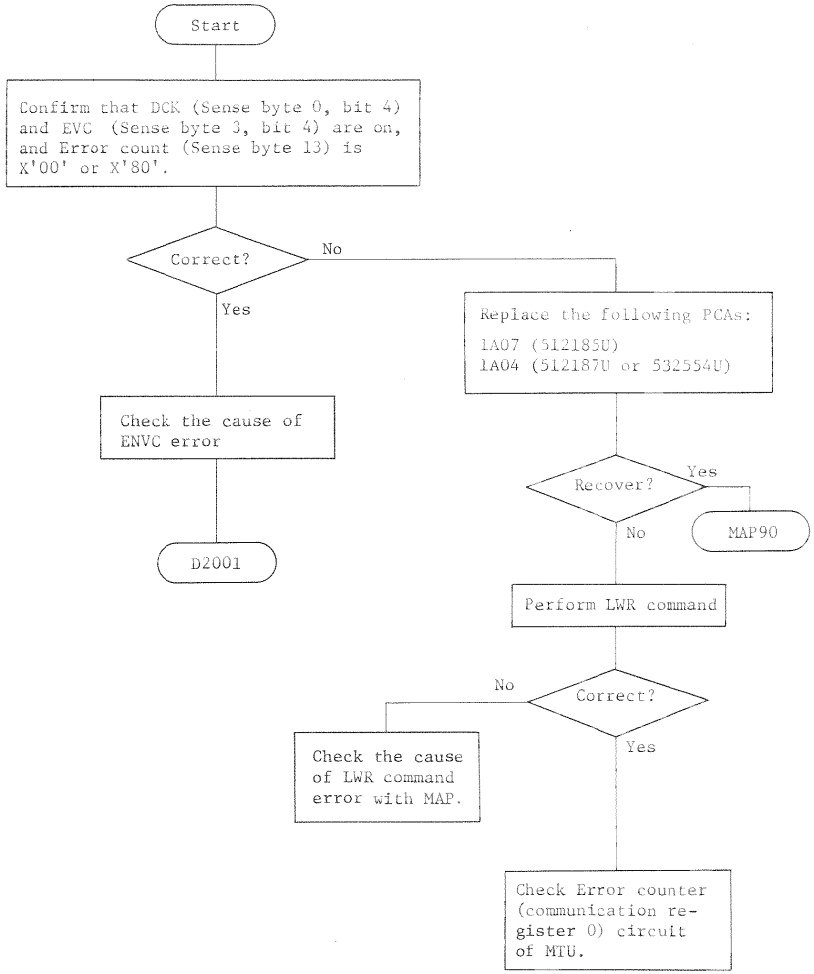
Transfer buffer bus in check, "1" when illegal XFR Buffer input data is applyed.

D2004	Error Count Overflow

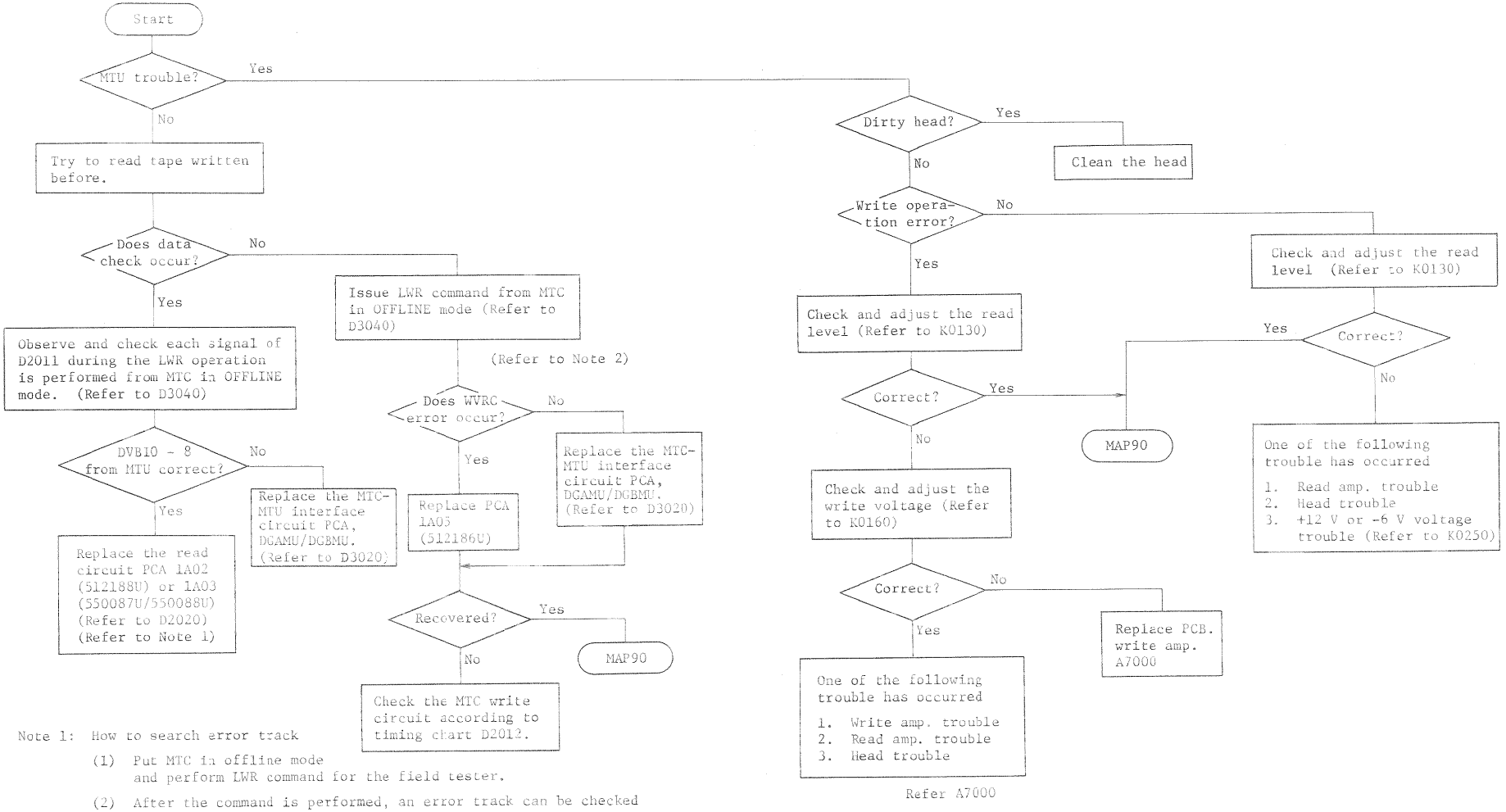
The error counter is incremented, if DCK and EVC (Envelope check: Sense byte 3, bit 4) are generated as a result of performing the write operation in 6250/1600 rpi mode. When performing write operation in 6250 rpi mode, if the error counter reaches X'00' or X'80', ECOVF (Error Counter Overflow: Sense byte 5, bit 7) is generated.

That is, ECOVF is generated each time 128 EVC errors are detected.

The error counter is provided for each MTU.



D2010	6250 rpi Data Check - 1



Note 1: How to search error track

(1) Put MTC in offline mode and perform LWR command for the field tester.

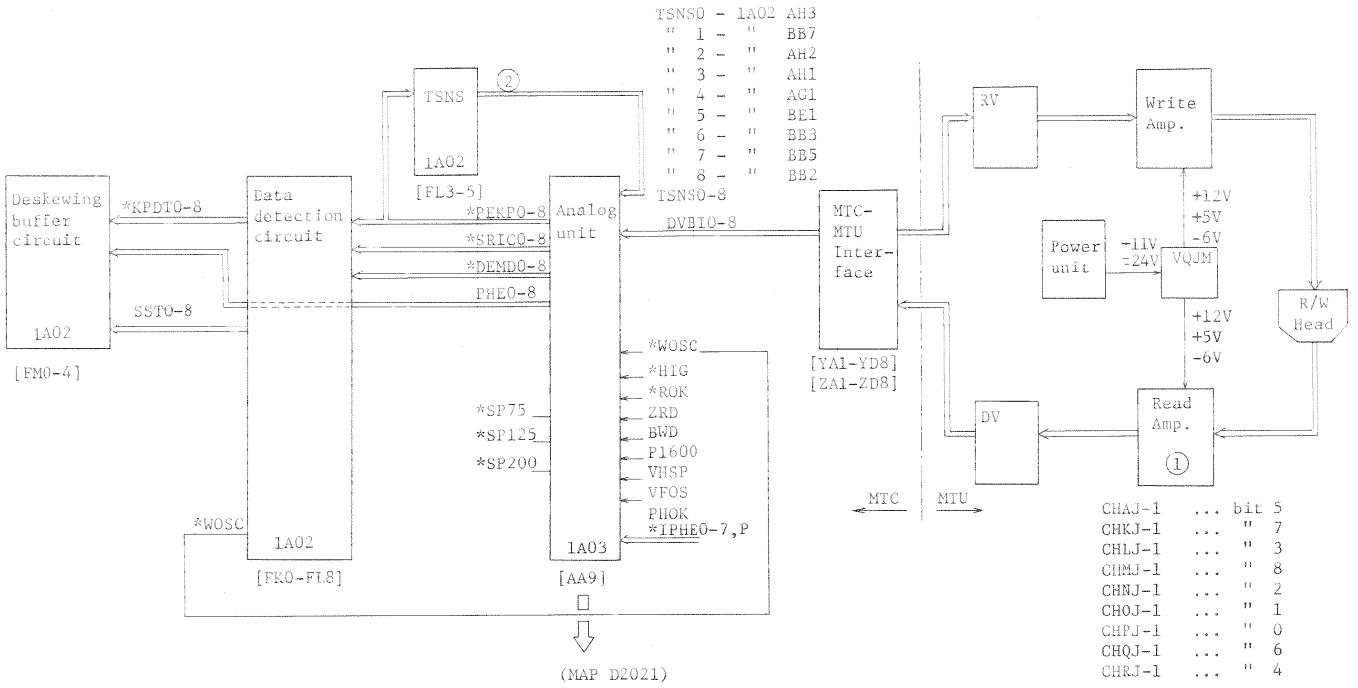
(2) After the command is performed, an error track can be checked by displaying the register at X'22' in the microprogram.

Note 2: How to search WVRC error

(1) Display the contents of the register at X'24' in the microprogram by the field tester.

(2) Bit 3 means WVRC.

D2011	6250 rpi Data Check - 2

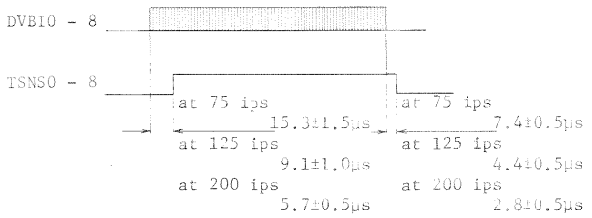


① 

Check the wave-form during write by Field Tester. (K0130)

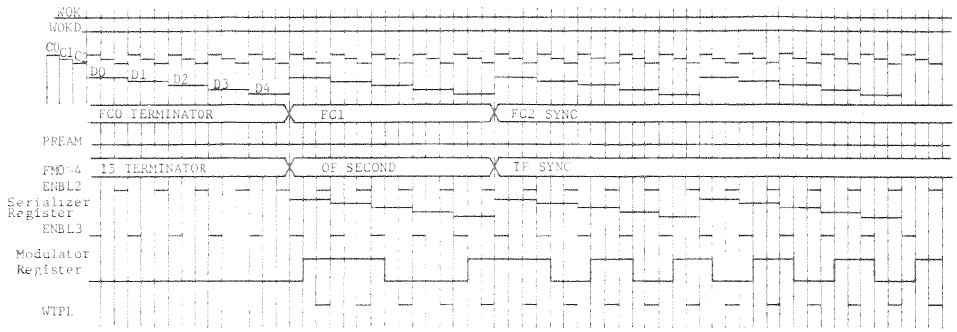
1) Set 9042 fci (GCR mode) after being 3200 fci (PE model) ... V ⩾ 1.0V for a few seconds.
2) Set 9042 fci after set ..... V = 2.0V±15% SAGC.
3) Perform the tape running backward which is written ..... V ⩾ 1.0V in 9042 fci.

②

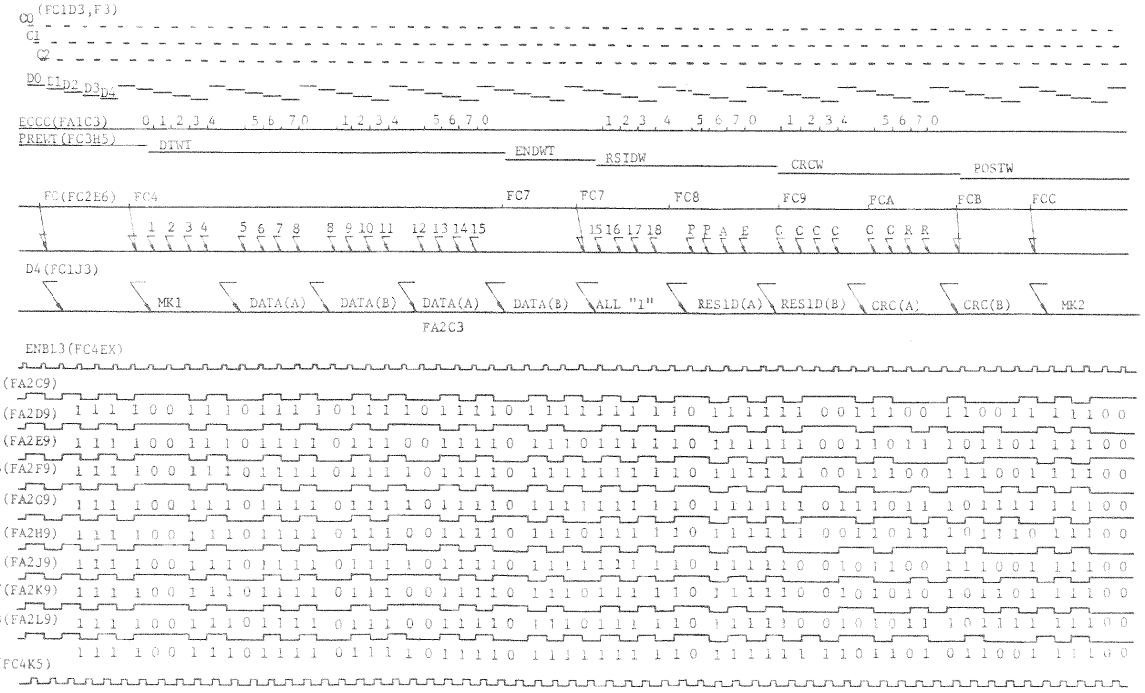


D2012	6250 RPI Write Time Chart

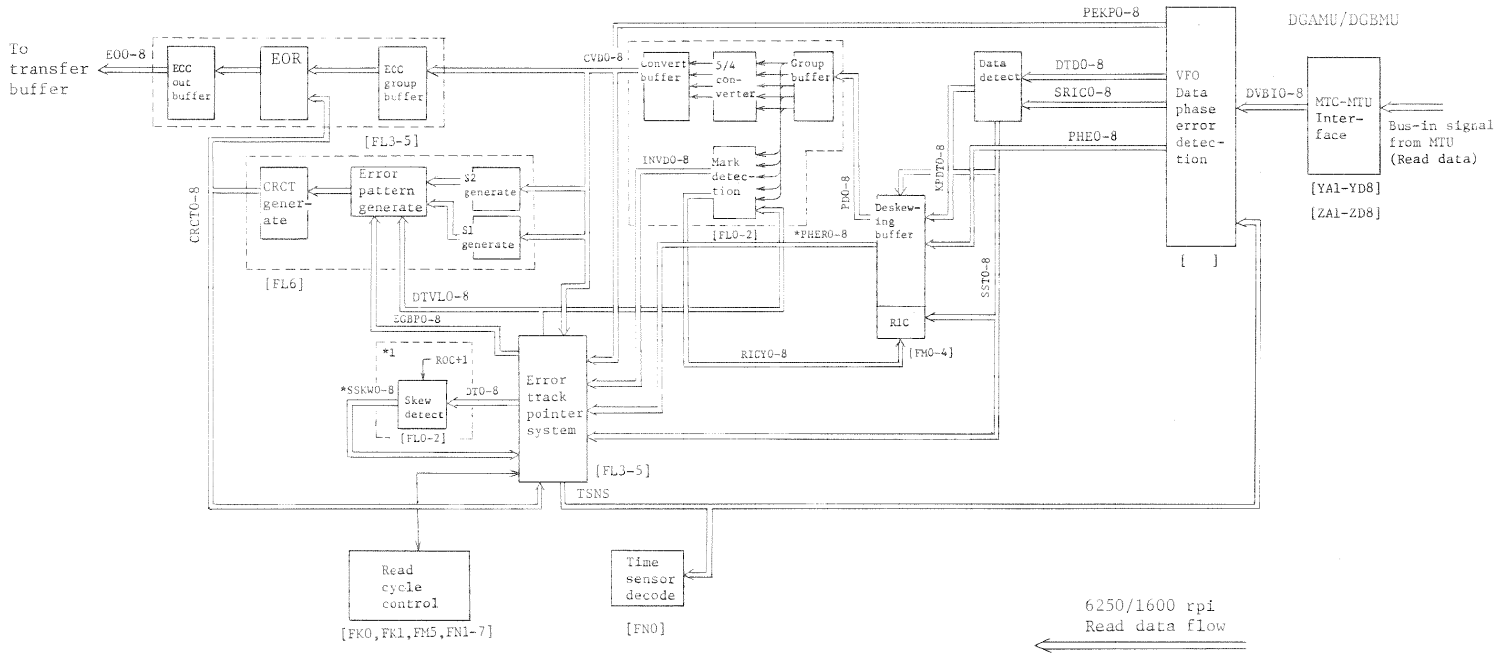
6250RPI Write Time Chart



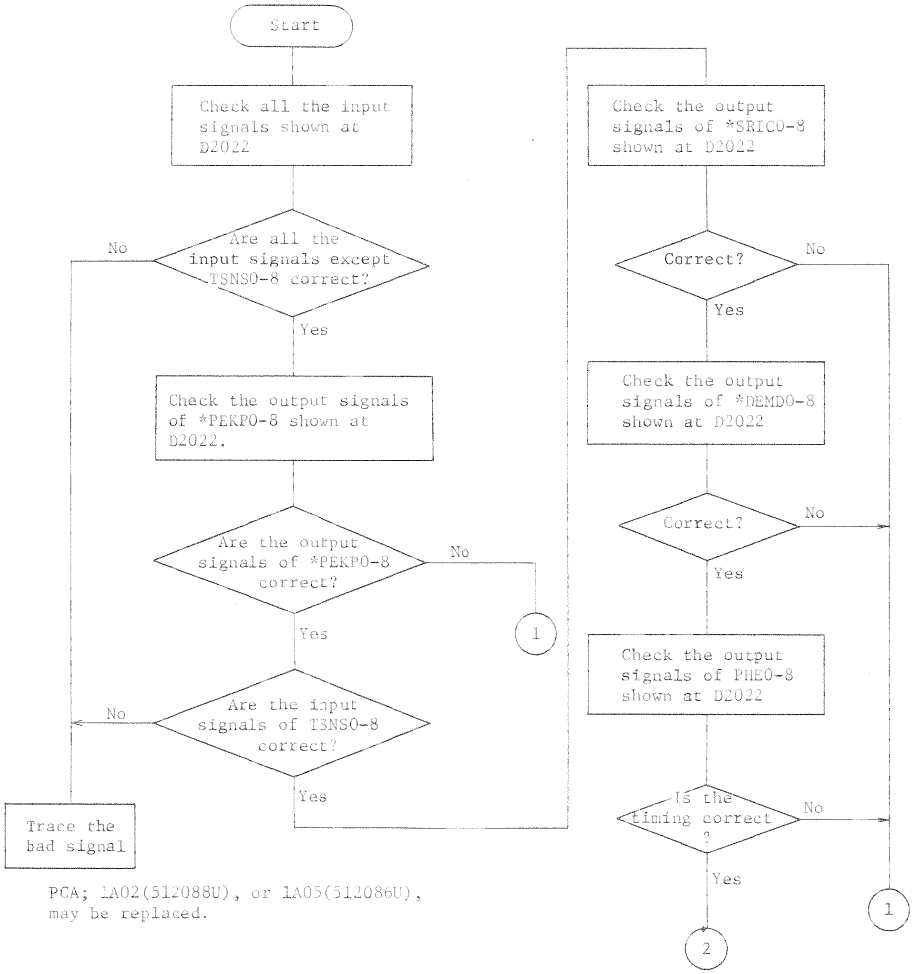
200ips 104μs
125ips 295μs
75ips 495μs



D2020	Read Data Flow and the Performance of PCB (6250/1600 rpi)



D2021	Demodulation Circuit Trace Flow - 1



PCA; 1A02(512088U), or 1A05(512086U), may be replaced.

Demodulation circuit;

DEAA (550088U) ..... for 200/125 ips
DEBA (550087U) ..... for 125/75 ips

D2022	Demodulation Circuit Trace Flow - 2

Demodulation Circuit

1. Input Signals

Table 1 Input signals

Item	Signal name	Contents	Bit 0	1	2	3	4	5	6	7	8	Reference
1	Peak Signal (DVBI0∿8)	Read peak position signal from MTU	AA3	AD6	ADU	AG5	AG9	ALX	GA9	BAX	BDZ	Fig. 1 Table 3
2	Time Sense (TSNS0∿8)	VFO input changing signal	AAU	AAV	ADY	AHZ	AK1	AKV	BA6	BD5	BD6	Fig. 3
3	Error Generated Signal (IPHE0∿8)	Signal generating suspected error	AB7	AD3	AEV	AH7	AHW	BB1	BB3	BE2	BEW	Ordinarily +2.4 V∿ +5.0 V
4	Read OK (*ROK)	Read start signal	AL7									Fig. 3
5	Z Read (ZRD)	Signal indicating 800 bpi	AK6									--------
6	Backward (BWD)	Signal indicating tape running direction	AL6									--------
7	Write Clock (*WOSC)	Clock signal of basic frequency	AKU									Fig. 2 Table 3
8	VFO Start (*VFOS)	Signal to reset VFO and start	AK8									Fig. 3
9	Speed Signal (*HSP)	Signal indicating tape speed	AL3									--------
10	1600 Signal (P1600)	Control signal indicating record density	AL5									--------
11	High Gain Signal (*HIG)	Signal changing VFO gain	BB5									Fig. 3 Table 4
12	Phase OK (PHOK)	Signal to start data demodulation	AK4									Fig. 3

2. Output Signals

Table 2 Output signals

Item	Signal name	Contents	Bit 0	1	2	3	4	5	6	7	8	Reference
1	Peak Pulse (*PEKP0∿8)	Rising and falling pulses of peak signal	AA8	AD1	ADZ	AH1	AGY	AKZ	BA4	BD3	BDV	Fig. 1
2	Read Clock (*SRIC0∿8)	Clock to get demodulated data	AA6	ABX	AD8	AEX	AGX	ALB	BB7	BAV	BEU	Fig. 4
3	Demodulation Data (*DEMD0∿8)	Data recognized with 1 and 0	AB3	AE6	ADV	AH5	AHU	AKY	BBU	BZY	BDX	Fig. 4
4	Phase Error (PHE0∿8)	Phase error detected signal	AA5	AAX	AEW	AG4	AGV	ALW	BA1	BD1	BD8	Fig. 5
5	*SP200 *SP125 *SP75	Signal indicating speed function of VFO	AE1 AK3 AK5									--------

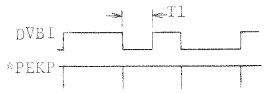


Fig. 1 DVBI and PEKP

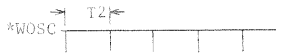


Fig. 2 WOSC

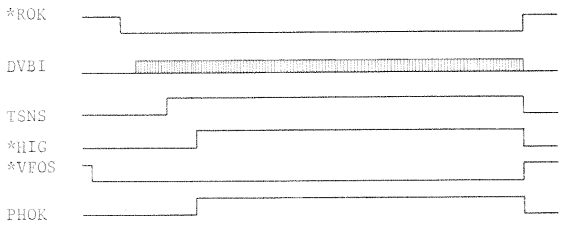


Fig. 2 Input timing

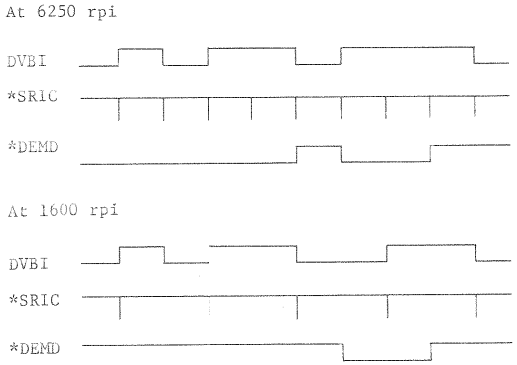


Fig. 4 Output timing

Table 3 Cycle of T1 and T2

Record density	Tape speed	T1 and T2
6250 rpi	200 ips	555±100 ns
	125 ips	885±180 ns
	75 ips	1475±300 ns
	50 ips	220±0.5 μs
1600 rpi	200 ips	1.56±0.3 μs
	125 ips	2.50±0.5 μs
	75 ips	4.20±0.8 μs
	50 ips	6.25±1.3 μs

Table 4 HIGH GAIN

Record density	Write/Read	*HIG
6250 rpi	Write	+2.4∿+5.0 V
	Read	Fig. 3
1600 rpi	Write, Read	+2.4∿+5.0 V

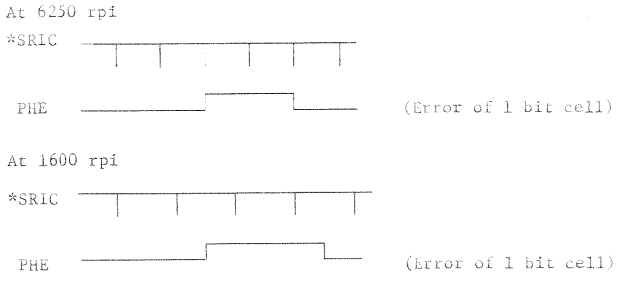
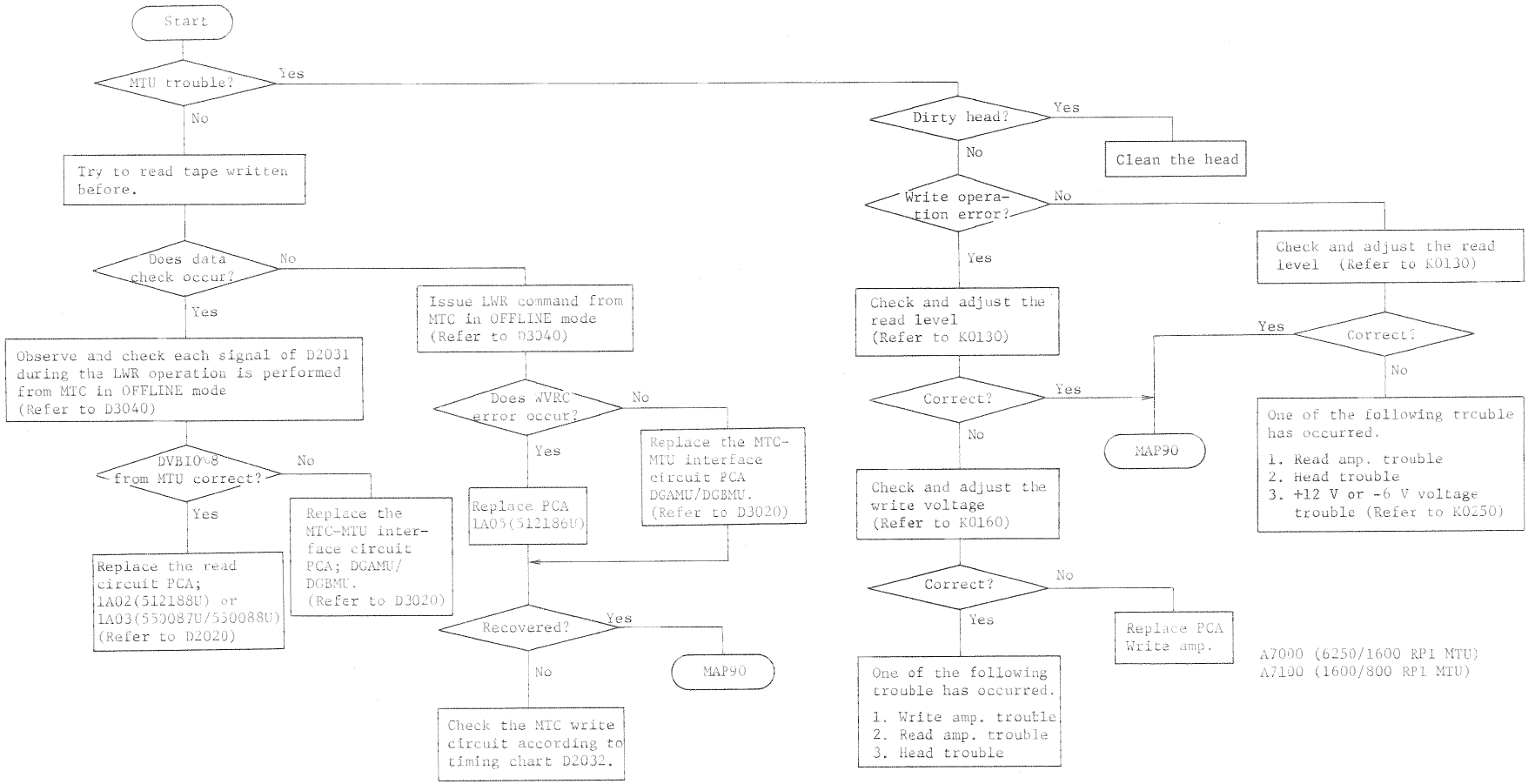


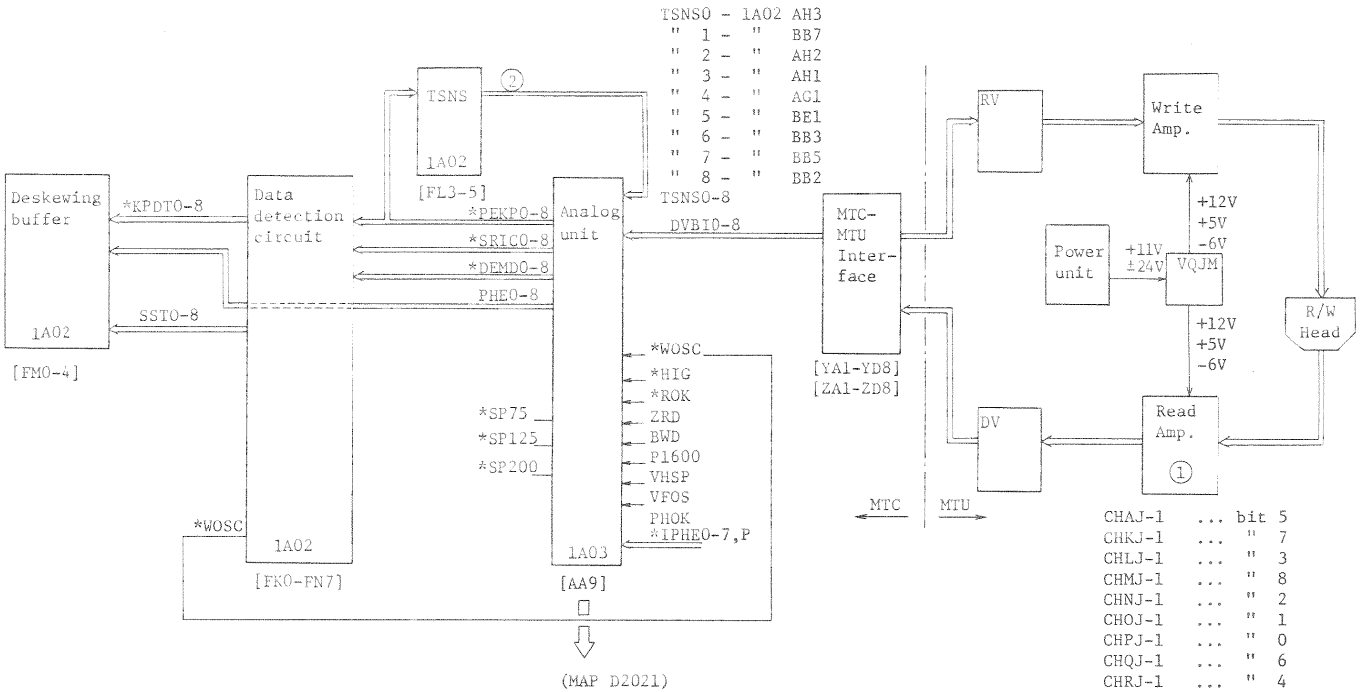
Fig. 5 PHE timing

D2030	1600 rpi Data Check - 1

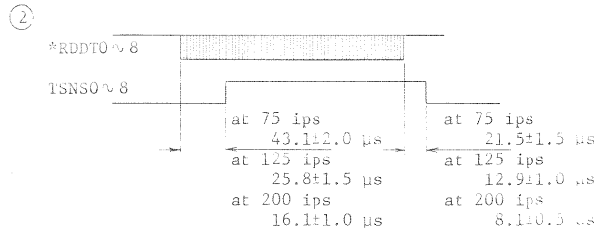


A7000 (6250/1600 RPI MTU)
A7100 (1600/800 RPI MTU)

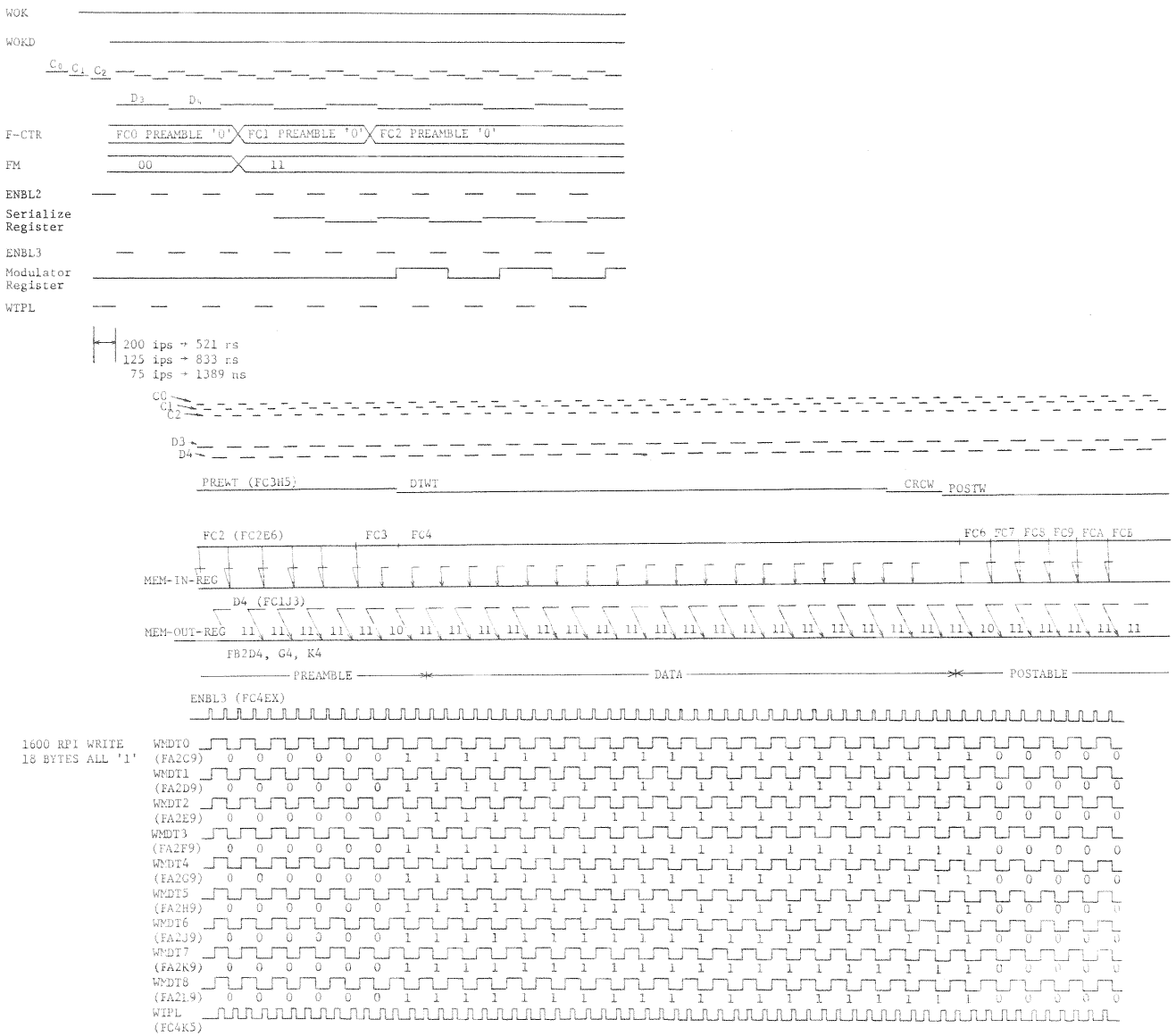
D2031	1600 rpi Data Check - 2



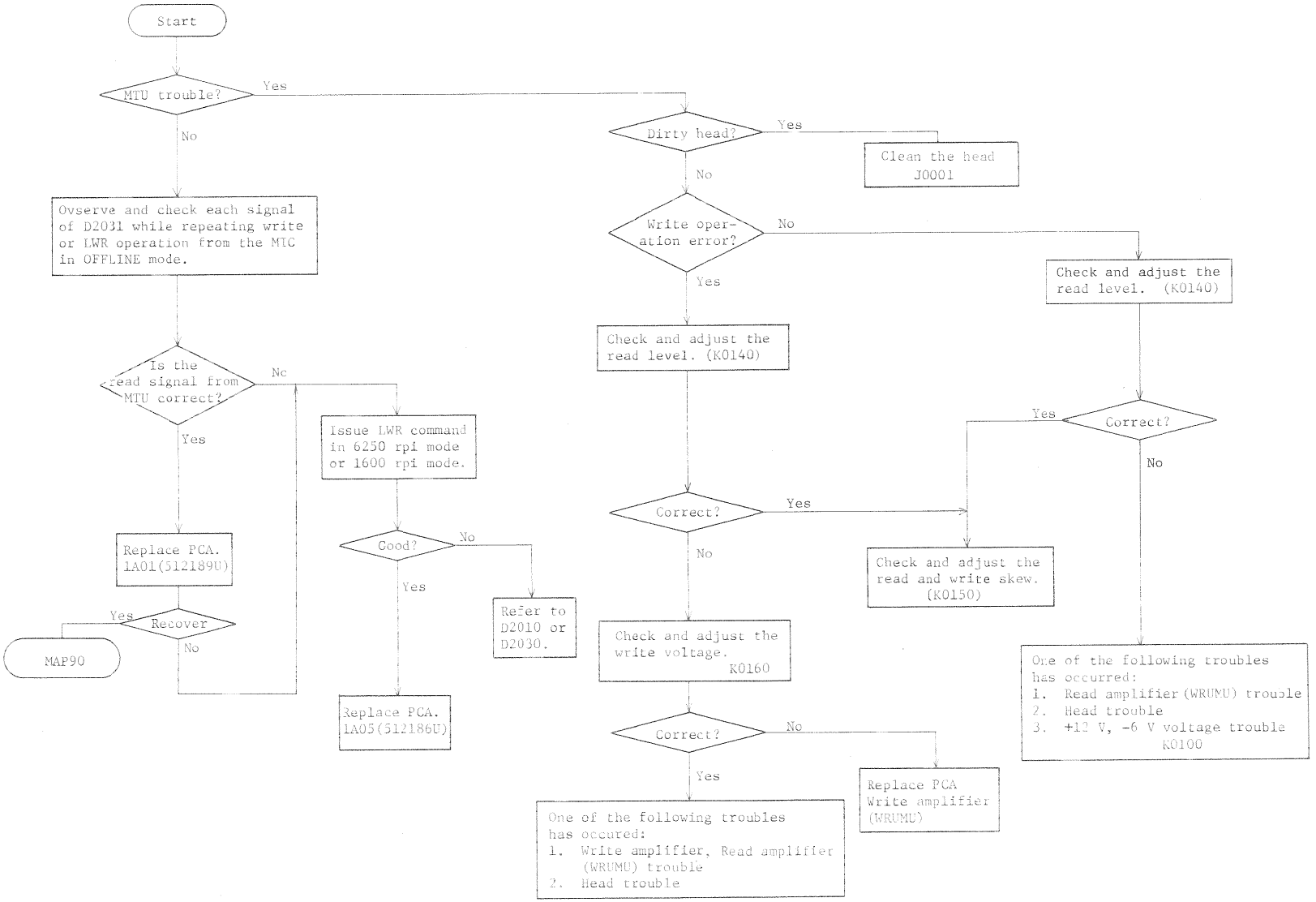
Check the waveform during write in 3200 fci (PE mode) by Field Tester.
(K0130, K1040)



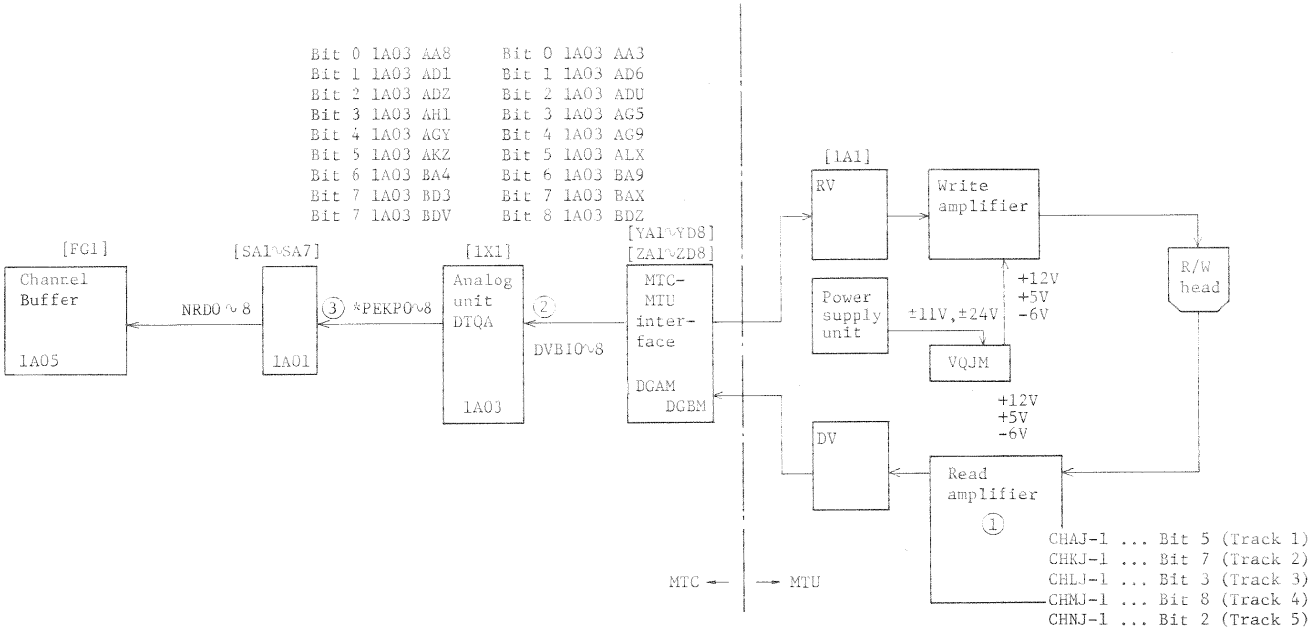
D2032	1600 rpi Write Time Chart

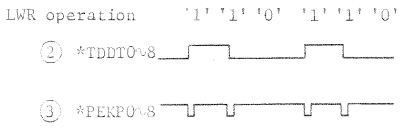


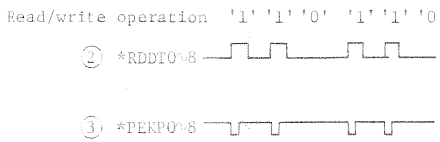
D2040	800 rpi Data Check - 1

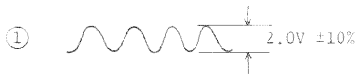


D2041	800 rpi Data Check - 2







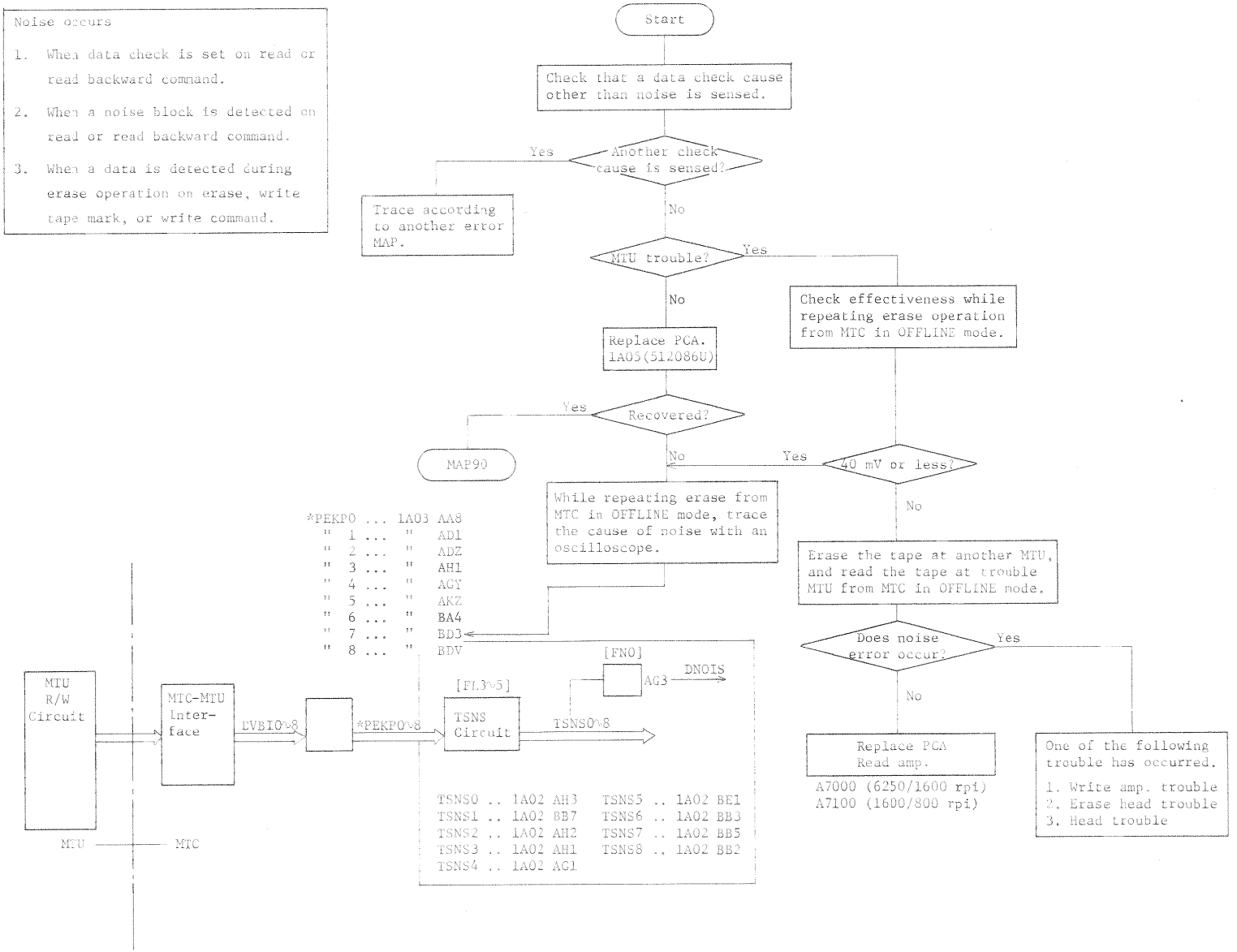


Observe the wave form while repeating the write operation in 800 fci (NRZI mode) from the field tester.

D2100	Noise

Noise occurs

1. When data check is set on read or read backward command.
2. When a noise block is detected on read or read backward command.
3. When a data is detected during erase operation on erase, write tape mark, or write command.



D2110	P Compare (Channel Buffer Check)

P compare means MTC parity check or compare check.
It occurs in the following cases.

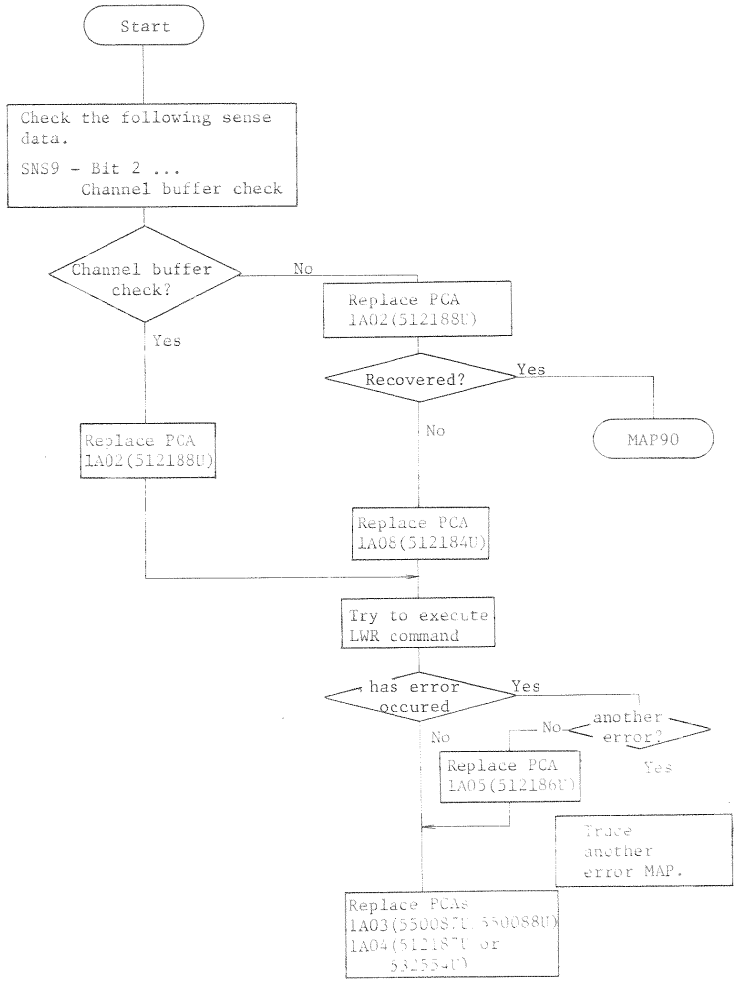
1. Channel buffer check
   When the comparison between channel buffer input and output data does not agree. (CRCA ≠ CRCB)

2. Parity check channel buffer
   When a parity error is detected in the channel buffer input data.

3. A/B register error
   When a parity error is detected in the A/B register at read operation.

4. Deskewing buffer check
   When an error is detected in the ROC of deskewing buffer.

Refer D2003 for FRU1,2.



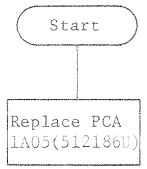
D2120	W-VRC Error

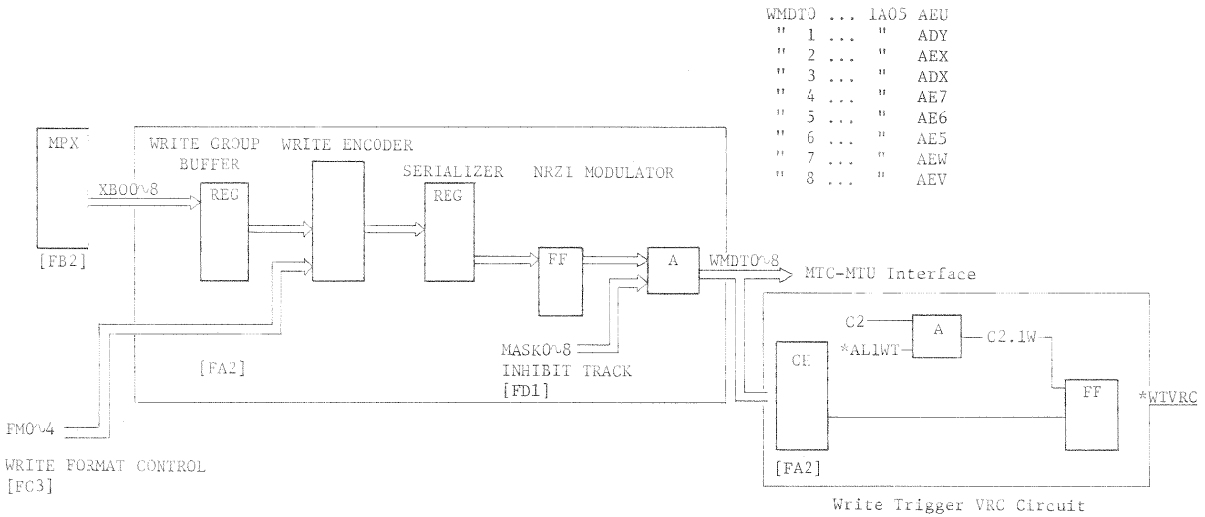
1. When parity error occurs in WTD0~8 at Write Trigger VRC Circuit.

   In this case "IBG detected" is not set.

2. When writing on creased tape.

   In this case "IBG detected" is also set.



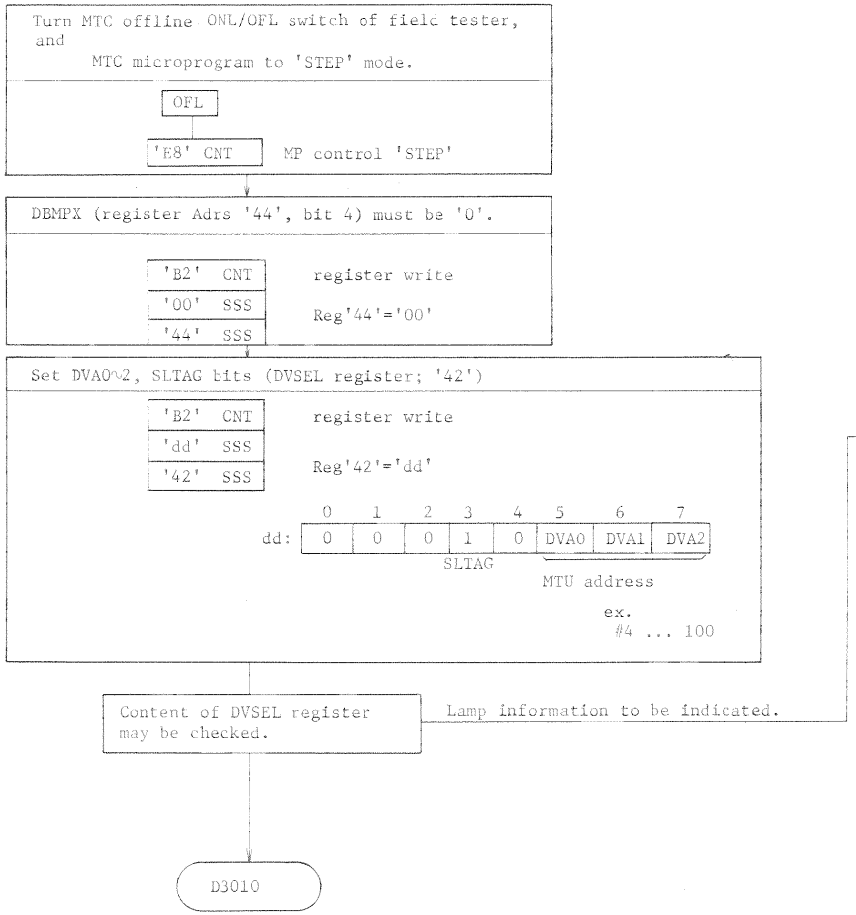


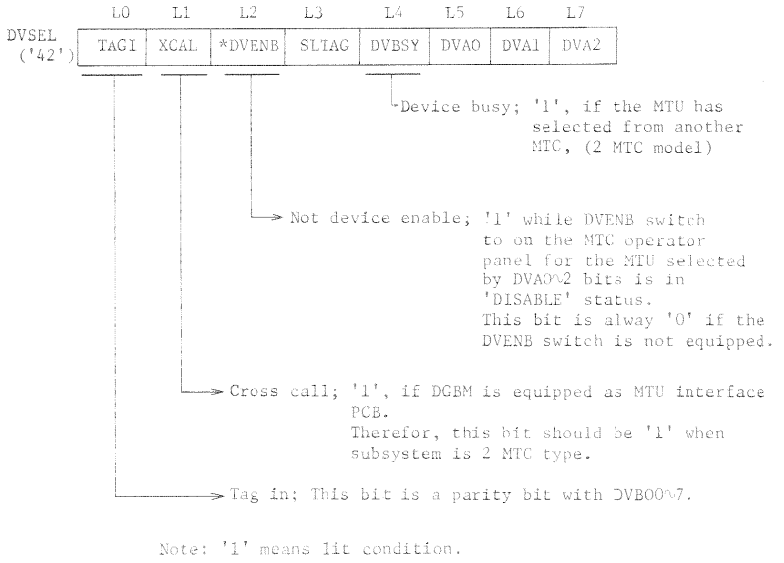
D3000	MTU Sense Abnormality

Field tester allows to confirm or manupulate the MTU status.
Various MTU status, e.g., BWD, NOT-FP, TWA or BOT, WRS, ONL, READY ... etc, can be displayed on field tester and checked.

MTU sense bytes representing those MTU status are showed in D3010, Table 1.

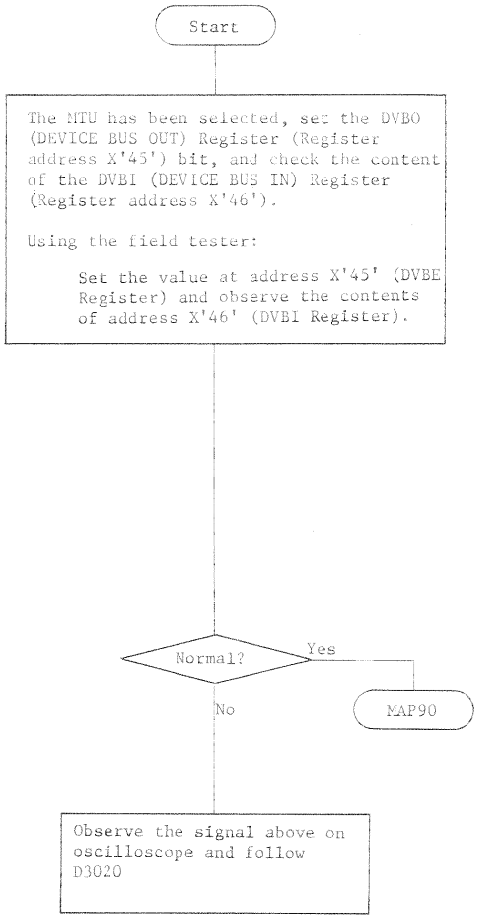
To inspect TU sense bytes, following manupilations should be done.





Note: '1' means lit condition.

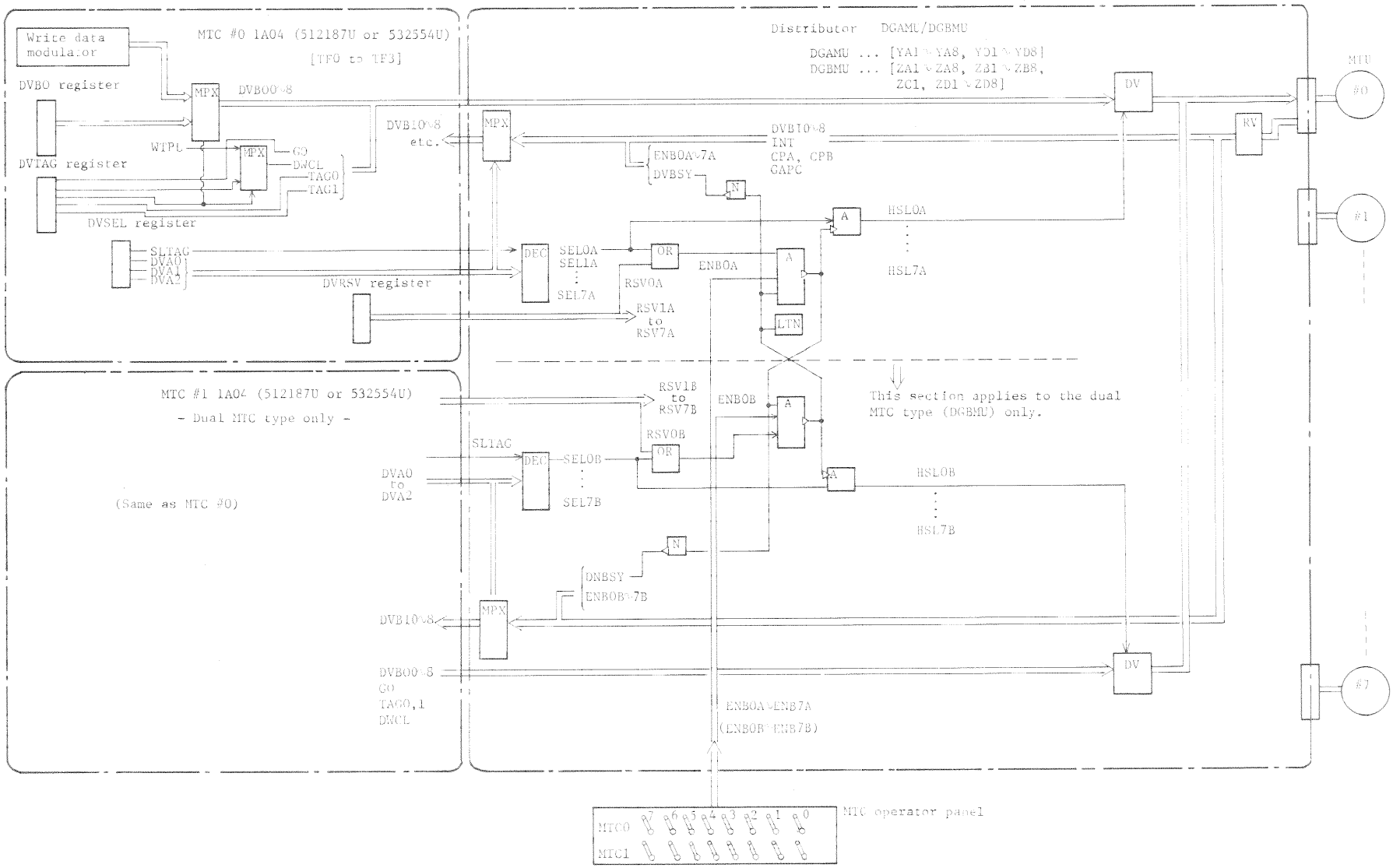
D3010	MTU Sense bytes configuration



TU sense byte	0	1	2	3	4	5	6	7	8
Bus-out bb: / Bus-in	'01' ('00')	'02'	'04'	'08'	'10'	'20'	'40'	'80'	'14'
Bit 0	BWD	New function	MISC error	VEL 0	2^7	SAGC count 0	Read data 0	Error code 0	Handler erase current ON
Bit 1	NOT FP	RESET key	Tape loop alarm left	VEL 1		" 1	" 1	" 1	Handler action
Bit 2	TWA	DSE	Tape loop alarm right	Ready hold	Tape unit unique ID low order	" 2	" 2	" 2	Handler backward status
Bit 3	BOT	7 tracks	ROM parity error	2^{12}		" 3	" 3	" 3	Handler write current ON
Bit 4	Write status	Test mode	Write circuit alarm	2^{11}		EC level 2^3 (Model conversion)	" 3	" 4	Handler 65% slice
Bit 5	ONLINE	Dual density	Fuse alarm	Tape unit unique ID high order		EC level 2^2	" 5	" 5	Handler over run
Bit 6	TU CK	High density	Air bearing alarm			" 2^1	" 6	" 6	Handler PE mode
Bit 7	READY	6250	Load failure	2^8	2^0	" 2^0	" 7	" 7	Tape mark
Bit 8	TAG-IN	TAG-IN	TAG-IN	TAG-IN	TAG-IN	TAG-IN	" 8	TAG-IN	TAG-IN

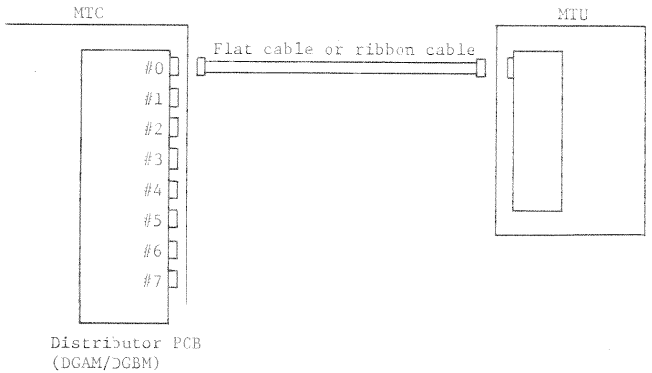
Table 1. MTU Sense Bytes

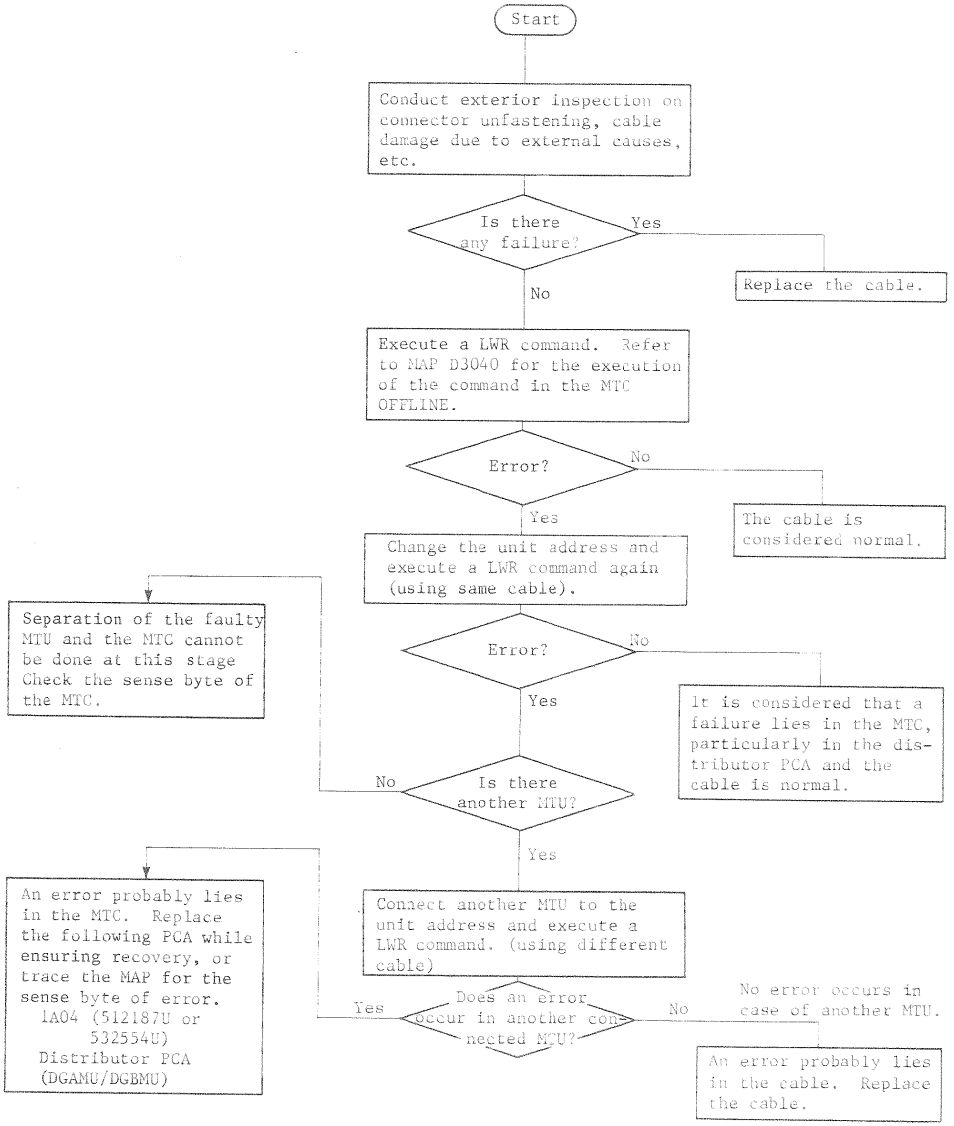
D3020	MTC-MTU interface circuit



D3021	Investigation of the Cable between the MTC and the MTU

In case a failure occurs in a particular MTU or the MTU having a specific unit number, an attempt is made to check whether the cable between the MTC and the relevant MTU is normal. (Connection failure, disconnection, shortcircuit, etc.)





D3040	Loop Write to Read Command (LWR) Execution - 1

How to execute the LWR command offline from MTC, using Field Tester

(1) If the MTC is not connected with a field tester, first a field tester must be connected. If a field tester is already connected, execution may be jumped to (7).

(2) Turn the ONL/OFL switch of field tester to the OFL position, and insert the connector in the connector for field tester 1A07 (512185U).
→ See MAP51

(3) To execute system reset and lamp TEST from the CE panel, the steps (4) to (5) should be executed.

(4) S0 to S7 are set at X'F0'. (Lamp test)
At this time, L0 to L11 must all light.

(5) Then, CNT switch is set on. .... System Reset

(6) If the system reset is completed, L8 (ERRF), L10 (PHLT), and L11 (PERR) are supposed to be off.

(7) To carry out command code setting, the field tester is operated in the following sequence. However, when register address '3D' is displayed in the register and '8B' is already set, this procedure may be omitted.

S0 ∿ S7 X'B2'
↓
CNT-SW ON
↓
S0 ∿ S7 X'8B'
↓
SSS-SW ON
↓
S0 ∿ S7 X'3D'
↓
SSS-SW ON

(8) To carry out device address setting, the field tester is operated in the following sequence. However, when register address '3E' is displayed in the register and the relevant device address is set, this procedure may be omitted.

S0 ∿ S7 X'B2'
↓
CNT-SW ON
↓
S0 ∿ S7 X'ΔΔ'
↓
SSS-SW ON
↓
S0 ∿ S7 X'3E'
↓
SSS-SW ON

ΔΔ: Device address

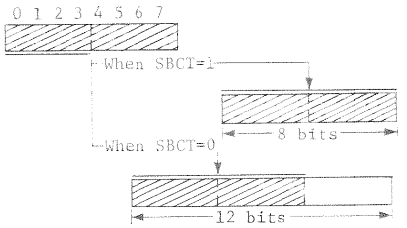
0	1	2	3	4	5	6	7
SBCT	"0"	"0"	"0"	"0"	DVA0	DVA1	DVA2

→ Short Byte Count
"1" → 8-bit counter
"0" → 12-bit counter

(9) To carry out byte count setting, the field tester is operated in the following procedure. However, when register address '3F' is displayed in the register and already set at a predetermined byte count value, this procedure may be omitted.

S0 ∿ S7 X'B2'
↓
CNT-SW ON
↓
S0 ∿ S7 X'oo'
↓
SSS-SW ON
↓
S0 ∿ S7 X'3F'
↓
SSS-SW ON

oo: Byte count



(Continue to D3041)

D3041	LWR Command Execution - 2

(Continue from D3040)

(10) Preparation for executing an LWR command is completed by performing steps (7) and (8). Thus, various parameters can be available for the execution of an LWR command. To modify the execution of the LWR using these parameters, they are loaded in registers SDIA1 (address X'38') ∿ SDIA3 (address X'3B') and OFLCNT (address X'3C').

→ See MAP M0000

By performing the above operations, in case it is considered that any unexpected parameters might have been set in registers, operate the register display to ensure the contents of registers.

These registers never be reset except the case when the MTC is power on.

(11) Execution of an LWR command

An LWR command is executed immediately when the SSS switch of field tester is turned on.

When 'REPEAT' parameter is designated, the execution of an LWR command is repeated ever without turning on the SSS switch until 'REPEAT' parameter is reset, a stop condition is made by such parameter as 'UNIT-CHECK-STOP', or 'SINH' is indicated.

If there is no 'REPEAT' parameter in the register, an LWR command is executed every time the SSS switch is turned on.

(12) Confirmation of the execution result

When the execution of an LWR command results in an error, ERRF bit (L8 lamp to be used wher S0 to S7 are set at X'80') lights. When this bit lights, it indicates that UNIT CHECK is contained in the END status of the executed command. This lamp is kept lighting throughout the time starting from generation of the END status and ending with issuance of the next command.

The END status is stored in DSB register at address '0A'.

(13) Sense byte

Since the sense data that indicates the cause of error is stored in SB0 (addressX '20') to SB23 (address X'2B') when the ERRF lights (when the UNIT CHECK of DSB register address '0A' is set on), check the contents of these registers through register display function of field tester instead of issuance of a sense command.

D3042	LWR2 operation

LWR2 operation allows the MTU to bypass write data at different point from one in normal LWR operation as showed in Fig. 1.
LWR2 operation may be useful to MTU Read/Write fault isolation.

When Read/Write problem occures on specific MTU, examine LWR2 operation. If LWR2 operation has resulted in success, it is considered that the problem lies in a part of Write/Read Amps, Read/Write head, or adjustment related to those. (Refer A7000, A7100)

If LWR2 operation has resulted in failure, normal LWR operation should be executed next, then a appropriate PCB may be replaced.

To execute normal LWR operation with an MTU, procedure (1)∿(6) in MAP D03040 should be done. Then issue SDIA command with SLWR bit of SDIA FLAG BYTE 1. Detailed procedures are described in MAP D3043∿.

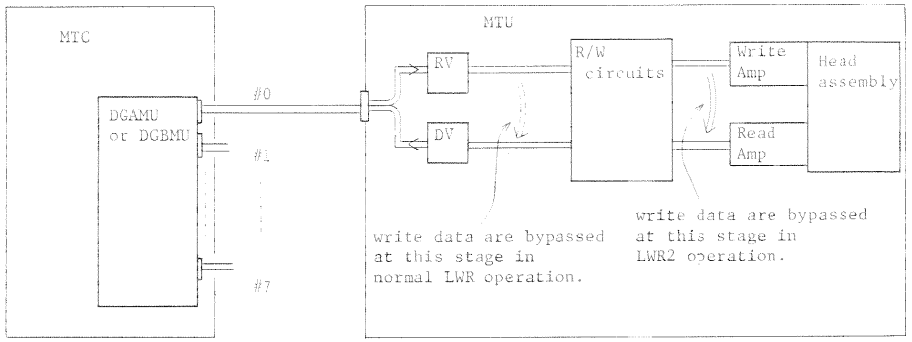
— Restriction —

1) 'Not capable' is posted when the MTU is in status detecting BOT.

2) 'Not capable' is posted when the MTU is in 800 rpi mode.

3) Executing LWR2 operation clears SAGC-Count of the MTU.

Fig. 1 LWR & LWR2



D3043	LWR2 Execution - 1

Refer M0100 about expression of field tester manupilation.

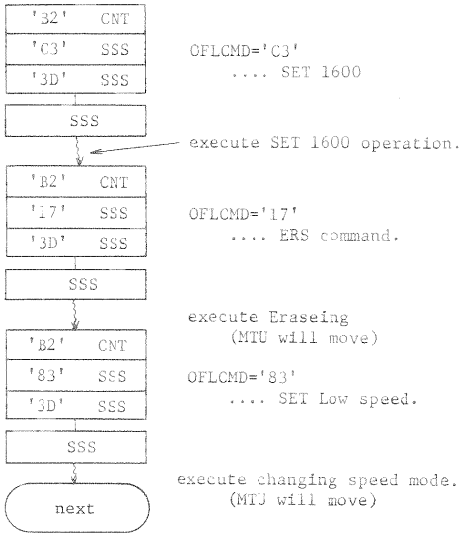
① Store MTU address and Byte count to OFLDVA, BCT register.
See procedure (8) (9) on MAP D3040.

OFLDVA = dd.
BCT = bb.

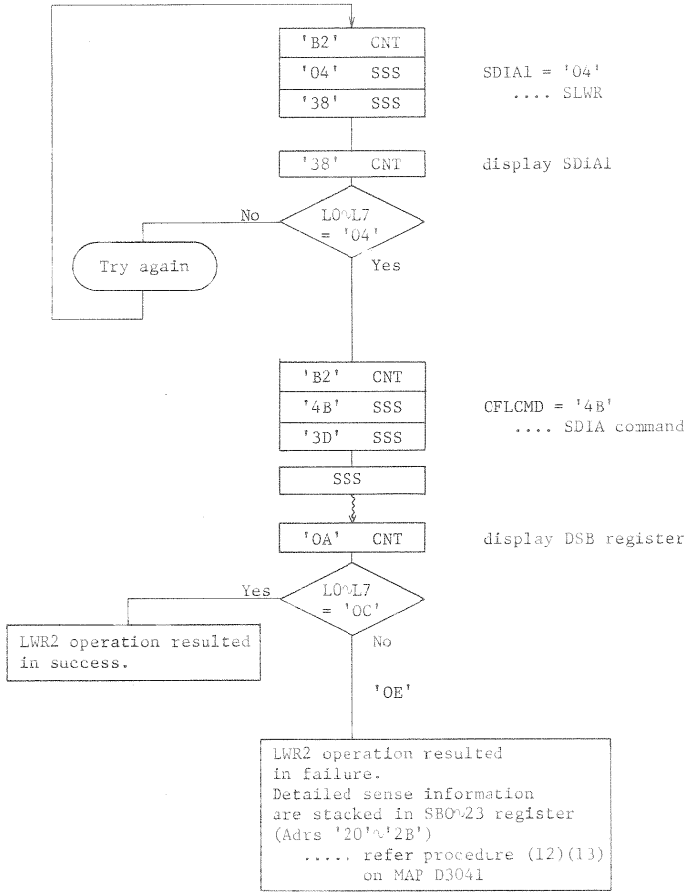
② Store offline execution parameter to DFLCNT register.
Here, parameter is .. all '0' (Single command execution).

OFLCNT = 00

③ To allow MTU to move foreard if the MTU is in BOT detected status, issue WRT, WTM, or ERS command to the MTU. If density or speed made have to be designated, SET 6250/SET 1600 command, or SET-HIGH SPEED/SET LOW SPEED command had better be issued. SET 6250/SET 1600 command should be issued to the MTU in BOT detected status.

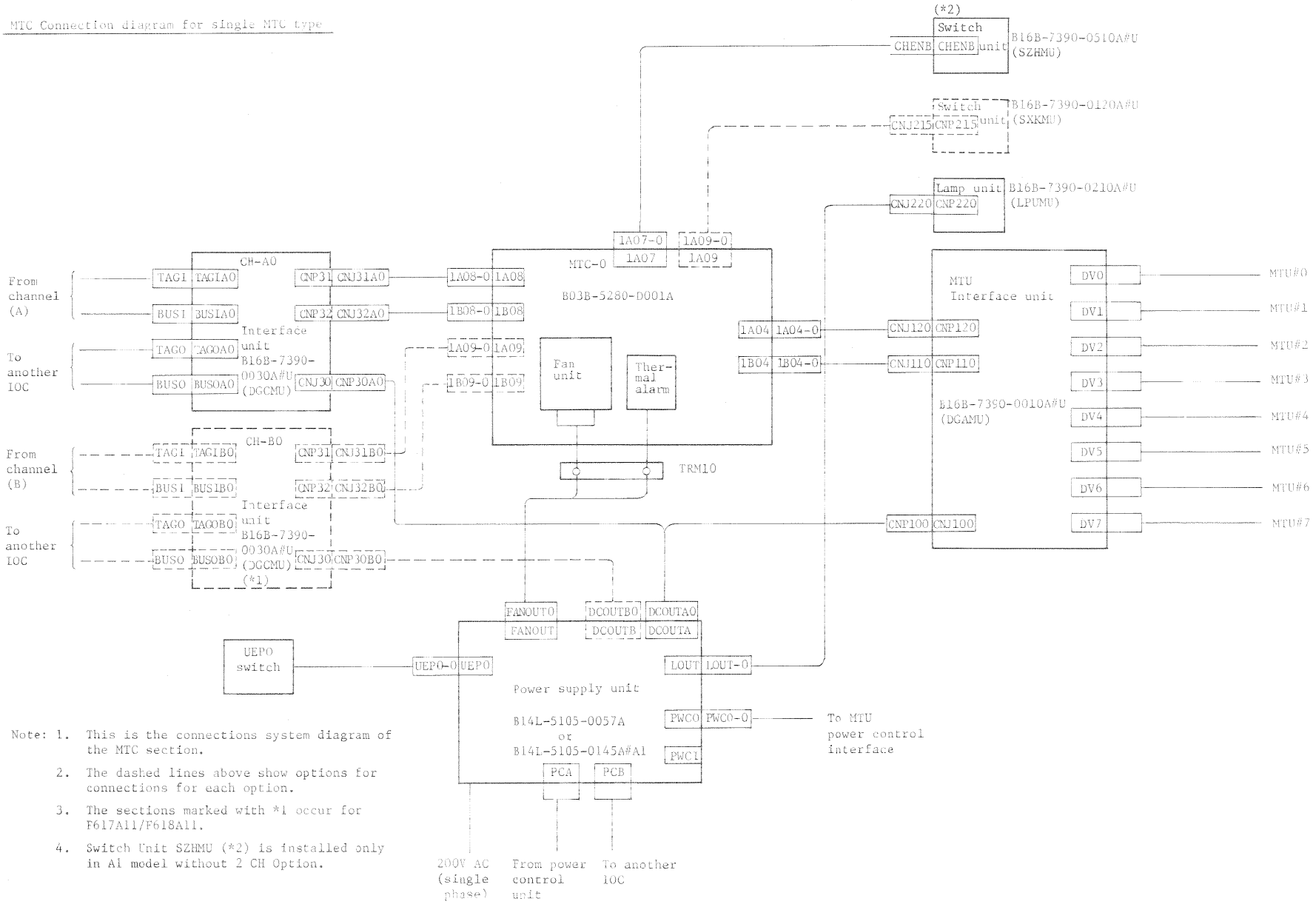


④ Store SLWR bit ('04') to SDiAl register. Then, issue SDIA command.



D3050	Cabling Network - 1

MTC Connection diagram for single MTC type



Note: 1. This is the connections system diagram of the MTC section.

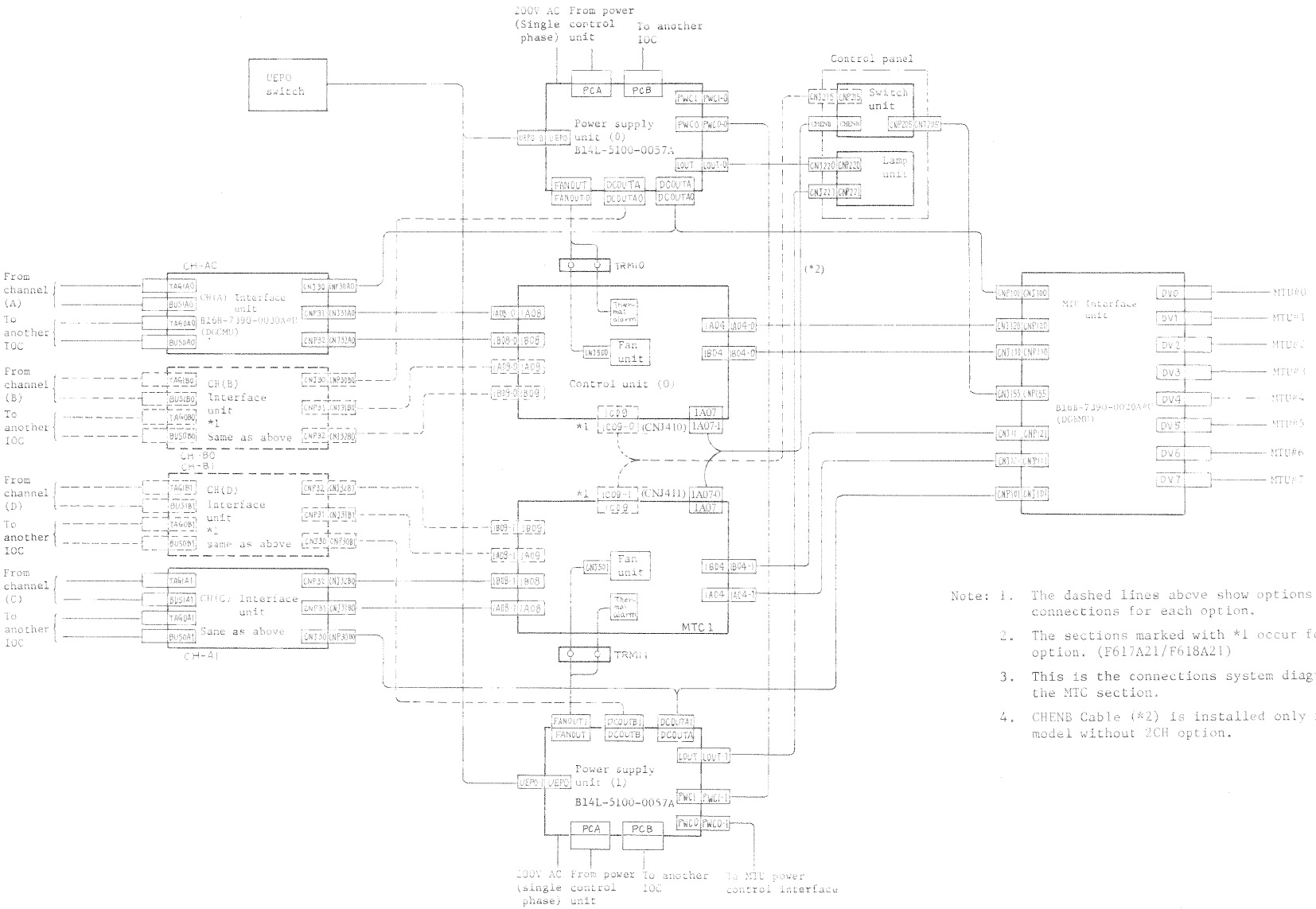
2. The dashed lines above show options for connections for each option.

3. The sections marked with *1 occur for F617A11/F618A11.

4. Switch Unit SZHMU (*2) is installed only in A1 model without 2 CH Option.

D3051	Cabling Network - 2

MTC Connection diagram for dual MTC type



Note: 1. The dashed lines above show options or connections for each option.

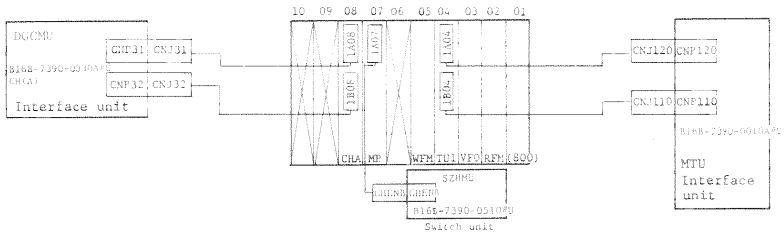
2. The sections marked with *1 occur for the 2CH option. (F617A21/F618A21)

3. This is the connections system diagram of the MTC section.

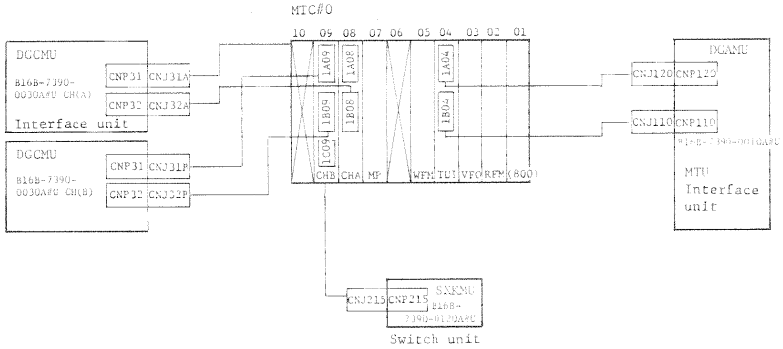
4. CHENB Cable (*2) is installed only in A2 model without 2CH option.

D3052	Cabling Network - 3

A1 2CH switch option absent; monitor interface option absent



A1 2CH switch option present; monitor interface option absent (with dashed lines)



The above diagrams show the cable connections of the A1/A2 type special PCAs with the MTC shelf.

*1 . When the 2CH option is present and the monitor interface option is absent:

A1 SXKMU.CNJ215 —— 1C09

A2 SXGMU.CNJ215 —— MTC#0.1C09, MTC#1.1C09

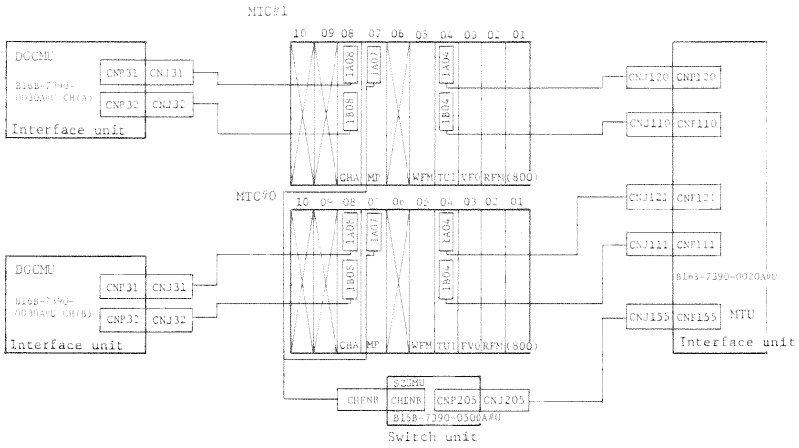
. When the monitor interface option is present:

A1 SXKMU.CNJ215 —— DGDMU.CNJ410 DGDMU.CNJ420 —— 1C09

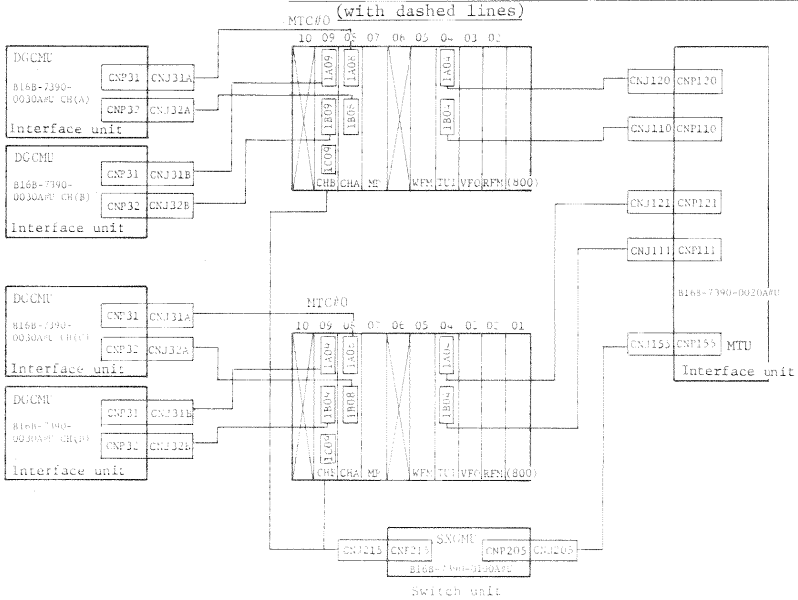
A2 SXGMU.CNJ215 —— DGDMU.CNJ410 DGDMU.CNJ420 —— MTC#0.1C09

DGDMU.CNJ411 DGDMU.CNJ421 —— MTC#1.1C09

A2 2CH switch option absent; monitor interface absent

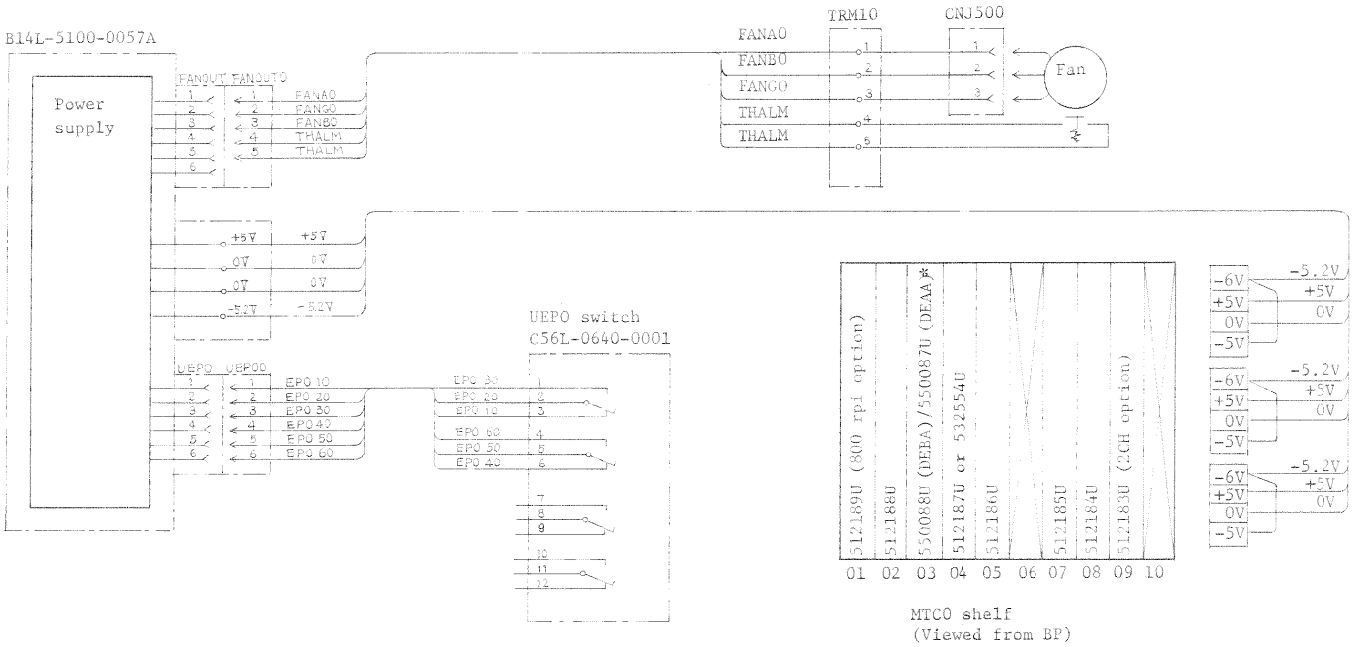


A2 2CH switch option present; monitor interface option absent (with dashed lines)



D3053	Cabling Network - 4

MTC power cabling for single MTC type

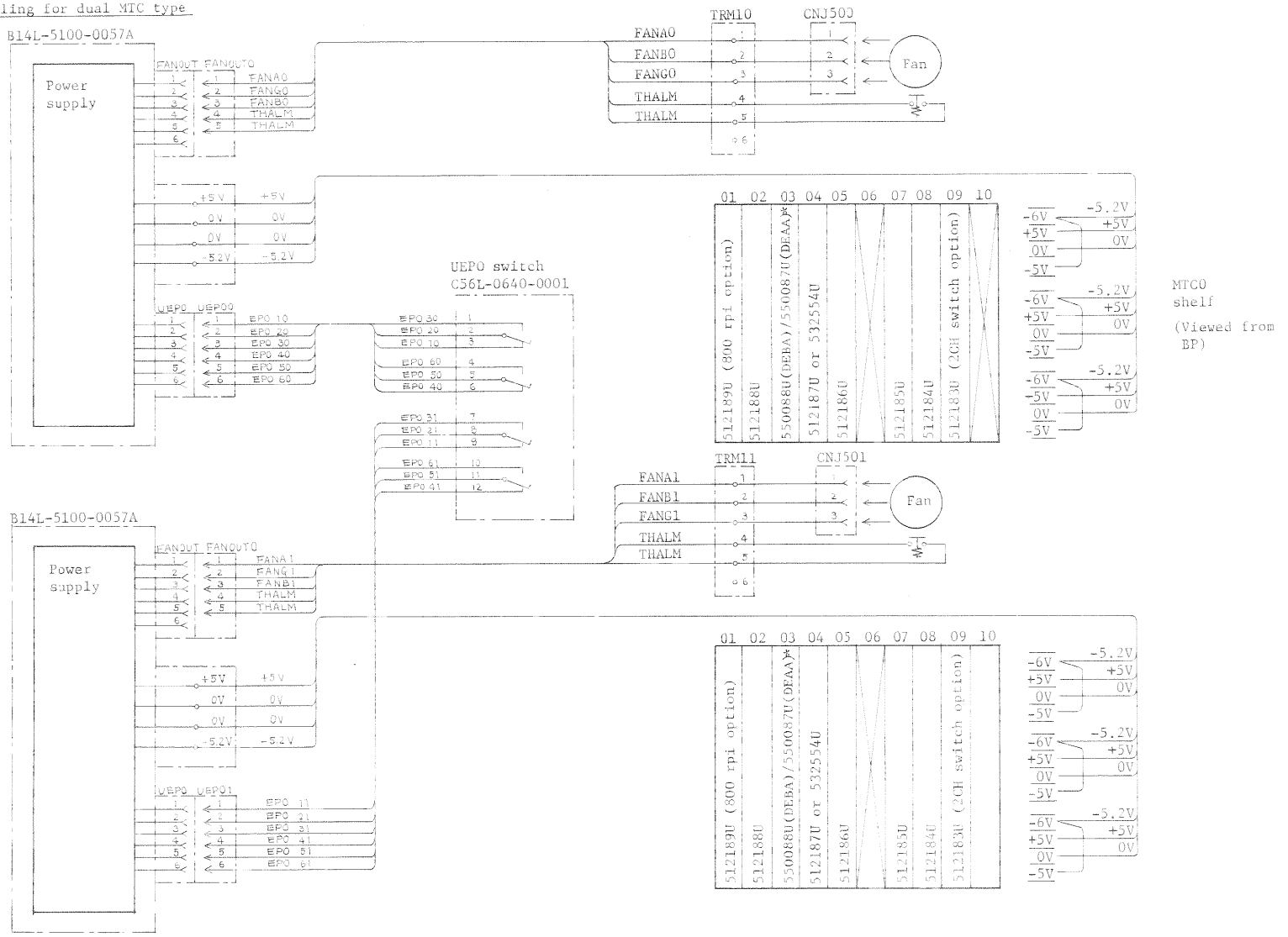


MTC0 shelf
(Viewed from BP)

*: 5500880 (DEBA) for 75/125 ips.
5500870 (DEAA) for 125/200 ips.

D3054	Cabling Network - 5

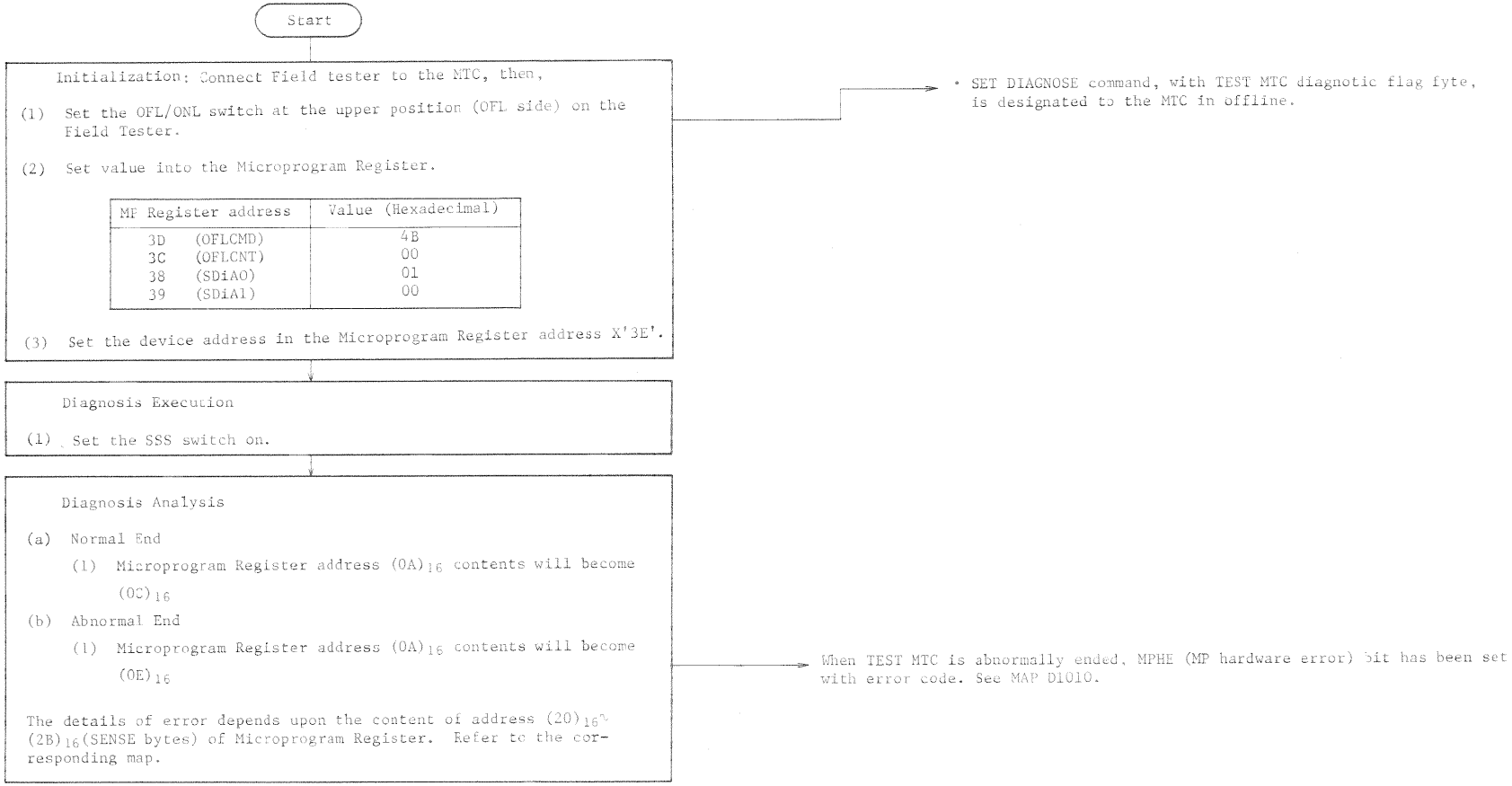
MTC power cabling for dual MTC type



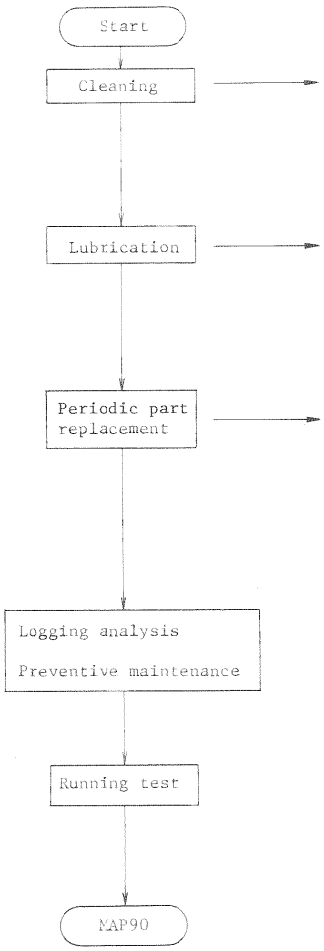
*: 550088U (DEBA) if F617A2
550087U (DEAA) if F618A2

F0001	Off Line Diagnosis Procedure for MTC

Execute "TEST MTC" which is part of the Offline Diagnosis. See M0175.



H0001	Preventive Maintenance



WARNING

1. Unload the tape before cleaning.
2. Use a solvent as cleaning agent.
3. Do not use heard tools, such as metal bars, which may damage the head.

J0000

	Maintenance	Period
1.	Tape guide: disassembly and cleaning	Every 3 months
2.	Tape cleaner: "	"
3.	Air bearing: "	Annually
4.	Tape panel front side: cleaning	Every 6 months
5.	Air filter (cooling): "	Every 3 months
6.	MTC air filter: "	"

WARNING

1. Apply the specified oil to the proper location in the correct quantity.
2. Do not lubricate excessively so as to prevent the oil from dripping or adhering to other parts.

J0000

1.	Front door rail: Lubrication	Every 6 months
2.	Slide rail: "	"

WARNING

1. Keep the power off during the parts replacement.
2. Do not lose the removed machine screws, washers, nuts, etc.
3. If any part is dropped into the unit, the part must always be removed.

J0000

1.	Absolute filter: replacement	Every 2 years
2.	Air filter (cooling): "	Every 2 years*
3.	Belt (air supply): "	Annually
4.	MTC air filter: "	Every 2 years

Note*: Air filter (cooling) is cleaned or replaced every 3 months, and moreover it shall be periodically replaced every 2 years.

REFERENCE Maintenance by operator: cleaning

	Maintenance	Period
1.	R/W and erase heads: cleaning	Every 8 hours
2.	Capstan roller: "	"
3.	Guide: "	"
4.	Air bearing: "	"
5.	Tape cleaner: "	"
6.	BOT/EOT photo sensor: "	"
7.	Column interior, glass cover "	"

J0000	Cleaning, Lubrication Procedure

Cleaning

The parts which are in contact with the tape must be carefully cleaned. Cleaning is required before any continuous long job operation. If the cleaning is neglected, errors may occur and dust attached to the tape may cause trouble.

Cautions in cleaning

1. Unlcad the tape before cleaning.
2. Use a solvent as a cleaning agent.
3. Do not use a hard tools, such as metal bars, which may damage the device.

Periodic cleaning by CE

	Maintenance	Period	Method
1	Tape guide: disassembly and cleaning	Every 3 months	J0005
2	Tape cleaner: "	"	J0007
3	Air bearing: "	Annually	J0006
4	Tape panel front side: cleaning	Every 6 months	J0009
5	Air filter (cooling): "	Every 3 months*	J0011
6	MTC air filter: "	Every 3 months*	J0012

Note*: Air filter (cooling) is cleaned or replaced every 3 months, and moreover it shall be periodically replaced every 2 years.

Periodic cleaning by operator

	Maintenance	Period	Method
1	R/W head and erase head: cleaning	Every 3 hours	J0001
2	Capstan roller: "	"	J0002
3	Guide: "	"	J0003
4	Air bearing: "	"	J0003
5	Tape cleaner: "	"	J0004
6	BOT/EOT photo sensor: "	"	J0008
7	Column interior, glass over: "	"	J0003

J0001	R/W Head and Erase Head Cleaning

Hold autocleaner tape path to the right and clean the Read/Write head and Erase head with a gauze cloth soaked in solvent, using a circular motion.
Never wipe the head with any hard materials.
After cleaning, check that no gauze thread is left on the heads.

J0002	Capstan Roller Cleaning

While turning the capstan by hand (covered with gauze cloth or clean glove), clean the capstan carefully with a gauze cloth soaked in solvent.
Do not touch the surface of the capstan directly.
Check for any peels of the surface coating and wears. Replace the capstan motor (L0130), if a discrepancy is detected.

J0003	Tape Guide, Air Bearing, Threading Chute, Roller Guide, Upper and Lower Threading Channels, Column Interior, and Glass Cover Cleaning

Clean each part carefully with a gauze cloth soaked in solvent.
To clean the narrower parts, use a cotton swab which contains solvent.
To remove dirt which cannot be removed easily with a gauze cloth or cotton swab, use a brush (containing solvent) and then use the gauze cloth or cotton swab (containing solvent).

J0004	Tape Cleaner Cleaning

Clean the edges of the tape cleaner with a gauze cloth or cotton swab soaked in solvant.

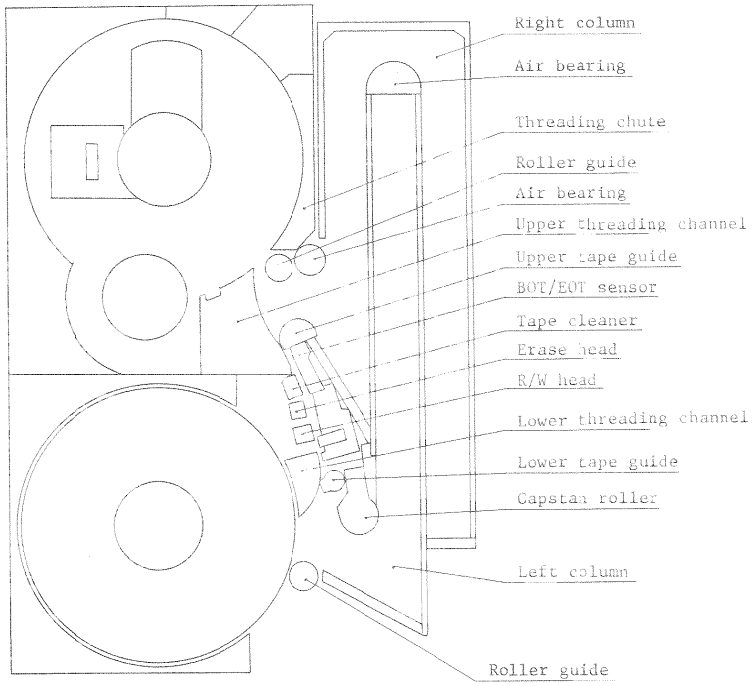


Fig. 1

J0005	Tape Guide Disassembly and Cleaning

Remove the tape guides at upper and lower from the body, disassemble the guides, and clean the elements carefully with a gauze cloth, cotton swab, and brush soaked in solvent.
The air outlet hole in the upper guide must be completely free of dust.
With a gauze cloth soaked in solvent, clean the panel surface on which the guides are to be mounted.
Check the guide and flanges for any damage or groove caused by wear. Replace the guide if a discrepancy is detected. Then, assemble and attach the guides.
Refer to upper guide replacement (L0070) and lower guide replacement for the assembly and disassembly of the guides.

J0006	Air Bearing Disassembly and Cleaning

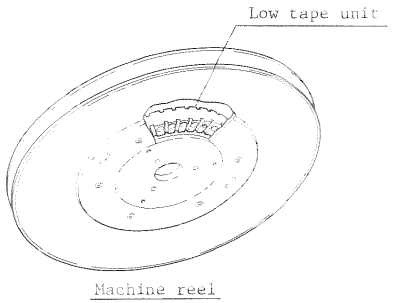
Disassemble the air bearing and clean it carefully with a gauze cloth, cotton swab, and brush soaked in solvent.
The air outlet holes in each air bearing must be completely free of dust.
With a gauze cloth soaked in solvent, clean the panel surface on which the air bearing is to be mounted. Then, attach the air bearing.

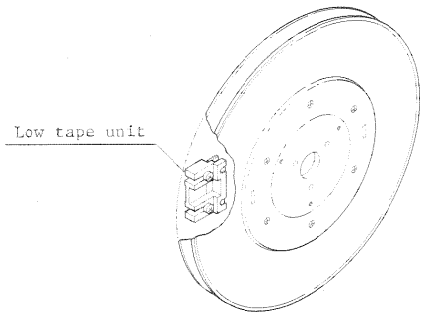
J0007	Tape Cleaner Disassembly and Cleaning

Disassemble the tape cleaner and clean it and the head mounting base carefully with a gauze, cotton swab, and brush soaked in solvent.
Refer to "Tape Cleaner Replacement" (L0050) for the assembly and disassembly of the tape cleaner.

J0008	BOT/EOT Sensor and Low Tape Unit Cleaning

Clean the surfaces of the light emission and reception elements of the BOT/EOT sensor and the low tape unit with a brush.
Before cleaning the low tape unit, machine reel must be removed. (Refer to L0230.)





J0009	Machine Reel, Panel Surface, and Door Glass Cleaning

Clean the external surface and interior of the machine reel, panel surface, and the both sides of the door glass with a gauze cloth soaked in solvent.

J0010	Mechanism Section Rear Side Cleaning

With a vacuum cleaner, clean the mechanism section from the rear.

J0011	Air Filter for Cooling Cleaning

Remove the air filter from the body and clean it with a vacuum cleaner.
Refer to "Air Filter (cooling) Replacement" (L0370) for the assembly and disassembly of the air filter (cooling).

J0012	MTC Air Filter Cleaning

Remove the air filter and clean it with a vacuum cleaner.

K0000	Check and Adjustment Procedure

General Cautions

1. Adjust oscilloscope and tester before measurement.
2. Unless otherwise noted, adjust the meter value to the center of the specified standard value.
3. Record the data at check and adjustment.
4. Handle the master skew tape carefully.
   Always remove the write enable ring during check and adjustment.
   (Operation requires the file protection.)

MTC Check and Adjustment Items

No.	Check & adjustment item	MAP No.	Period
1	Power supply voltage	K0001	Annually
2	VFO free-running frequency (6250 rpi, 1600 rpi)	K0002	Every 6 months
3	Clock width check and adjustment	K0003	Annually
4	System setting ... MTC address	K0004	-
	" ... MTC EC level	K0005	-
	" ... MTC feature	K0006	-
	" ... Interface unit setting	K0007	-

MTU Check and Adjustment Items

No.	Check & Adjustment Items	MAP No.	Period
1	Power supply voltage	KC100	Annually
2	Clock pulse check	KC101	Annually
3	Capstan tachometer output	KC110	Every 3 months
4	Azimuth	KC120	Every 6 months
5	Read signal level (6250/1600 rpi MTU)	KC130	Every 6 months
6	Read signal level (1600/800 rpi MTU)	KC140	Every 6 months
7	Read and Write Skew (1600/800 rpi MTU)	KC150	When necessary
8	Write voltage	KC160	Annually
9	Erase effect	KC170	When necessary
10	Hose tube	KC180	When necessary
11	Pressure level (pressure, vacuum)	KC190	When necessary
12	Belt tension (air supply unit)	KC200	When necessary
13	BOT/EOT detection circuit	K0210	Annually
14	Low tape detection circuit	K0220	Annually
15	Tape loop position detection circuit	K0240	Annually
16	File protect mechanism	K0260	Every 6 months
17	Front door synchronous belt tension	K0280	When necessary
18	Auto cleaner	K0290	When necessary

K0001	Power Supply Voltage Check and Adjustment (MTC)

Measure and adjust the following voltages with a 0.5 class or more voltmeter.

Voltage	Measurement point	Allowable range	Adjustment point
+5 V	+5 V Terminal (Shelf)	+4.75 ~ +5.25V	+5 V VOLT ADJ (Power supply unit)
-5.2 V	-5.2 V Terminal (Shelf)	-5.46 ~ -4.94 V	-5.2 V VOLT ADJ (Power supply unit)

Refer Fig. 1 on MAP B0102

K0002	VFO Free-Running Frequency Check (6250 rpi, 1600 rpi)

VFO Free-Running Frequency Check (6250 rpi, 1600 rpi)

1. Attach the Field-Tester to MTC and turn the ONLINE-OFFLINE switch to OFFLINE.

2. Set the tape speed and the density of MTC as following.

Field tester manupilation to set Tape speed

X'B2'	CNT
X'αα'	SSS
X`44`	SSS

αα:

0	1	2	3	4	5	6	7
0	0	0	0	0	A1	A2	A3

MTC model	Tape speed	A_1	A_2	A_3
324X	75 ips	0	1	0
	125 ips	1	0	1
326X/8T	125 ips	1	0	0
	200 ips	1	1	1

Field tester manupilation to set Density

X'B2'	CNT
X'ββ'	SSS
X'4C'	SSS

ββ:

0	1	2	3	4	5	6	7
0	0	C	0	B1	B2	0	0

Density	B_1	B_2
6250 rpi	1	0
1600 rpi	0	1

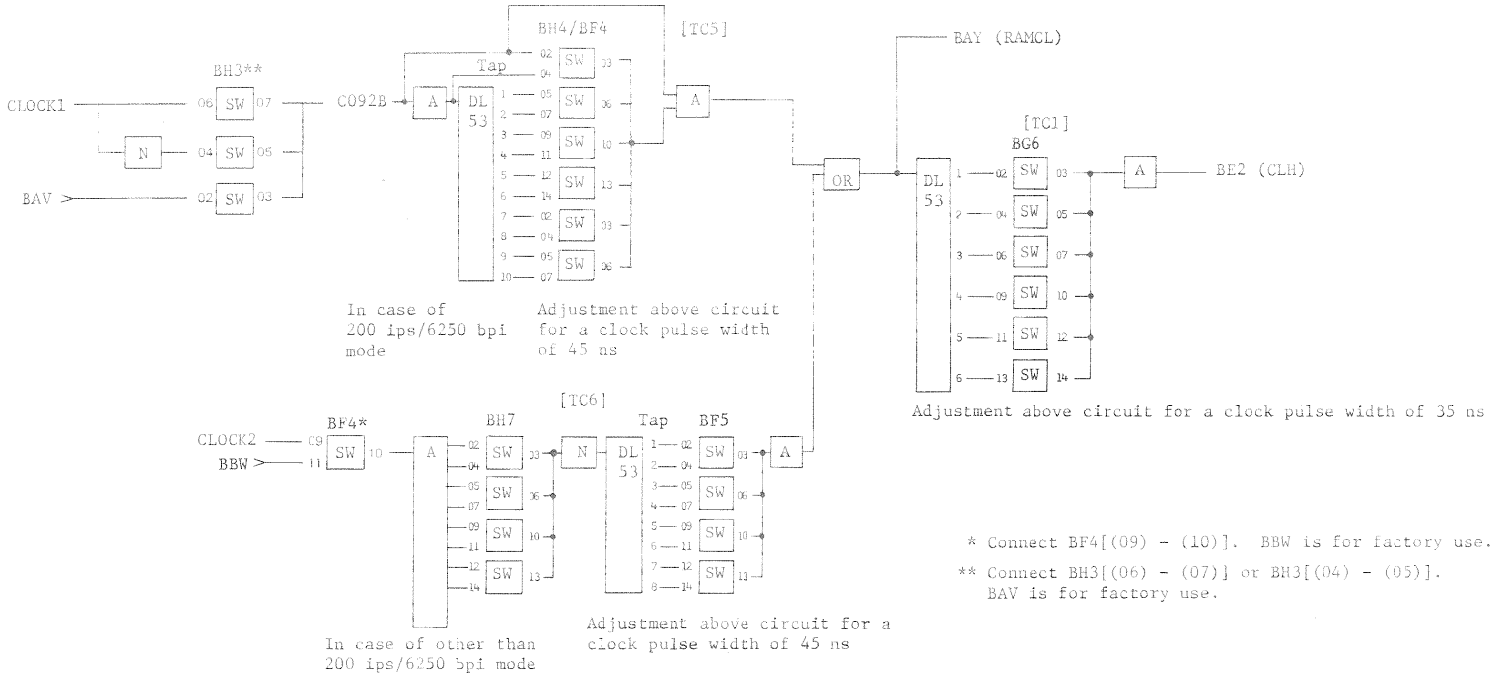
3. Clamp following back panel pins to 0 V, and measure the oscillation frequency of VFO. (Using appropriate columns on a per track basis.)

Bit	0 V clamp point			Measurement point
		324X	326X/8T	
0	1A03 Signal GND AL4	1A03 AB8	1A03 AA9	1A03 AA6
1		AE2	AAY	ABX
2		AE5	ADX	AD8
3		AG1	AH3	AEX
4		AHX	AL1	AGX
5		AKX	BB2	AL8
6		BA5	BA3	BB7
7		BE3	BD4	BAV
8		BEV	BDU	BEU

Recording density	Tape speed	Allowable range	Duration	Tolerance
6250 rpi	200 ips	1.80 MHz ± 15 %	555 ns	±83 ns
	125 ips	1.13 MHz ± 15 %	885 ns	±130 ns
	75 ips	678 MHz ± 15 %	1.48 µs	±0.22 µs
1600 rpi	200 ips	320 MHz ± 15 %	3.2 µs	±0.47 µs
	125 ips	200 MHz ± 15 %	5.0 µs	±0.75 µs
	75 ips	120 MHz ± 15 %	8.33 µs	±1.25 µs

4. Remove the 0 V clamp after the check.

K0003-1	Clock Width Check and Adjustment



* Connect BF4[(09) - (10)]. BBW is for factory use.

** Connect BH3[(06) - (07)] or BH3[(04) - (05)]. BAV is for factory use.

Circuit Diagram Number TC0/TC1/TC5/TC6

Setting PCA C16B-5121-0870#U or C16B-5325-0540#U

Check and adjust the clock width with an oscilloscope

1. Check and adjustment of a clock having a pulse width of 45 ns in the 200 ips/6250 bpi mode

Measuring point	Allowable range	Adjusting method			
		DL53 Tap	SH09 mounting position		
RAMCL 1A04 BAY	45^{+5}_{-2} ns	1	02 04 > 03	1A04 BH4	Use one of them for adjustment
		2	05 07 > 06		
		3	09 11 > 10		Pulse width narrows by 2 ns for the increment of one tap on the left column.
		4			
		5	12 14 > 13		
		6			
		7	02 04 > 03	1A04 BF4	
		8			
		9	05 07 > 06		
		10			

Note: Set the MTC in the 200 ips/6250 bpi mode before checking of this mode. To set the MTC in this mode, set X'08' to the register address X'4C' of the microprocessor and X'08' to X'4C'. (Refer K0002)

K0003-2	Clock Width Check and Adjustment (continued)

2. Check and adjustment of a clock having a pulse width of 45 ns in other than the 200 ips/6250 bpi mode

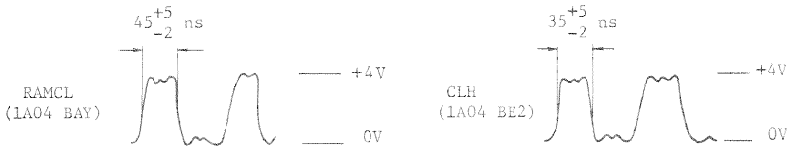
Measuring point	Allowable range	Adjusting method	
		AND circuit DL53 Tap	SH09 mounting position
RAMCL 1A04 BAY	45^{+5}_{-2} ns		02 > 03 04 > 05 > 06 07 > 09 > 10 11 > 12 > 13 14 > 1A04 BH7 Use one of them for adjustment Rough adjustment is done by this setting. When setting the bottom part on the left of the above figure, pulse width increases by 3 to 6 ns for the increment of one tap.
		1 – – + 02 > 03 2 – – + 04 > 3 – – + 05 > 06 4 – – + 07 > 5 – – + 09 > 10 6 – – + 11 > 7 – – + 12 > 13 8 – – + 14 > 1A04 BF5 Use one of them for adjustment Fine tuning is done by this setting. Pulse width increases by 2 ns for every increment of one tap in the above figure.	

Notes: 1) In this setting there are two setting portions.

2) Set the MTC in the appropriate mode before checking this mode. (either 800 or 1600 BPI)

3. Check and adjustment of a clock having a pulse width of 35 ns

Measuring point	Allowable range	Adjusting method	
		DL53 Tap	SH09 mounting position
CLH 1A04 BE2	35^{+5}_{-2} ns	1 – – + 02 —— 03 2 – – + 04 —— 05 3 – – + 06 —— 07 4 – – + 09 —— 10 5 – – + 11 —— 12 6 – – + 13 —— 14	1A04 BG6 Use one of them for adjustment A pulse width narrows for every increment of one tap on the left column.



K0004	System Setting .... MTC Address

The MTC address is set with 0 to 4 on the ADDRESS BUS.

	MTC				MTU		
bit	0	1	2	3	4	5	6	7

Connection for Route A side channel

MTC address bit No.	Connected terminal No.		Short-circuit mounting position
	"0"	"1"	
0	04-03	02-03	1A08 AG7
1	07-06	05-06	
2	11-10	09-10	
3	14-13	12-13	
4	04-03	02-03	1A08 AG6

Circuit Diagram Number [IA3]

Setting PCA C16B-5121-0840#U

This content can be ensured setting $(00)_{16}$ to the address '58' of microprogram register using a field tester to display the contents of Address '58' (bits 0 to 4) of microprogram register. Refer Map K0013.

Connection for Route B side channel

MTC address bit No.	Connected terminal No.		Short-circuit mounting position
	"0"	"1"	
0	04-03	02-03	1A09 AM5
1	07-06	05-06	
2	11-10	09-10	
3	14-13	12-13	
4	04-03	02-03	1A09 AM6

Circuit Diagram Number [JA3]

Setting PCA C16B-5121-0830#U

Using a field tester, this content can be ensured by displaying the content of bits 0 to 4 of address 64 of microprogram register. Refer Map K0013.

K0005	System Setting .... MTC EC Level

The EC level of MTC is determined by plugging pins on the terminal board (SH09) on a PCA.

MTC EC BIT No.	Connected terminal No.		Short-circuit mounting position
	"0"	"1"	
0	09-10	11-10	PCA 512585U BB1 (1A07)
1	12-13	14-13	"
2	02-03	04-03	"
3	05-06	07-06	"

Circuit Diagram Number MP1

Using a field tester, this content can be ensured by displaying the content of bits 4 to 7 of address '61' of microprogram register. Refer Map K0013.

K0006	System Setting .... MTC Feature

Mounting position	Pin No. portion A	Meaning	Pin No. protion B	Meaning
1A07 AA7	03-04	For the MTC other than that to MEMOREX Co.,	02-03	For the MTC to MEMOREX Co.,
	06-07	IB.ARA write retry is not carried out.	05-06	IB.ARA WRITE RETRY is carried out.
	10-11	Normal IBG (0.3")	09-10	Long IBG (0.4")
	13-14	800 read, IBM mode	12-13	800 read, FJ mode
1A07 AA6	03-04	15 m check (RWTOV) function is valid.	02-03	15 m check (RWTOV) is not checked.
	06-07	Normal Sense Byte. (IBM compatible)	05-06	Special Sense Byte assignment.
	10-11	Normal	09-1	SPERRY SYS 80 MODE ON
	10-11 13-14	Spare Portion A is " always set in this state.	09-10	Protion B must not be set on this side for future use.

Mounting position of the setting PCA is at C7 column, and specification No. is C16B-5121-0850#U. This setting is at '7F' for consignment, so setting pins must not be changed unless the above mode is changed.

This content can be ensured by displaying the content of address '63' of microprogram register using a field register. When pins are set at the above portion A, lamp lights, and when pins are set at the above portion B, lamp is turned off.

The following explains the above bits:

Bit 0 *MRX : Shows whether the MTC is for MEMOREX Co.

Bit 1 *IBRTRY: In case of portion B, IB and ARA write retry is carried out three times.

Bit 2 *LIBG : In case of portion B, IBG is set to 0.4 inch in the 6250 rpi mode.

Bit 3 I-800 : In case of portion A, noise (sense byte 1, bit 0) is not reported for a block less than 8-bit cell at 800 rpi in the IBM compatible mode.

Bit 4 15CK : In case of portion B, RW Time Over check function is suppressed, then long data block can be written (more than 15 m).

Bit 5 NSB : In case of portion B, sense byte 4 bit 0 is 20 m check and sense byte 4 bit 4 is MP Hardware error. Under IBM OS, setting must be portion A.

Bit 6 *SP MODE : For SPERRY System 80, setting must be portion B. Under IBM OS, setting must be portion A.

Bit 7 reserved for future use.

Mounting position	Pin No. portion A	Meaning	Pin No. protion B	Meaning
1A08 AG6	09-10	IBM compatible mode	10-11	Not IBM compatible mode
	05-06	IBM type BMC	06-07	Special setting for FJ BMC (SBMC)

Mounting position of the setting PCA is at 08 column, and specification No. is C16B-5121-0840#U.

This content can be ensured by setting $(00)_{16}$ at address '5F' of microprogram register using a field tester and by displaying the content of bit 5 and 6 of address '58'. Refer Map K0013.

Setting should be IBM compatible mode and IBM type BMC.

K0007	System Setting .... Interface Unit Setting

Short-circuit PCA and condition		Connected terminal No. SW1
DGCMU SW1	SELECT OUT receiving	03-04 06-07 13-14
	SELECT IN receiving	02-03 05-06 12-13

MTC miscel-laneous	Connected terminal No.	Short-circuit mounting position
must be connected as right.	05-06 12-13	1A08 AG6
	06-07 10-11 13-14	1A09 AM6
	03-04	1A07 BG7

K0008	Channel Extension Feature

Maximum length for channel cable can be increased by channel Extension Feature. In this case, data transfer between MTC and Channel are performed with Offset-Interlock mode rather than normal Interlock. There are some restrictions to select this feature. See Installation Manual, Section 3.

Feature selected	Connected terminal No.	Short circuit position
Normal mode	12-13	Column 1A08 PCA 512184U Location AG6
Channel Extension Feature	13-14	

K0009	Other Setting

If 2-channel switch is installed, setting must be 2-channel switch mode. Other two setting is not used.

Meaning	Connected terminal No.	Short circuit Position
Not used	05-06	Column 1A09 PCA 512183U Location AM6
	06-07	
Not used	09-10	
	10-11	
2-channel switch	12-13	
W/O 2CH SW	13-14	

Follow setting is for special mode other than IBM type, setting must be normal mode.

Meaning	Connected terminal No.	Short circuit Position
Special mode	02-03	Column 1A07 PCA 512185U Location BG7
Normal mode	03-04	

Note: There is no functional difference between two mode.

K0010	MTU settings ... PCA at 1A06 (1)

The PCA at 1A06 has five short-circuits (SH09) for setting of the serial manufactured number, the EC level and function. The serial manufactured number, EC level and function shall be set at the replacement.
In the 1A06 PCA replacement is for trouble recovery, the short-circuits setting contents are different, so, pay attention to the short-circuit setting for the PCA.

PCA designation	Setting contents	SH09 mounted position	Connected pin number	Remarks
512182U or 512649U	Tape Unit Unique ID	AG4, AG6, AG5, AG7 (See Fig. 1)	Procedure 1	Manufactured Serial No.
	EC Level	AF4 (See Fig. 1)	Procedure 2 (Next page)	Engineering Change Level
	Function	AG4 (See Fig. 1)	Procedure 3 (Next page)	Extended Interface, Skip File Feature, Enable Interrupt
Only 512649U	Function	AJ6 (See Fig. 1)	Procedure 4 (Next page)	SAGC step, streaming, Dual Density

Procedure 1 Setting of Manufactured Serial No.

Read the manufactured serial number of the right lower side at the back of MTU and convert the number to 13 bit binary code.

Correspondence of each bit and pin number of SH09 at the PCA

Short-circuits mounted position	Connected pin number '0'	Connected pin number '1'	Remarks
AG4	12 - 13	13 - 14	TID12 (2^{12})
AG6	02 - 03	03 - 04	TID11 (2^{11})
	05 - 06	06 - 07	TID10 (2^{10})
	09 - 10	10 - 11	TID9 (2^{9})
	12 - 13	13 - 14	TID8 (2^{8})
AG5	02 - 03	03 - 04	TID7 (2^{7})
	05 - 06	06 - 07	TID6 (2^{6})
	09 - 10	10 - 11	TID5 (2^{5})
	12 - 13	13 - 14	TID4 (2^{4})
AG7	02 - 03	03 - 04	TID3 (2^{3})
	05 - 06	06 - 07	TID2 (2^{2})
	09 - 10	10 - 11	TID1 (2^{1})
	12 - 13	13 - 14	TID0 (2^{0})

Set by inserting thirteen short-terminals to short-circuit SH09.
(See Fig. 2 of next page.)

Note: In case of replacement for trouble recovery, set the short-circuit (SH09) according to above Procedure 1.

Example: When manufactured No. 538

Binary code	AG4	AG6	AG5	AG7
	0	0 0 1 0	0 0 0 1	1 0 1 0
Connected Pin No.	12-13	2-3 5-6 10-11 12-13	2-3 5-6 9-10 13-14	3-4 5-6 10-11 12-13

PCA Parts Number: C16B-5121-0820#U or C16B-5126-0490#U

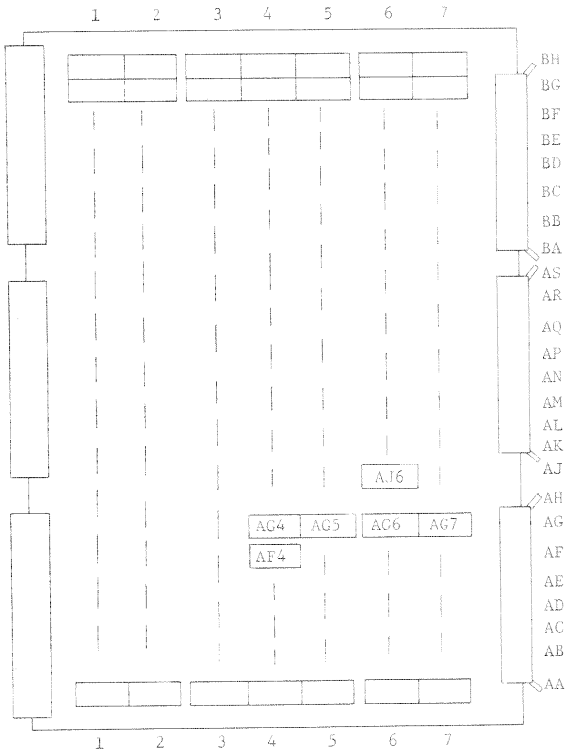


Fig. 1 SH09 location

K0011	MTU settings ... PCA at 1A06 (2)

Procedure 2 Setting of EC Level

Convert the EC level to 4 bit binary code and set the short-circuit SH09 (AF4) as follows.

Correspondence of each bit and connected Pin No.

Bynary code	2^3	2^2	2^1	2^0
Setting of '1'	3-4	6-7	10-11	13-14
Setting of '0'	2-3	5-6	9-10	12-13

} Connected pin No.

Set by inserting four short-terminals to the short-circuit SH09 (AF4). (See Fig. 2.)

Note: If EC level is not changed, PCA setting shall be the same as the previous PCA.
When MTU model has been converted (e.g. from 125 ips to 200 ips MTU), this 2^3 bit is set to '1'. This bit means MODEL CONVERSION.

Example: When EC level is 05

Setting					
	Binary code	0	1	0	1
	Connected Pin No.	2-3	6-7	9-10	13-14

Procedure 3 Setting of Function

Set the short-circuit SH09 (AG4) as follows.

	Extended interface	Skip file feature	Enable interrupt
Setting of '1'	3-4	6-7	(10-11)
Setting of '0'	(2-3)	(5-6)	9-10

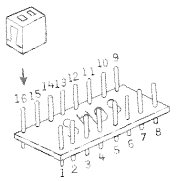
Set by inserting three short-terminals to the short-circuit SH09 (AG4). (See Fig. 2.)

Note: Extended interface ... When MTU has the Streaming function or Skip file function, set it to 1.

Skip file feature .... When MTU has the Space File and Backspace File functions, set it to 1.

Enable interrupt ..... To set Interrupt when the status is Not Ready to Read, set it to 1.

Short-terminal



SH09

Fig. 2 Setting for manufactured No., EC level and function

Procedure 4 Setting of Function

Set the short-circuit SH09(AJ6) in PCA 512649U as follows.

	Not Used	SAGC step	Streaming function	Dual Density
Setting of "1"	-	(6-7)	10-11	13-14
Setting of "0"	2-3	5-6	(9-10)	-

Set by inserting four short-terminals to the short-circuit SH09 (AJ6). (See Fig. 2.)

Note: SAGC step ..... If the read slice level change when the SAGC step is greater than C, set it to 0.
If the read slice level change when the SAGC step is greater than A, set it to 1.

Streaming function ... If User not use the streaming function, set it to 0. In case of 200 ips MTU, it must be set to '0'.

Dual Density ..... Always 1.

K0012	MTU settings ... PCA at 1A05

The PCA on 1A05 has a circuit for selecting options. All of them are set to 0 because no option function is implemented at present.

PCA Parts Number: C16B-5121-0810#U or C15B-5126-0480#U or C16B-5325-0210#U

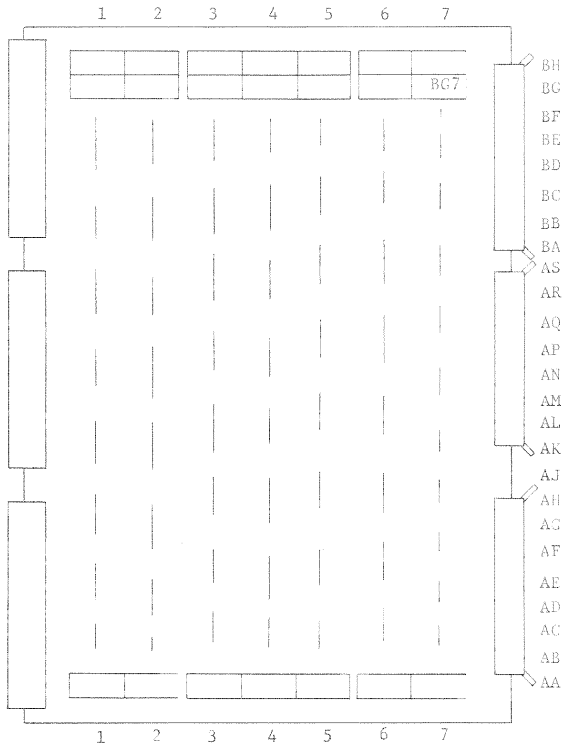


Fig. 1 SH09 location

Procedure 1 Setting of Option

Set the short-circuit SH09 (BG7) as follows.

	Option 0	Option 1	Option 2	Option 3
Setting of '1'	3-4	6-7	10-11	13-14
Setting of '0'	2-3	5-6	9-10	12-13

Install jumpers to select options SH09 (BG7). (See K0011, Fig. 2.)

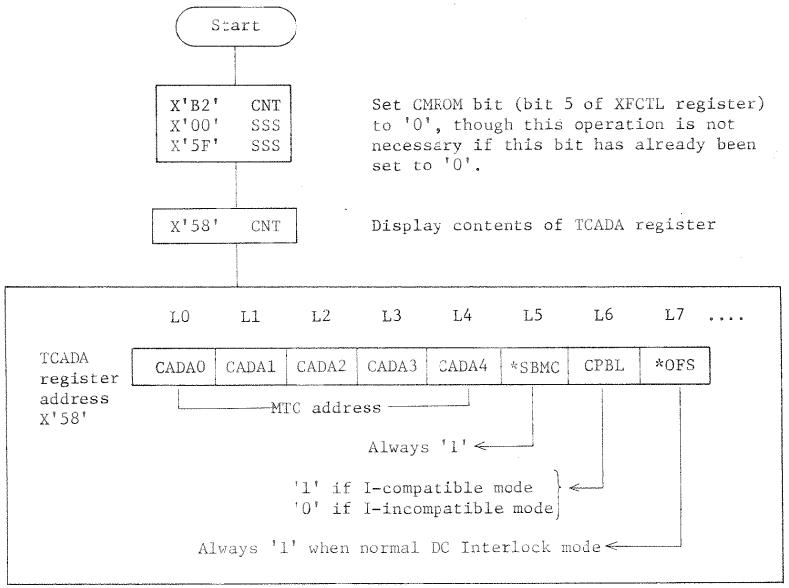
Note: Set all to be 0 because of no option function is implemented now.

K0013	Channel Interface Setting Inspection

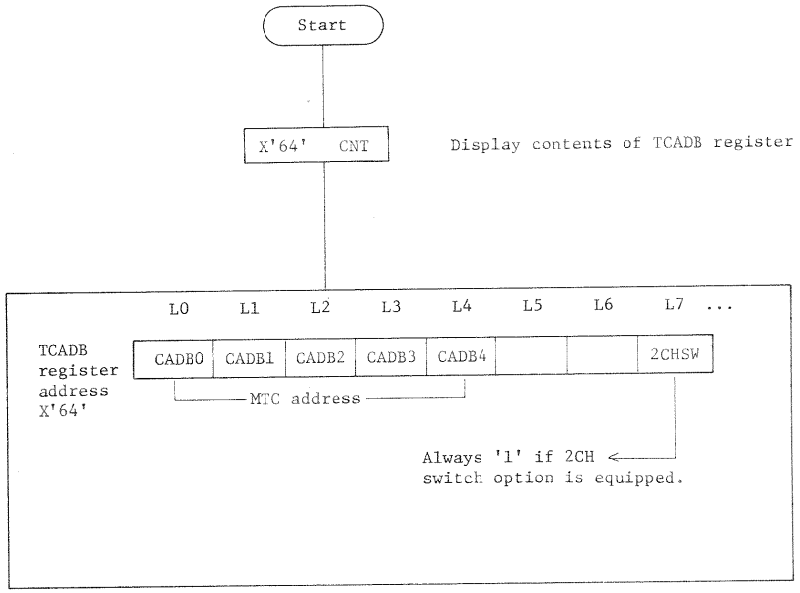
The setting of the MTC address, etc, can be displayed and checked by displaying the contents of the TCADA (address X'58') and TCADB (address X'64') registers with the field tester.

- Channel (A) interface -

The MTC must be in a stop or idle status.

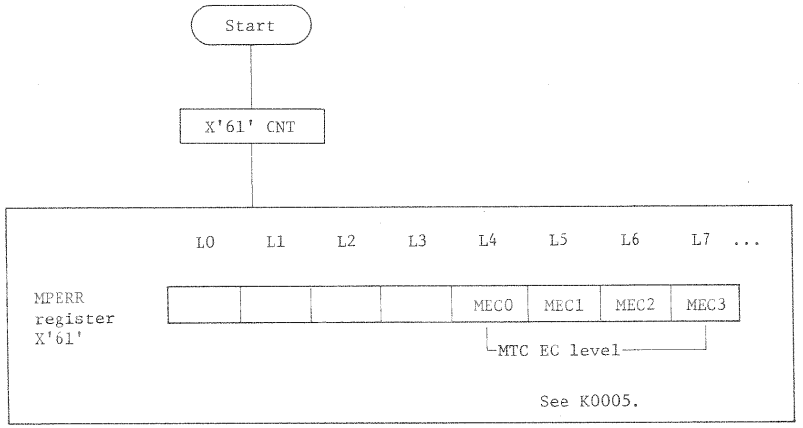


- Channel (B) interface -

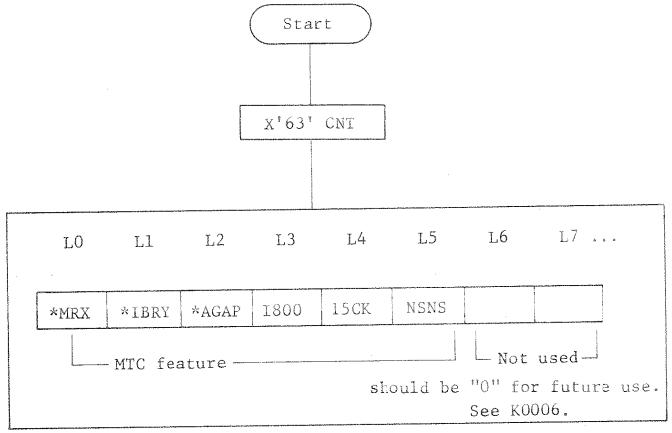


K0014	MTC EC Level/MTC Feature Inspection

- MTC level inspection -



- MTC feature inspection -



K0100	Power Supply Unit Check and Adjustment

Check and adjust the following items with potentiometer or digital voltmeter.

Confirmation items

Voltage	Check point	Allowable range	Adjustment position
+ 5V	Gate part 1A04 +5 V ... AK1 0 V ... AK2	+5 V±2%	1A02 VQJMU RV1
+12 V	WR⌴MU CHWR1 cn CHWR*	+12 V±8%	
-6 V	WR⌴MU CHWR5 cn CHWR	-6 V±8%	
±13 V	Gate part 1A01 +13 V ... ADV -13 V ... AEV	±13 V±8%	

*: File protect pin must be pushed in.

Procedure of exchanging PCA VQJMU

(1) Detach the connectors (CNP33, CNP35, CNP36) of VQJMU and confirm that the voltage (±24 V) across 6 and 7 and across 8 and 7 of terminal board TRM41, and the voltage (+11 V) between 4 and 5.

(2) Connect connector CNP33 only and temporarily adjust variable resistor RV1 on VQJMU to satisfy that the voltage across +5 V check point and 0 V check point is 5 V±2%.

(3) Connect connectors CNP35 and CNP36, and check the voltages listed in the above table (+5 V and confirm +12 V, -6 V, ±13 V).

Note: If the requirements of ±24 V and +11 V are not satisfied, replace the power supply unit.
If the requirements of +5 V, +12 V, -6 V and ±13 V are not satisfied, replace VQJMU.

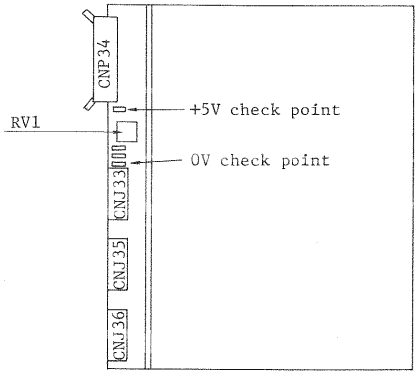


Fig. 1 Power circuit PCA (VQJMU)

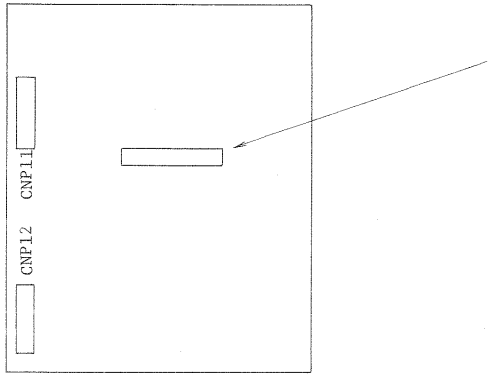
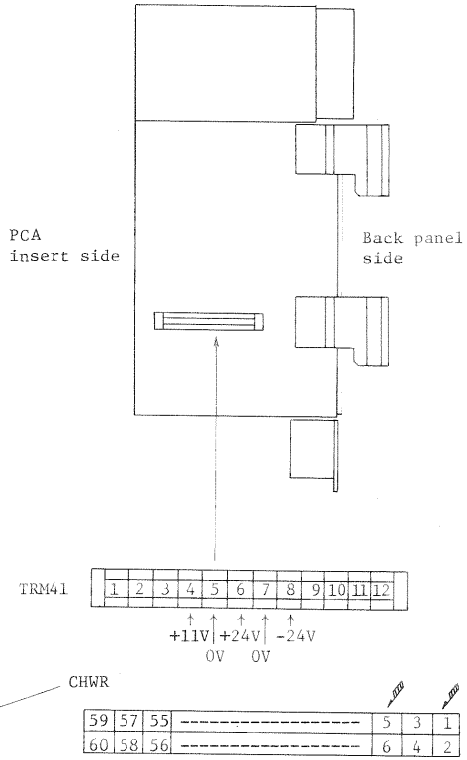


Fig. 2 Write/Read Amplifier PCA (WR⌴MU)

Fig. 3 Gate part



K0101	Clock Pulse Check

Check the following clock pulses with oscilloscope.

Item	Clock pulses	Check point	Allowable range	Remarks
1	CL8M	1A06 BB8 Gate section	T_0 = 125 ns ±1.5% Duty (Tw_0/T_0) = 50±15%	See Fig. 1.
2	CL1MA	1A06 BAX	T_1 = 1 µs±1.5%	
3	*DSPCL	1A06 ALV	T_2 = 500 ns±50 ns	
4	PTYCL	1A06 BBX	T_3 = 750 ns±50 ns Tw_1, Tw_2, Tw_3 = 62.5 ns±20 ns	

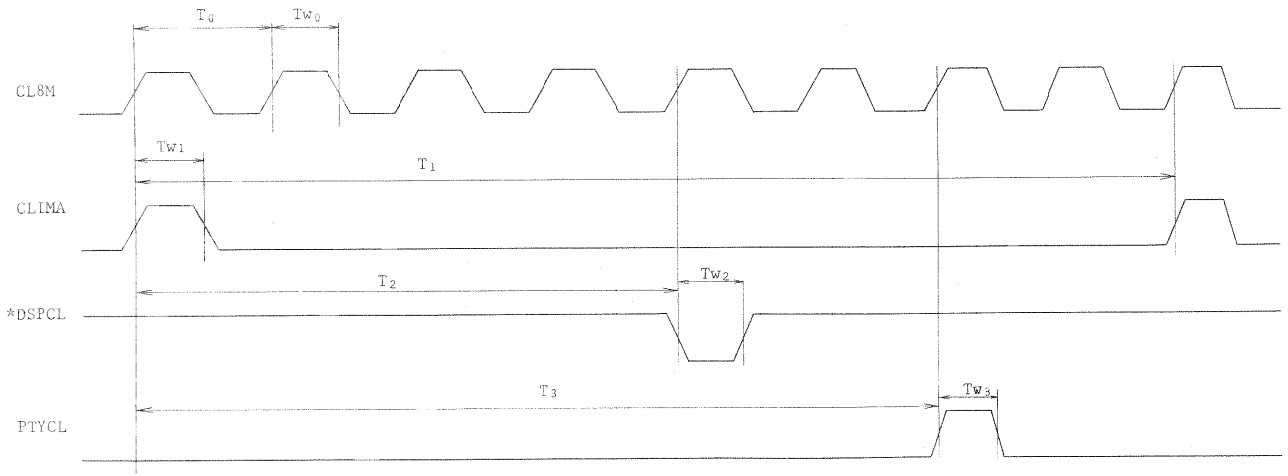


Fig. 1

K0110-1	Capstan Tachometer Output Check (1)

Check the following three items regarding tachometer output CPA and CPB of the capstan motor.

I. Duty Check

Connect a field tester and load a magnetic tape. Observe CPA and CPB with an oscilloscope during forward (Command code: $01) and backward (Command code: $41) motions in continuous mode using a field tester. Check that both directions of motion satisfy the requirements shown in Fig. 1.

Capstan tachometer	Measurement position (back panel)	Requirement
CPA CPB	1A01 AA6 1A01 AB6	Shown in Fig. 1

(If the requirements are not satisfied, see next page K0110-2, Note 1 for adjusting the duty.)

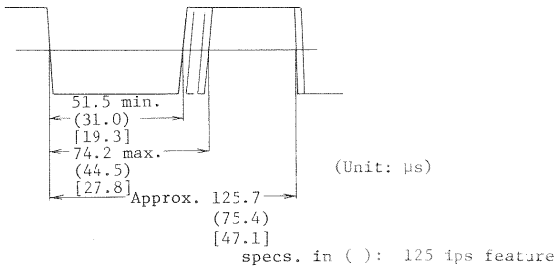


Fig. 1

II. Phase Check

Measurement at FWD running (Command code: $01):

1. Run a tape in the FWD direction in the same manner as item I above.
2. Observe CPA with channel (CH1) and CPB with channel (CH2) simultaneously.
3. Check that the requirements shown in Fig. 2 are satisfied when triggered by trailing edge of the pulse CPB (CH2).

Measurement at BWD running (Command code: $41):

1. Run a tape in the BWD direction.
2. Measure at the same terminals as in FWD running. In this case, exchange the oscilloscope input CH1 and CH2.
3. Check that the measured values satisfy the requirements shown in Fig. 2.

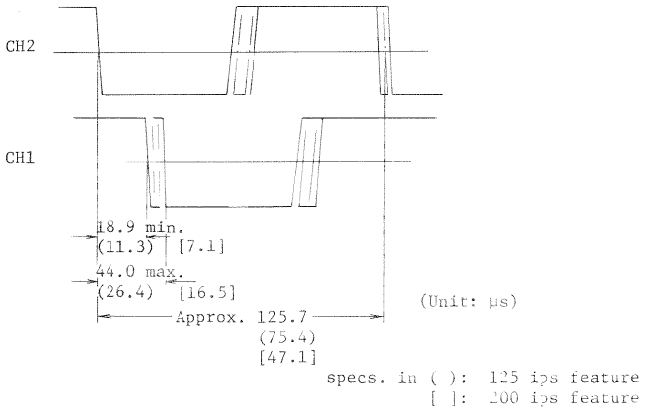


Fig. 2

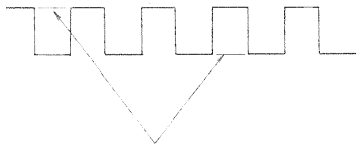
K0110-2	Capstan Tachometer Output Check (2)

III. Capstan High-speed Rotation Check

1. Remove the magnetic tape.
2. Connect a field tester with 1C05, set switches 0∿7 to $9D, and push SSS switch. The capstan motor will rotate with high speed. Then, check the tachometer.
3. If an error occurs, Unit check LED is illuminated and error code is displayed. In this case, the capstan motor rotates with insecure speed.

Correct pulse form

Incorrect pulse form



Note 1: If the requirement for capstan pulse CPA or CPB is not satisfied, adjust the potentiometer that corresponds to CPA or CPB at capstan motor (refer to Caution below).

Correspondence between pulse and potentiometer:

Pulse CPA: Pot 1
Pulse CPB: Pot 2

shown in Fig. 1.

If a requirement is satisfied, do not adjust or touch the potentiometer. If there in no hole for adjustment on cover, do not adjust it.

CAUTION

If a potentiometer is turned too far, the capstan will be in a runaway condition. If this occurs, immediately push the Door Interlock switch to stop the capstan. Return potentiometer(s) to midrange and repeat adjustment.

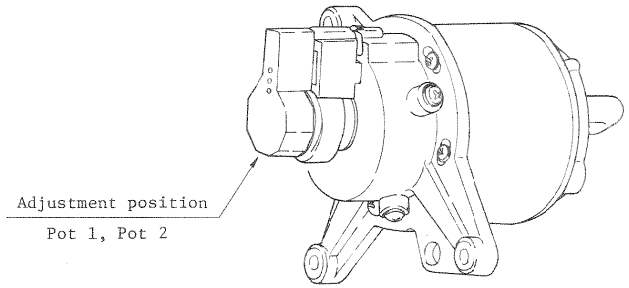


Fig. 1

K0120-1	Azimuth Check and Adjustment (1)

I. Azimuth Check

Check the azimuth according to the following procedure:

1. Demagnetize the read/write head and the erase head with a head eraser.
2. Connect a field tester and load a master skew tape.
   (P/N: BM.BvMt 351d)
3. Set the field tester to Low speed, PE mode and FWD read.
   (See Table 2.)
4. Now, trigger the read output of Track 1, and check that the phase difference with the read output of track 9 (Fig. 1) satisfies the requirements shown in Table 1. (See Fig. 2.)
5. Check that the other tracks have the same ROW output.
6. Observe the BWD (backward) operation in the same manner and check that the requirements shown in Table 1 are satisfied.
7. If the FWD or BWD operations do not satisfy the requirements shown in Table 1, an adjustment of the azimuth must be performed according to item II.

Table 1

Model	Check point			Requirement
	Track 1	Track 9	Other tracks	
125 ips 6250/1600 rpi (WRHMU)	CHAJ-1	CHAR-1	CHAK-1 ∿ CHAQ-1	FWD skew within 0.6 µs BWD skew within 1 µs
75 ips 6250/1600 rpi (WRIMU)	CHAJ-1	CHAR-1	CHAK-1 ∿ CHAQ-1	FWD skew within 1 µs BWD skew within 1.6 µs
125 ips 1600/800 rpi (WRJMU)	CHAJ-1	CHAR-1	CHAK-1 ∿ CHAQ-1	FWD skew within 0.4 µs BWD skew within 0.4 µs
75 ips 1600/800 rpi (WRKMU)	CHAJ-1	CHAR-1	CHAK-1 ∿ CHAQ-1	FWD skew within 0.7 µs BWD skew within 0.7 µs
200 ips 6250/1600 rpi (WRHMU)	CHAJ-1	CHAR-1	CHAK-1 ∿ CHAQ-1	FWD skew within 0.4 µs BWD skew within 0.6 µs

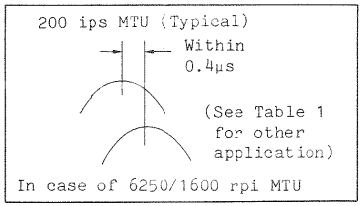


Fig. 1

Table 2 Field tester operation procedure

Procedure	Operation		Switch 0 ∼ 7	SSS	Remarks
1	Mode setting	6250/1600 rpi 1600/800 rpi	$E0 $E2	ON	MTU is in off line mode.
2	Running direction	Forward Backward	$01 $41		
3	Execution			ON	
4	Stop			ON	

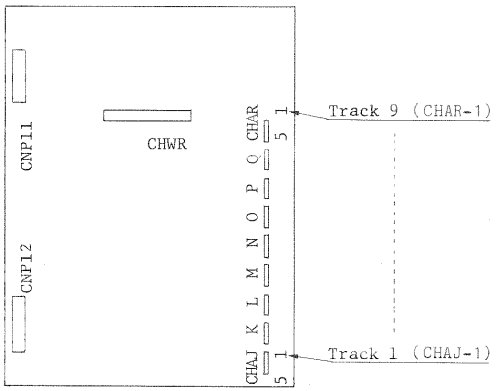


Fig. 2 Write/Read amplifier PCA

II. Azimuth Adjustment

1. Carry out adjustment of dynamic alignment. (L0130-2)
2. Trigger the read output of Track 1 and observe the phase difference with the Read output of Track 9 in the same way as in the azimuth check above. Turn the azimuth adjusting screw Ⓐ (Fig. 3) with a screwdriver and adjust the phase of the two waveforms.
3. Check that other tracks have the same ROW output.
4. Observe BWD operation in the same way and if the requirements shown in Table 1 is satisfied, no adjustment is needed.
5. If the requirements are not satisfied:
   6250/1600 rpi MTU: Turn the upper capstan alignment adjusting screw until the backward skew is within the requirements.
   (1) If track 9 leads track 1, turn the screw counter clockwise.
   (2) If track 1 leads track 9, turn the screw clockwise.
   Note: The rotation of the azimuth adjusting screw must be within 1/4 turn.
6. Check that forward skew satisfies the requirements shown in Table 1 of K0120-1, and repeat steps 4 and 5.

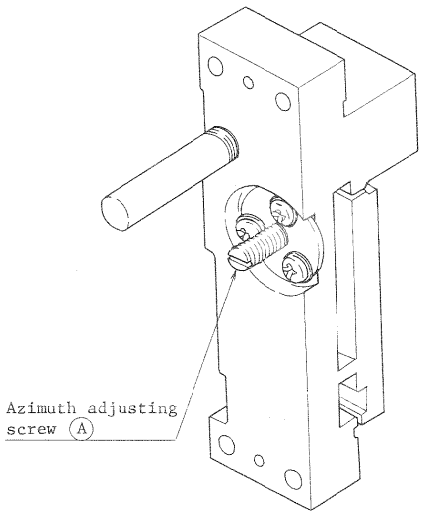


Fig. 3 Head block figure observed from back of mechanic panel

K0130-1	Read Signal Check and Adjustment, and Head Replacement Specification (6250/1600 rpi MTU)	(1)

Prerequisites for checking:

1. Clean the read/write and erase heads before checking. (See J0001.)
2. Use a tape free from damage.
3. The vacuum levels in columns shall be normal. (See K0190.)
4. Capstan alignment shall be normal. (See L0130.)

If the above prerequisites have been satisfied, then mount a field tester and load the tape. Then, check and adjust read levels for the respective modes as shown below. Some adjustment becomes necessary if any standard is not satisfied or a head has been replaced with another.

I. Low Speed PE signal check/adjustment (Including 200 ips start/stop mode)

Table 1

Item		Field tester		Operation	Standards (Statuses of LED0 to LED8)	Remarks
At check time	At adjustment time	Code	Setting switch name			
1	1	$1E	CNT	Set LEDs on the field tester to the TMSR0 to TMSR8 (register $1E) display mode.		At 200 ips mode. adjust RV4, RV5 to the middle of each range
2	2	$E8	SSS	Set the tape speed to the low speed mode.		
	3	$FA	SSS	Set the slice level to 100%.		
	4	$89	SSS	Write 3200 fci in the low speed PE mode.	Adjust RV1J to RV1R so that LEDs can be set to a semi-luminous status.	After adjustment, set the SSS switch to on and stop the tape.
3	5	$F9	SSS	Set the slice level to 90%.		
4	6	$89	SSS	Write 3200 fci in the low speed PE mode.	LED0 to LED8 shall all light.	After checking, set the SSS switch to on and stop the tape.
5	7	$FB	SSS	Set the slice level to 110%.		
6	8	$89	SSS	Write 3200 fci in the low speed PE mode.	LED0 to LED8 shall all be gone out.	After checking, set the SSS switch to on and stop the tape.

Notes: 1. A semi-luminous status is intermediate between the going-out and the most luminous status of a LED.
2. The word "lighting" refers to a status other than going-out.
3. The correspondences between LED0 to LED8 and RV1J to RV1R are as follows:

Variable resistor	RV1J	RV1K	RV1L	RV1M	RV1N	RV1O	RV1P	RV1Q	RV1R
Track No.	1	2	3	4	5	6	7	8	9
LED No.	5	7	3	8	2	1	0	6	4

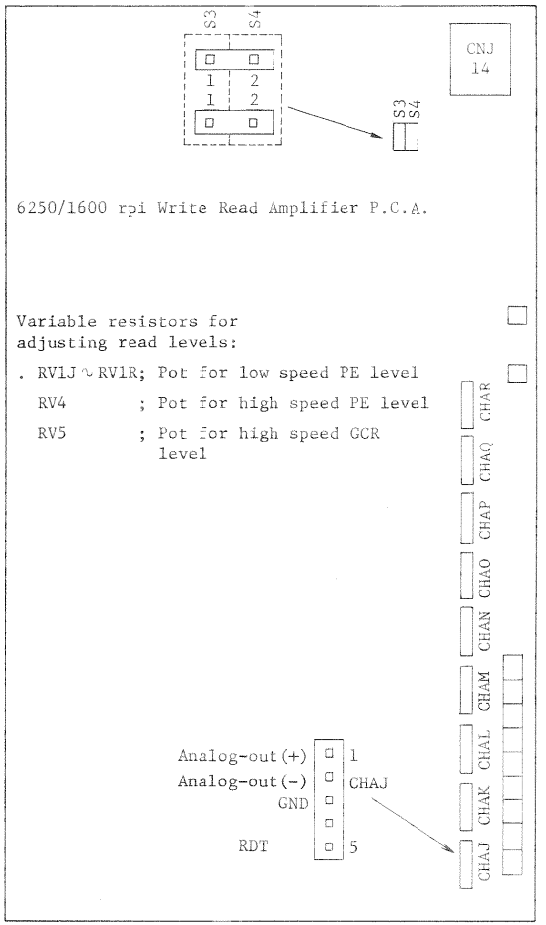


Table 5
Setting MTU model

Plug / MTU model	S3	S4
125ips	Open	Short
200ips	Short	Open

(in case of WRHMU)

RV5 (High speed GCR)

RV4 (High speed PE)

RV1R (Bit 4, Track 9)
RV1Q (Bit 6, " 8)
RV1P (Bit 0, " 7)
RV1O (Bit 1, " 6)
RV1N (Bit 2, " 5)
RV1M (Bit 8, " 4)
RV1L (Bit 3, " 3)
RV1K (Bit 7, " 2)
RV1J (Bit 5, " 1)

Fig. 1 Variable resistors and check terminals for 6250/1600 rpi MTU

II. High Speed PE signal check/adjustment

Table 2

Item		Field tester		Operation	Standards (Statuses of LED0 to LED8)	Remarks
At check time	At adjustment time	Code	Setting switch name			
1	1	$1E	CNT	Set LEDs on the field tester to the TMSR0 and TMSR8 (register $1E) display mode.		
2	2	$EC	SSS	Set the tape speed to the high speed mode.		
	3	$FA	SSS	Set the slice level to 100%.		
	4	$89	SSS	Write 3200 fci in the high speed PE mode.	Adjust RV4 so that four or more LEDs of LED0 to LED8 can light.	After adjustment, set the SSS switch to on and stop the tape.
3	5	$F5	SSS	Set the slice level to 80%.		
4	6	$89	SSS	Write 3200 fci in the high speed PE mode.	LED0 to LED8 shall all light.	After checking, set the SSS switch to on and stop the tape.
5	7	$F7	SSS	Set the slice level to 125%.		
6	8	$89	SSS	Write 3200 fci in the high speed PE mode.	LED0 to LED8 shall be gone out.	After checking, set the SSS switch to on and stop the tape.

III. Low Speed GCR signal check (Including 200ips start/stop mode)

Table 3

Item	Field tester		Operation	Standards (Statuses of LED0 to LED8)	Remarks
	Code	Setting switch name			
1	$1E	CNT	Set LEDs on the field tester to the TMSR0 and TMSR8 (register 1E) display mode.		
2	$EA	SSS	Set the tape speed to the low speed mode.		
3	$F3	SSS	Set the slice level to 51%.		
4	$C6	SSS	Set the DGC amplifier to step 6.		Since the tape runs, set the SSS switch to on and stop the tape.
5	$8B	SSS	Write 9042 fci in the low speed GCR mode.	LED0 to LED8 shall all light.	After checking, set the SSS switch to on and stop the mode.
6	$F5	SSS	Set the slice level to 80%.		
7	$8F	SSS	Perform a SAGC operation in the low speed GCR mode and write 9042 fci.	LED0 to LED8 shall all light.	After checking, set the SSS switch to on and stop the mode.
8	$F7	SSS	Set the slice level to 125%.		
9	$8B	SSS	Write 9042 fci in the low speed GCR mode.	LED0 to LED8 shall all be gone out.	After checking, set the SSS switch to on and stop the mode.
10	$F3	SSS	Set the slice level to 51%.		
11	$41	SSS	Read backward in the low speed GCR mode.	LED0 to LED8 shall all light.	Use the tape position written at item 9.

Note 1: Do not rewind the tape in the middle of performing each check item.

IV. High Speed GCR signal check/adjustment

Table 4

Item		Field tester		Operation	Standards (Statuses of LED0 to LED8)	Remarks
At check time	At adjustment time	Code	Setting switch name			
1	1	$1E	CNT	Set LEDs on the field tester to the TMSR0 and TMSR8 (register 1E) display mode.		
2	2	$EA	SSS	Set the tape speed to the low speed mode.		
3	3	$8F	SSS	Write 9042 fci in the low speed GCR mode.		After operating for one or more seconds, set the SSS switch to on and stop the tape.
4	4	$EE	SSS	Set the tape speed to the high speed mode.		
	5	$FA	SSS	Set the slice level to 100%.		
	6	$8B	SSS	Write 9042 fci in the high speed GCR mode.	Adjust RV5 so that four or more LEDs of LED0 to LED8 can light.	After adjustment, set the SSS switch to on and stop the tape.
5	7	$F4	SSS	Set the slice level to 64%.		
6	8	$8B	SSS	Write 9042 fci in the high speed GCR mode.	LED0 to LED8 shall all light.	After checking, set the SSS switch to on and stop the tape.
7	9	$F7	SSS	Set the slice level to 125%.		
8	10	$8B	SSS	Write 9042 fci in the high speed GCR mode.	LED0 to LED8 shall all be gone out.	After checking, set the SSS switch to on and stop the tape.
9		$F3	SSS	Set the slice level to 51%.		
10		$42	SSS	Read backward in the high speed GCR mode.	LED0 to LED8 shall all light.	Use the tape position written at item 8.

Note 1: Do not rewind the tape in the middle of performing each check item.

If adjustments I, II, and IV cannot be performed, then replace the head with another. If any standards of check III and check items 9 and 10 of check IV are not satisfied, then replace the head and perform checks I to IV once more.

For head replacement see L0010. If no check/adjustment can be done even after head replacement, then go to A7000.

K0140-1	Read Signal Check and Adjustment and Head Replacement Specification (1600/800 rpi MTU) (1)

Prerequisites for checking:

1. Clean the read/write and erase heads before checking. (See J0001.)
2. Use a tape free from damage.
3. The vacuum levels in columns shall be normal. (See K0190.)
4. Capstan alignment shall be normal. (See L0130.)

If the above prerequisites have been satisfied, then mount a field tester and load the tape. Then, check and adjust read levels for the respective modes as shown below. Some adjustment becomes necessary if any standard is not satisfied or a head has been replaced with another.

I. NRZI signal check/adjustment

Table 1

Item		Field tester		Operation	Standards	Remarks
At check time	At adjustment time	Code	Setting switch name			
1	1	$EC $89	SSS SSS	Write 800 fci in the NRZI mode.	Adjust RV1J to RV1R so that terminals CHAJ-1 to CHAR-1 can develope the following value: 2.0 Vp-p±10% (against the grounding). Use an oscilloscope for observation.	

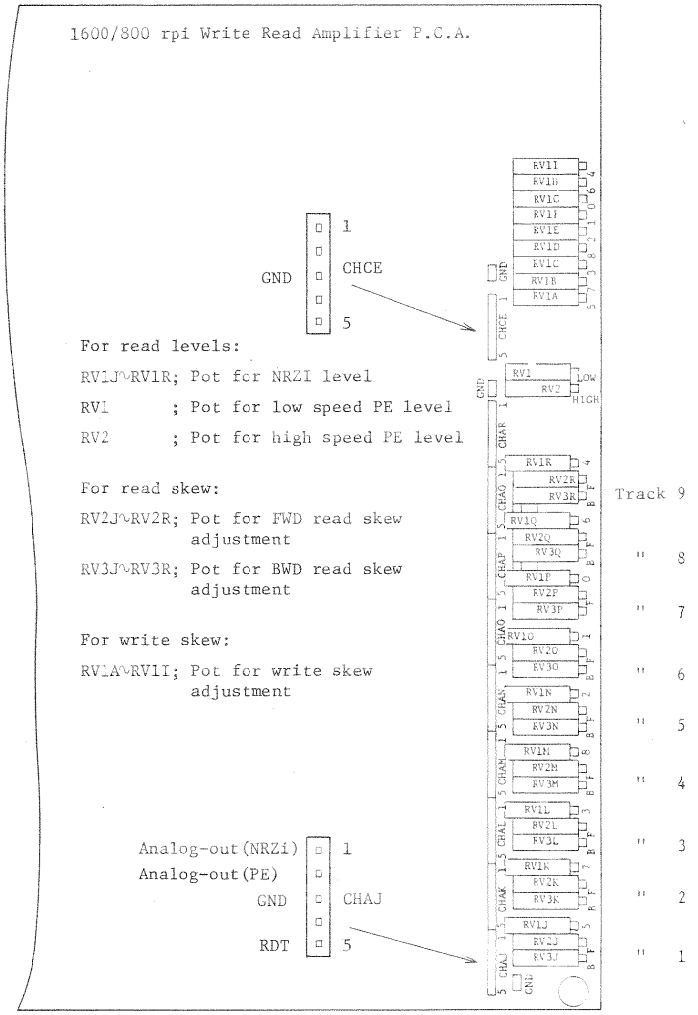


Fig. 1 Variable resistors and check terminals for 1600/800 rpi MTU

II. Low Speed PE signal check/adjustment

Table 2

Item		Field tester		Operation	Standards (Statuses of LED0 to LED8)	Remarks
At check time	At adjustment time	Code	Setting switch name			
1	1	$1E	CNT	Set LEDs on the field tester to the TMSR0 and TMSR8 (register 1E) display mode.		
2	2	$E2	SSS	Set the tape speed to the low speed mode.		
	3	$FA	SSS	Set the slice level to 100%.		
	4	$8B	SSS	Write 3200 fci in the low speed PE mode.	Adjust RV1 so that four or more LEDs of LED0 to LED8 can light.	After adjustment, set the SSS switch to on and stop the tape.
3	5	$F5	SSS	Set the slice level to 80%.		
4	6	$8B	SSS	Write 3200 fci in the low speed PE mode.	LED0 to LED8 shall all light.	After checking, set the SSS switch to on and stop the tape.
5	7	$F7	SSS	Set the slice level to 125%.		
6	8	$8B	SSS	Write 3200 fci in the low speed PE mode.	LED0 to LED8 shall all be gone out.	After checking, set the SSS switch to on and stop the tape.

III. High Speed PE signal check/adjustment

Table 3

Item		Field tester		Operation	Standards (Statuses of LED0 to LED8)	Remarks
At check time	At adjustment time	Code	Setting switch name			
1	1	$1E	CNT	Set LEDs on the field tester to the TMSR0 and TMSR8 (register 1E) display mode.		
2	2	$EC	SSS	Set the tape speed to the high speed mode.		
	3	$FA	SSS	Set the slice level to 100%.		
	4	$8B	SSS	Write 3200 fci in the high speed PE mode.	Adjust RV2 so that four or more LEDs of LED0 to LED8 can light.	After adjustment, set the SSS switch to on and stop the tape.
3	5	$F5	SSS	Set the slice level to 80%.		
4	6	$8B	SSS	Write 3200 fci in the high speed PE mode.	LED0 to LED8 shall all light.	After checking, set the SSS switch to on and stop the tape.
5	7	$F7	SSS	Set the slice level to 125%.		
6	8	$8B	SSS	Write 3200 fci in the high speed PE mode.	LED0 to LED8 shall all be gone out.	After checking, set the SSS switch to on and stop the tape.

Notes: 1. A semi-luminous status is intermediate between the going-out and the most luminous status of a LED.

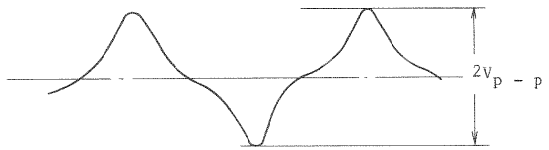
2. The word "lighting" refers to a status other than going-out.

3. The correspondences between LED0 to LED8 and tracks are as follows:

Track No.	1	2	3	4	5	6	7	8	9
LED No.	5	7	3	8	2	1	0	6	4

Track 1 corresponds to unit J; track 9 corresponds to unit R.

If adjustments I, II, and III cannot be performed, then replace the head with another. For head replacement, see L0010.



800NRZI mode

Fig. 2 Read signal waveform

K0150-1	Read and Write Skew Check and Adjustment (1600/800 rpi MTU)	(1)

Check and adjust read/write skew by taking the following steps:

I. Read skew check/adjustment

Check and adjust read skew by taking the following steps:

1. Degauss the magnetic and erasing heads with the demagnetizer (eraser) and clean the heads.
2. Mount a field tester.
3. Load a standard skew adjustment tape; check that the FILE PROTECT lamp on the operator panel is then lighting.
4. Run the tape forwards or backwards in the NRZI mode.

Operation of the field tester is as follows:

Table 1

Item	Field tester		Operation	Remarks
	Code	Setting switch name		
1	$E0	SSS	Set to the NRZI mode.	
2	$01	SSS	Forward running	The tape stops running if a BOT or an EOT is detected.
	$41	SSS	Backward running	

5. Reference track deskew pulse width check/adjustment

Check that the pulse width developed at check terminal CHAN-5 for track 5 falls into the value shown below. Adjust the pulse width for the specified value with RV2N (forward running) and RV3N (backward running).

Table 2

Speed	Checked/adjusted pulse width (tw)	Observed waveform
75 ips (for 75/125 ips device)	3.0 μs±10%	CHAN-5 tw 2.4∿5V 0∿0.4V
125 ips (for 125/200 ips device)	2.0 μs±10%	

6. Check that the rise times of pulses for the respective tracks fall into the standards as shown in Table 3 for forward and backward running when the output levels of other tracks are observed using the output level of check terminal CHAN-5 for track 5 as a reference.

Also, adjust the above rise times with RV2J to RV2R (except RV2N; forward running) and RV3J to RV3R (except RV3N; backward running).

Table 3

Speed	Running direction	Variable resistors	Check terminal	Standard (Δt) (See Fig. 1)
75 ips	Forward	RV2J to RV2R (except RV2N)	CHAJ-5 to CHAR-5 (except CHAN-5)	0.3 μs or less
	Backward	RV3J to RV3R (except RV3N)		
125 ips	Forward	RV2J to RV2R (except RV2N)		0.2 μs or less
	Backward	RV3J to RV3R (except RV3N)		

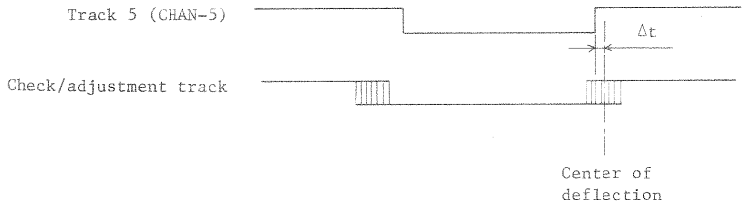


Fig. 1

Note 1: For locations of check terminals and variable resistors see Fig. 1 in K0140-1.

K0150-2	Read and Write Skew Check and Adjustment (1600/800 rpi MTU) (2)

II. Write skew check/adjustment

Check and adjust write skew by taking the following steps:

1. Load a writable tape.
2. Write 800 fci in the NRZI mode.

   Field tester code: $E0

   Field tester setting switch: SSS

   Field tester code: $89

   Field tester setting switch: SSS

3. Reference track deskew pulse width check/adjustment

   Observe the deskew clock pulse width for track 5 of the write circuit at check terminal CHCE-1 and check that the clock pulse width falls into the value shown in Table 4. Also, adjust the pulse width for the specified value with RV1E.

Table 4.

Speed	Adjusted pulse width (tw)	Observed waveform
75 ips (for 75/125 ips device)	3.0 µs±10%	CHCE-1 
125 ips (for 125/200 ips device)	2.0 µs±10%	

4. Check that the rise times of pulses for the respective tracks fall into the standards as shown in Fig. 1 when the output levels of other tracks are observed using the output level of check terminal CHAN-5 for track 5 as a reference. Also, adjust the rise time with RV1A to RV1I (except RV1E).

Table 5

Speed	Variable resistor	Check terminal	Standard (Δt) (See Fig. 1)
75 ips (for 75/125 ips device)	RV1A to RV1I (except RV1E)	CHAJ-5 to CHAR-5 (except CHAN-5)	0.3 µs or less
125 ips (for 125/200 ips device)			0.2 µs or less

Note 1: For locations of check terminals and variable resister see Fig. 1 in K0140-1.

K0160	Check for Write Voltage

1. Connect a field tester and load a writable tape.
2. Set the field tester to the write mode (in PE mode), erase mode, or read mode.
3. Check for voltage at each check point. (See Table 1.)

Table 1

Note. *; all Units

Mode / Field tester command / MTU type	Revision of PCA	Check point	Write mode		Erase mode	Read mode
			E8 (SSS) 89 (SSS)	EC (SSS) 89 (SSS)	83	01
6250/1600 rpi Mode	*	CHWR- 6	11.2±1 V		Max. +0.4 V	Max. +0.4 V
	WRHM; * WRIM; B	CHWR- 8	5.6±0.4 V		Max. +0.4 V	Max. +0.4 V
	WRIM; after E		5.2±0.4 V	5.8±0.4 V		
	*	CHWR-10	2.4±0.4 V		2.4±0.4 V	Max. +0.4 V
1600/800 rpi Mode	*	CHWR- 6	10.5±1 V		Max. +0.4 V	Max. +0.4 V
	*	CHWR-10	2.4±0.4 V		2.4±0.4 V	Max. +0.4 V

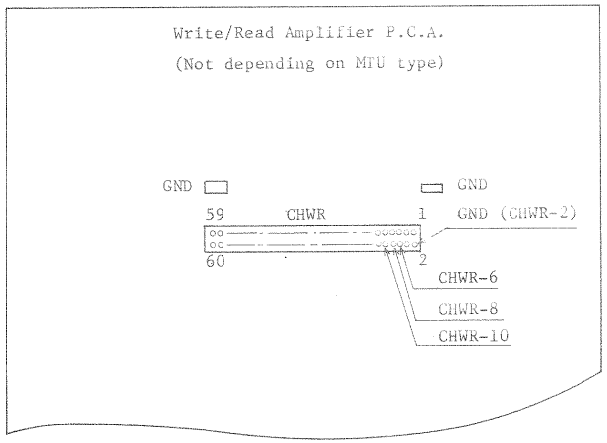


Fig. 1 Locations of check points

K0170	Check for Erase Effect

1. Prepare a tape to which all '1's have been written in the 1600 PE mode.

2. Connect a field tester and load the tape.

3. Erase the tape content by issuing an erase command from the field tester (code $80).

4. Read the tape content and check that the output levels at the respective check points are to the specifications provided in Table 1.

Table 1

MTU type	Read mode (code)	Check points	Allowable range
6250/1600 rpi MTU	PE ($E0, $01)	CHAJ-1 to CHAR-1	At most 40 mVp-p
1600/800 rpi MTU	PE ($E2, $01)	CHAJ-2 to CHAR-2	

Note: Locations of check points show the K0130-1 Fig. 1 (6250/1600 rpi MTU) or K0140-1 Fig. 1.

K0180	Check of Hose and Tube

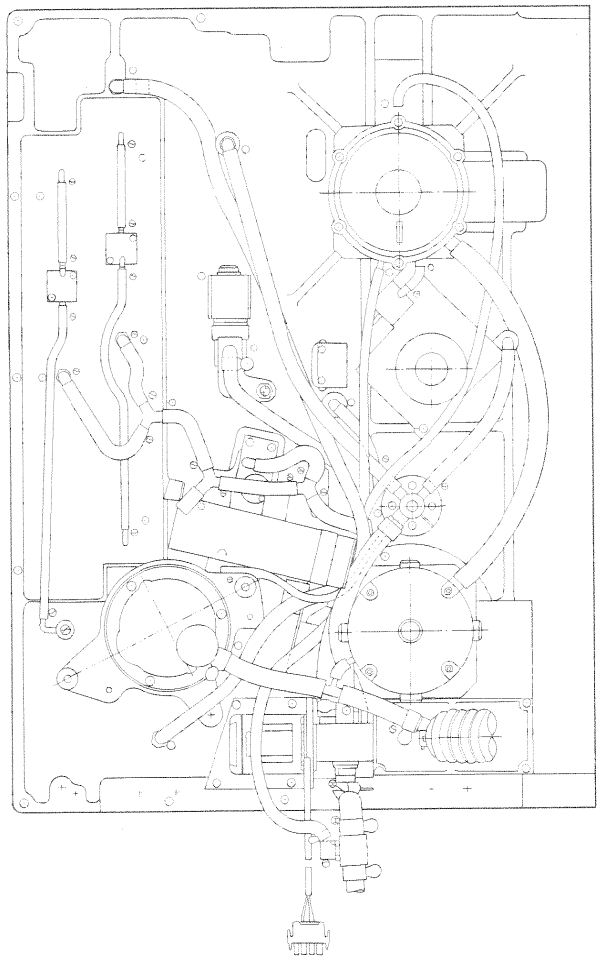
Procedure:

(1) Check to be sure that no cracks or other problems exist on the hoses and tubes.

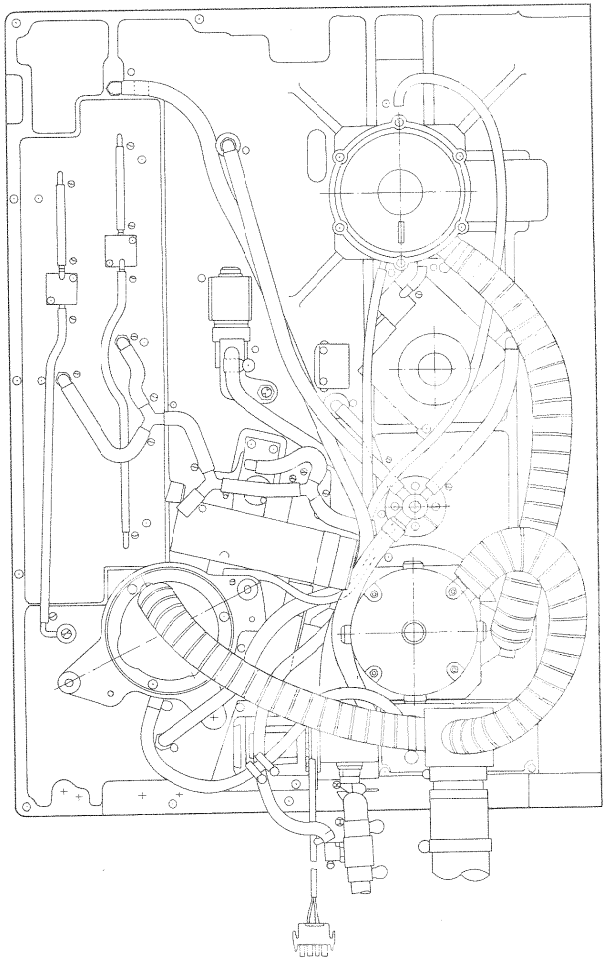
(2) Check for loose connection of tubes or disconnected tubes.

(3) Check for folded hose or disconnected hose.

Pictorial: 1 75/125 ips MTU



Pictorial: 2 200 ips MTU



K0190	Check and Adjustment of Pressure and Vacuum Levels

Checking and Adjusting Pressure

Checking Procedure:

During Threading

(1) Connect a pressure gauge to Restraint Number Pressure Port C.

(2) Mount the Special Tool (B960-0110-T026A) on the air outlet of restraint-member.

(3) Check if the pressure is within Table 1 check specification.

During Servo On

(1) With the tape loaded into the columns, connect the pressure gauge to servo on pressure port B.

(2) Check if the pressure is within Table 1 check specification.

Adjusting Procedure:

During threading

Adjusting the Distributor screw so that the pressure is within Table 1 adjust specification (Enter A5 into tester)

During Servo On

Adjust the pressure relief valve (See Fig. 1) that the pressure is within Table 1 adjustment specification.

Note 1. When adjusting pressures/vacuum levels the following sequence shall be observed.

1 Vacuum Column
2 Servo On Pressure
3 Restraint Pressure

Note 2. In order to accurately check and adjust the vacuum and pressure levels it is necessary to allow the pneumatics assembly to thermally stabilise. Adjustments and measurements are therefore to be made to the time frames indicated in Table 1.

Table 1

Measuring port	All Figures mmH_2O	Check within	Adjust to
A	Vacuum Column	950 ± 50	950 ± 30
B	Servo on Pressure	2600 ± 50	2600 ± 30
C	Restraint Pressure	650 ± 30	650 ± 15
		Only after running for at least 10 minutes	Only after running for at least 30 minutes

Checking and Adjusting Vacuum Levels

Checking and Adjustment Vacuum Pressure

Checking Procedure:

(1) Connect the vacuum gauge to column vacuum measuring port A.

(2) Check if the vacuum level is within Table 1 check specification.

Adjusting Procedure:

Adjust the vacuum Restrictor so that the vacuum level is within Table 1 adjustment specification.

Note: Refer to Manual Sheet L0350 for parts layout such as check ports and restrictor.

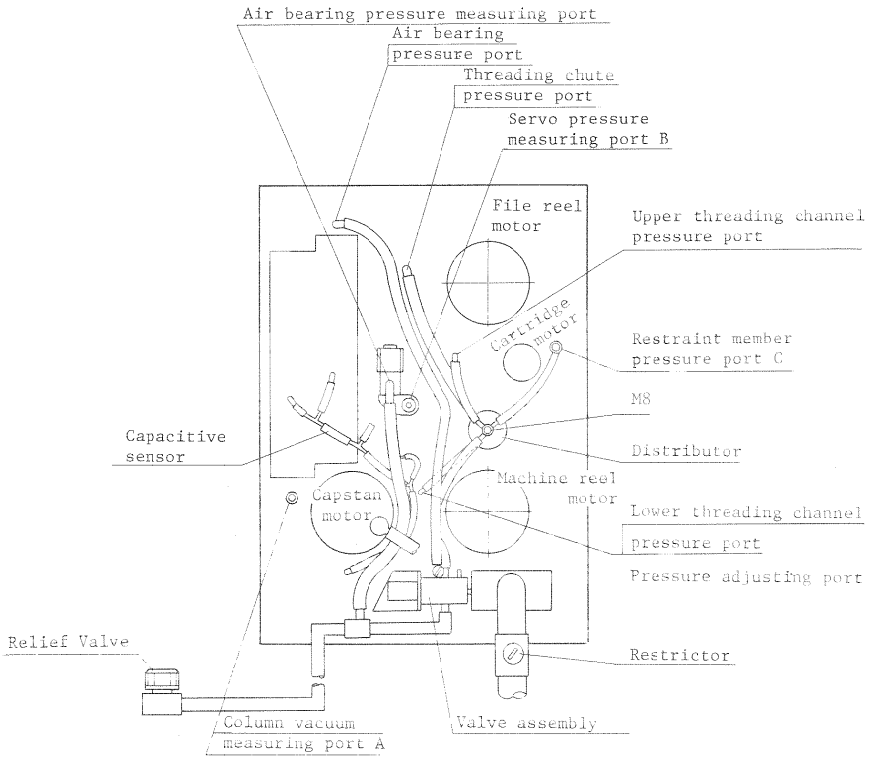


Fig. 1

K0191-1	Frequency Setting (1)

Exchange large pulley, belts and the connections of CNP66, CNP66C, if necessary. (Refer to Fig. 1)

1. Exchange of connector positions

   Exchange the connections of CNP66 and CNP66C. (See Fig. 1.)

2. Exchange of large pulley and belts

   1. Remove pulley and belts from the air supply cabinet. (In this case, detach fitting bolts.)
   2. Detach the fitting bolts of the air supply cover and remove that cover.
   3. Loosen the fitting bolts Ⓐ (for the blower) and fitting bolts Ⓑ (for the pump) and remove the bolts respectively. (See Fig. 2. ... Next page)
   4. Remove the fitting bolts (for the blower pulley) and fitting bolts (motor pulley on the pump side).
   5. After replacing each pulley, attach a new belt and perform frequency conversion between 50 Hz and 60 Hz. (See Fig. 3.)
   6. Check and adjust belt tension. (Refer to K0200.)
   7. Check and adjust the pressure and vacuum level. (Refer to K0190.)

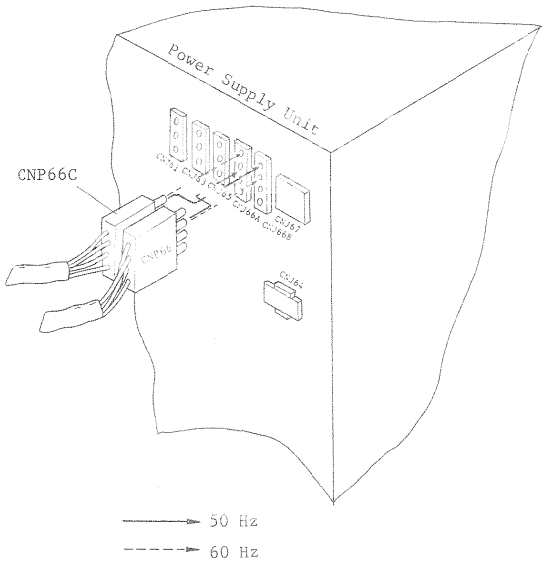


Fig. 1

K0191-2	Frequency Setting (2)

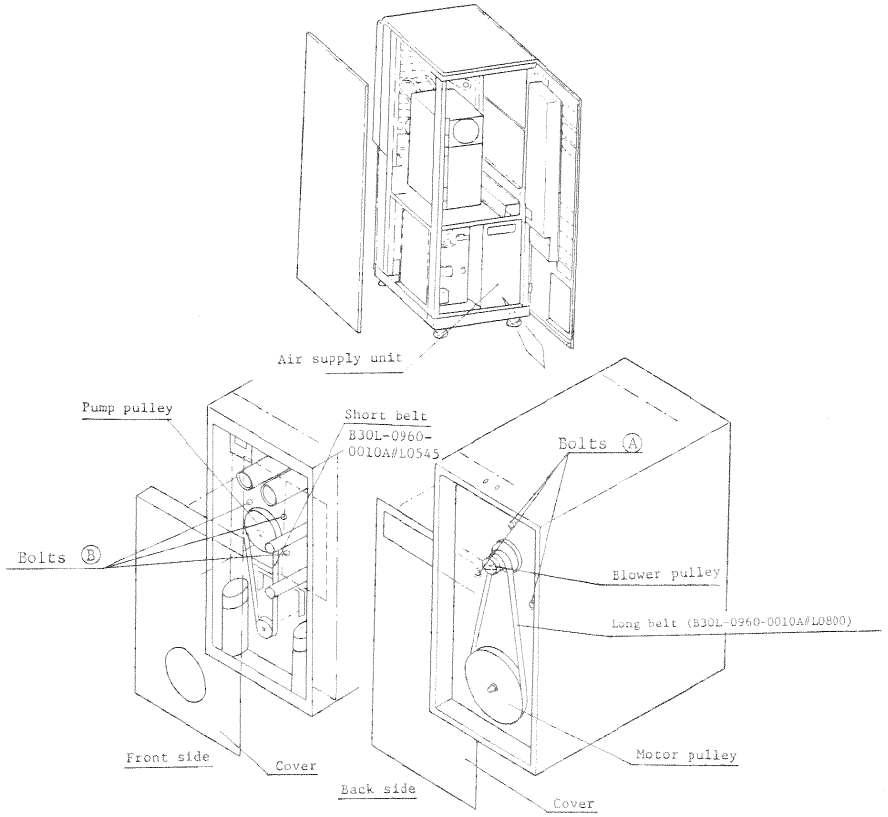


Fig. 2

K0191-3	Missing Description for altitude Setting (3)

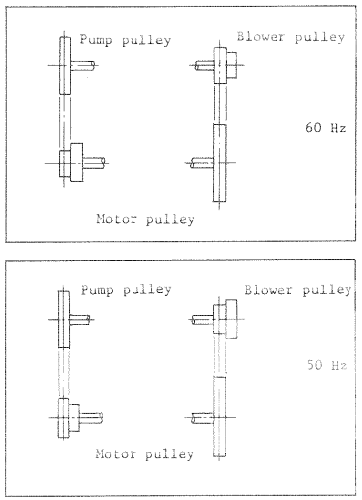


Fig. 3

K0200	Belt Tension Check and Adjustment

1. Detach the fitting bolts of the rear and front of MTU and remove the air supply from the rear of unit.

2. Remove the front and rear covers.

3. Measure the belt tension with a tension meter.

   Turn the motor pulley 3 to 5 turns by hand before measurement. Snap the belt as shown in Fig. 3, push up the lever with a finger as shown in Fig. 2, 3 and read the value in pound at the time when the back of the belt comes into contact with "A" part indicated by the arrow in Fig. 3.

4. Adjust the belt tension by shifting the fixing position of the blower or pump.

   - o If the belt is to be replaced, the new belt must be adjusted so that the tension level required in Table 1 are satisfied.
   - o If the old belt is to be used again, measure its tension before removing it, and adjust the belt to that tension when putting it back on. (Set the belt in same direction as removing).

Table 1

Belt	Required value	Adjusted value	
		New belt using	Old belt using
Belt between motor and blower (longer belt)	16.5 (lbs) or more	29∿34 (lbs)	Original tension (Refer to Note 2.)
Belt between motor and pump (shorter belt)	12.5 (lbs) or more	29∿34 (lbs)	

Note 1: The belt tension repidly deteriorates in several days ∿ several months. If the required value is not satisfied, the belt must be replaced.

2: Since the old belt has been extended, its life may be extremely shortened if its tension is adjusted to the adjusted value for a new belt.

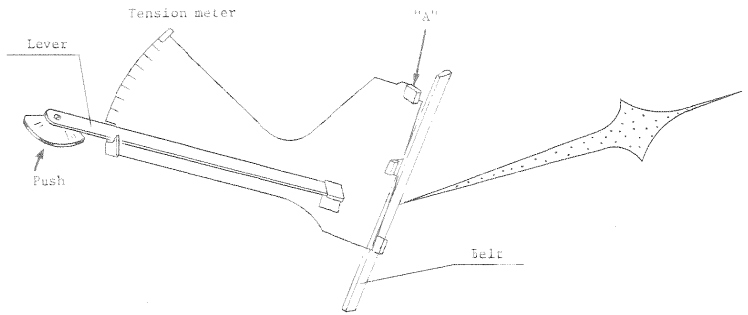


Fig. 3

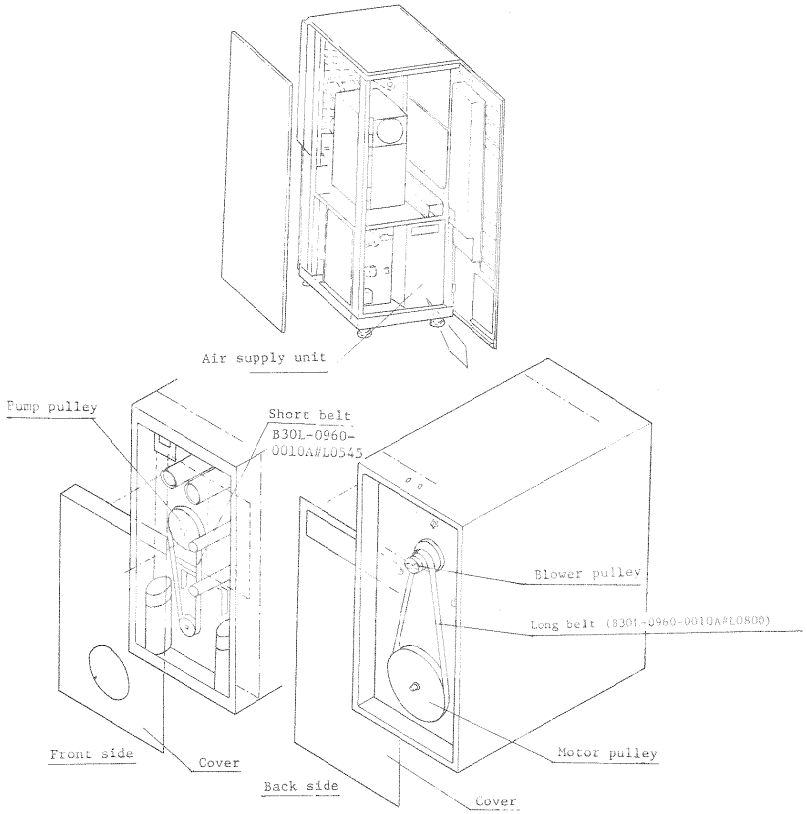


Fig. 2

K0210 Check and Adjustment of BOT and EOT Detection Circuits

1. Prepare a new magnetic tape and two new reflective markers. Attach these markers to the magnetic tape as shown in Fig. 1.
2. Without the tape being loaded, adjust the voltage level at check terminals "BOT" and "BOT" with degital voltmeter to 2.0 V with the poteniometer "RV5" and "RV6" respectively on the tape drive PCA.
3. Connect a field tester and load the tape prepared in step 1 above.
4. After the tape stopped at the BOT, measure the check terminal "BOT" level. If the level is lower than 2.0 V adjust the level to +1.6 V by the potentiometer "RV5" again.
5. Set the field tester to FWD, CONTI, and READ (Command code: $01) and run the tape.
6. After the tape has stopped at the EOT, check that the "BOT" level is lower than +0.3 V.
7. Measure the "EOT" level. If the level is lower than 2.0 V adjust level to +1.6 V by again.
8. Set the field tester to REW (Command code: $47). After the tape has stopped at the BOT, check that the "EOT" level lower than +0.3 V.

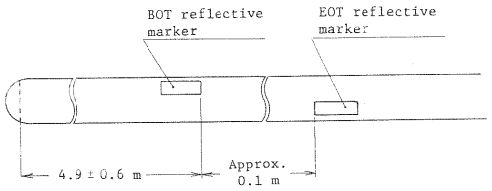


Fig. 1

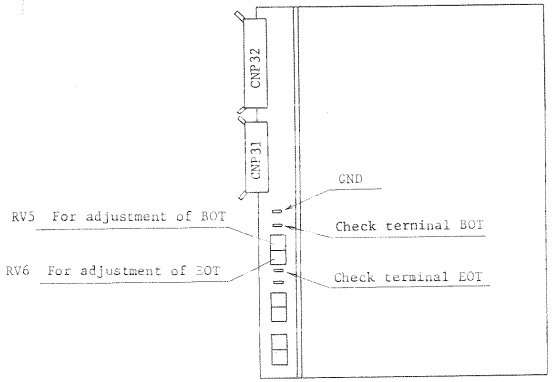


Fig. 2 Tape Drive PCA (TKBMU or TKHMU)

K0220 Check of Low Tape Detection Circuit

Check the low tape detection circuit according to the following procedure.

1. Without the tape being loaded, connect the field tester.
2. Set the field tester to Machine Reel FWD (Command code: $D2).
3. Check that check terminal "1A01 AB8" output voltage level is +1.4 Vp-p or more. (Fig. 3)

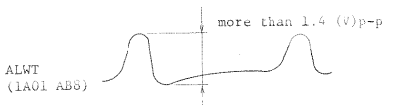


Fig. 3 Low Tape Output

K0240	Check and Adjustment of Tape Loop Position Detection Circuit

1. Confirm that the column vacuum and the pressure of capacitive sensor satisfy the requirements. (Refer to K0190.)

Column vacuum	950 mmH_2O ± 10%
Pressure of capacitive sensor	240 mmH_2O

2. Do a load, pull tape from columns and hit reset twice.
3. Turn on the air supply with a field tester (Command code: $A8 and SSS switch on), feed the tape inside the column, and fix the tape loop at F0 and M0. (See Fig. 1.)
4. Adjust RV2F and RV2M of TKBMU or TKHMU, which is mounted on 1A04, to approximately 50%.
5. Adjust RV1F and RV1M so that the output voltage of the sensor satisfies the following requirements:

Check position	Sensor output voltage
File reel: LSF (TKBMU or TKHMU) or AD8 (1A01)	0 ± 0.2 V
Machine reel: LSM (TKBMU or TKHMU) or AE7 (1A01)	0 ± 0.2 V

6. Set Switch 6 of the field tester on (Command code: $AA). The loop of the magnetic tape will stop at position F1 and M1. Under this condition, adjust RV2F and RV2M so that the absolute value of the voltage on the check position is in the range of 6.5 V ± 0.2 V.
7. Set Switch 7 of the field tester on (Command code: $AB). The loop of the magnetic tape will stop at positions F2 and M2. Under this condition, if the absolute value of the voltage on the check positions is below 6.5 V, adjust RV2F and RV2M so that it satisfies 6.5 V ± 0.2 V.
8. Set off Switch 7 of the field tester (Command code: $AA) and check that the voltage at each check point is about 6.5 V ± 0.2 V (Absolute).
9. Set on SSS to terminate the test.

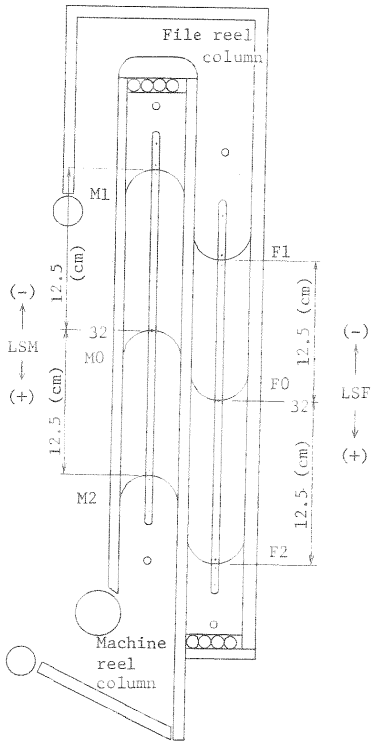


Fig. 1

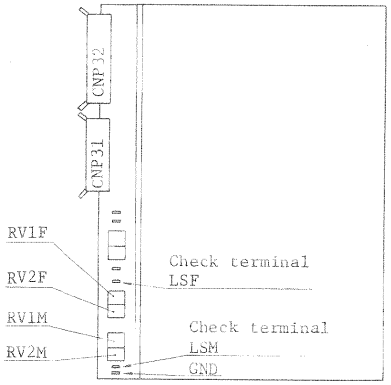
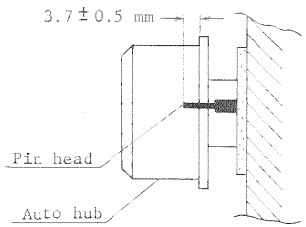


Fig. 2 Tape drive PCA (TKBMU or TKHMU)

K0260	Check and Adjustment of File Protection Mechanism

Check and adjustment of the file protection mechanism is performed by confirming the position of the pin head of the file protection both in a usual state and when the magnetic tape with enable ring loaded.

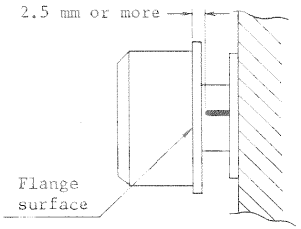
1 Usual state



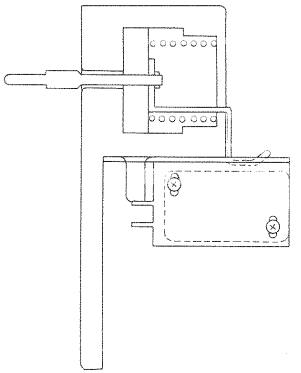
2 When magnetic tape with enable ring is loaded

Push the pin head as far as the flange surface, and press the LOAD/REWIND button. Check that the distance between flange surface and pin head is 2.5 mm or more.

The file protection must be replaced if the specified value is not satisfied.



3 Push the pin head with a hand. Check that the micro switch is actuated before the pin point is moved 1 to 2.8 mm.
If not, remove the file protection from the panel and adjust the position of the micro switch.



K0280	Check and Adjustment of Front Door Synchronous Belt Tension

If there is a problem concerning the tension of the front door synchronous belt, check and adjustment are performed in accordance with the procedures described below.

Measuring instrument:

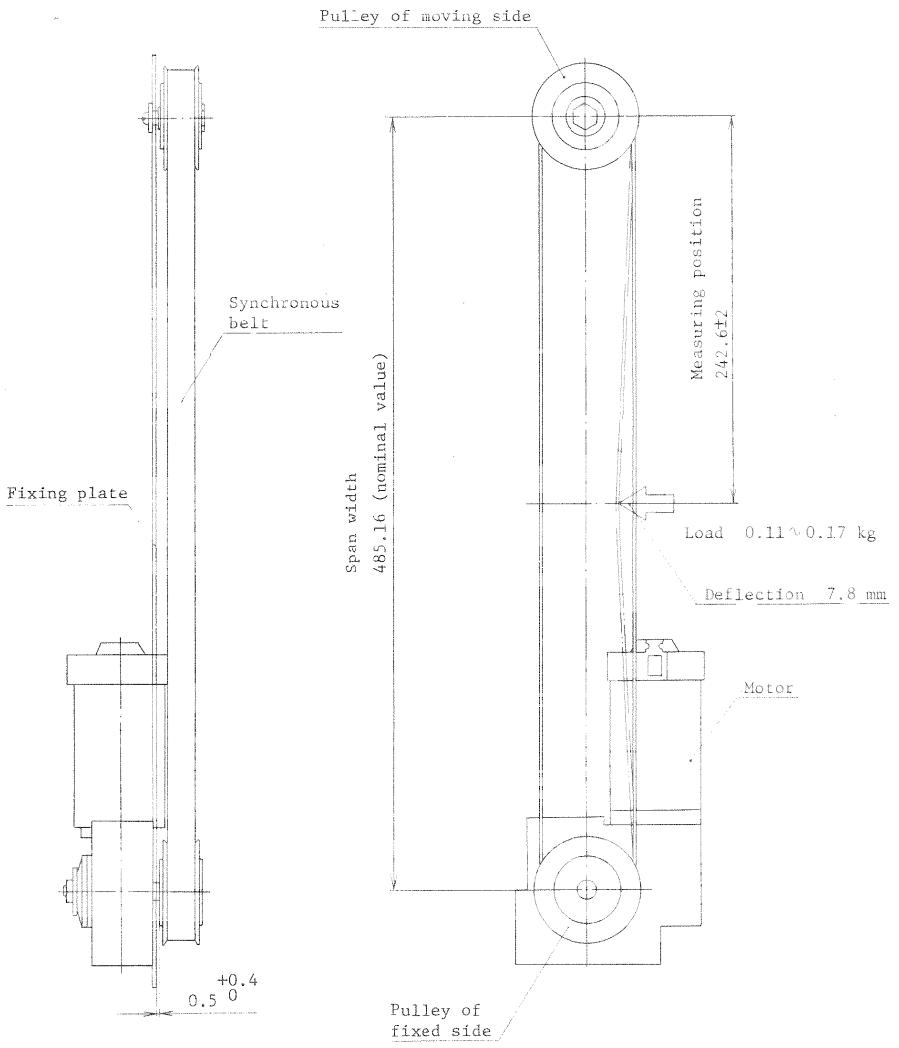
Spring scale (1 kg maximum)

Check Procedures:

Place the spring scale against the belt at the position indicated by the arrow. When the belt deflection is about 7.8 mm, the belt shall be pushed straight up with 0.11 ∿ 0.17 kg force. For the measurement, slide-rail part must be removed from the belt and the belt must be free.

Adjustment Procedures:

Belt tension adjustment is performed by loosening one fixing screw of the pulley on moving side and moving the pulley up or down.



K0290	Check of Auto Cleaner

1. The auto cleaner can be positioned with the guide pins on the magnetic head. (See Fig. 1.)

2. Check that the ribbon is taut and is properly mounted on the ribbon guide and slide part.

   If it is loose, depress the load button after turning the power on. Then the motor turns automatically and the sag is eliminated.

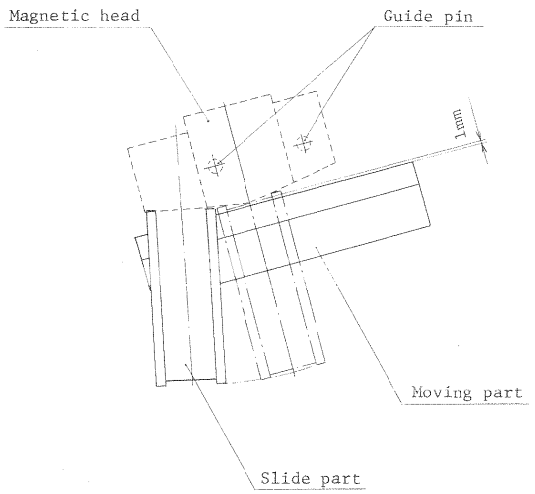


Fig. 1 Magnetic head and auto cleaner

L0000	Parts Replacement Procedure

General Precautions

1. In general, the power supply must be turned off for replacing part.
2. Correctly calibrated tools must be used.
3. Any work designated to be performed by two CE's nust not be performed by one CE alone.
4. Be careful not to loss any removed screws, washers, and nuts.
5. Any parts that fall into the equipment must always be removed.
6. Remember the conditions prior to replacement for the convenience of checking the conditions and performances after replacement.
7. In replacement of PCA with Green Mark, you must check and adjust.

MTU Parts Replacement Procedure

Item	Parts name	MAP No.
1	Read/write head	L0010
2	Erase head	L0020
3	Read/Write PCA (Write Read amplifier)	L0030
4	Threading channel	L0040
5	Tape cleaner	L0050
6	EOT/BOT sensor	L0060
7	Tape guide	L0070
8	Roller guide	L0080
9	Auto cleaner	L0110
10	Capstan motor	L0130
11	Threading chute and restraint member	L0140
12	Cartridge opener	L0150
13	Error marker	L0160
14	File protect mechanism	L0170

Item	Parts name	MAP No.
15	Auto hub	L0180
16	Cover assembly	L0190
17	Latch	L0200
18	Cam assembly	L0210
19	Rear housing assembly	L0220
20	Machine reel	L0230
21	Low tape sensor	L0250
22	Reel motors	L0260
23	Vacuum column cover	L0270
24	Vacuum column section	L0280
25	Micro switch for opening/closing glass	L0300
26	Front door clutch section	L0310
27	Valve ASM vacuum and pressure	L0330
28	Restrictor	L0350
29	Fan unit	L0360
30	Cooling air filter	L0370
31	Absolute filter	L0380
32	Air supply unit	L0400
33	Threading cover	L0410
34	Cartridge sensor	L0420
35	Capacitive sensor	L0430
36	Power supply unit	L0440
37	Operator panel	L0450
38	Door switch	L0460
39	Rib	L0470

L0010	Replacement of Read/Write Head

Procedure:

[Removing]

1. Remove FPC board connectors and frame ground terminal from the head.
2. Loosen erase head set screws, and remove erase-head from its plate.
3. Loosen the block screws, and remove the block.
4. Loosen the two head plate set screws, and remove the head base from head block.

[Mounting]

1. Place the head plate onto the plate positioning pin, and then place and tighten two screws other than those for erase head and head block.
2. Place the block in position by using the positioning pin, and tighten screws with holding the block onto head.
3. Place erase head in position using positioning pin, and tighten screws with holding the head onto the other pin.
4. Connect FPC board connectors and fix the frame ground terminal.
5. Check the Azimuth. (Refer to K0120, K0130)

L0020	Replacement of Erase Head

Procedure:

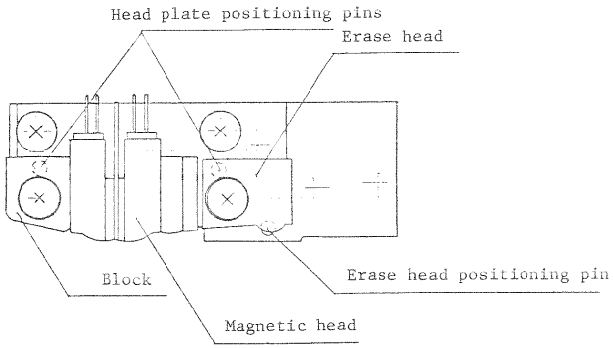
[Removing]

1. Remove connectors.
2. Remove screws and erase head.

[Mounting]

1. Place erase head onto its positioning pin, and tighten screws with holding the head onto the other pin.

Fig.



L0030	Replacement of Read/Write PCA

Be sure to turn off power before replacement of the Read/Write PCA.

Removal

1. Open the column cover and threading cover, detach the ground terminal screw of the FPC cable, and remove the erase connector (CNJ03). (See Fig. 1.)
2. Detach the following connectors, which are connected with Read/Write PCA on the back of the unit. (See Fig. 2.)

   Read FPC cable, Write FPC cable, interface connector (CNJ13) and Power supply connector (CNP14)
3. Pull the neightlatch and remove Read/Write PCA, being careful not to damage the PCA.

Mounting

1. Set or check the MTU model setting plug in case of WRHMU (K0130)
2. Put Read/Write PCA on a leading groove and set the nieghtlatch.
3. Attach all the connectors and the ground terminal screw.

Confirmation and adjustment:

1. Write voltage - (K0160)
2. Read signal level - (K0130, K0140)
3. Read and write skew - (K0150)

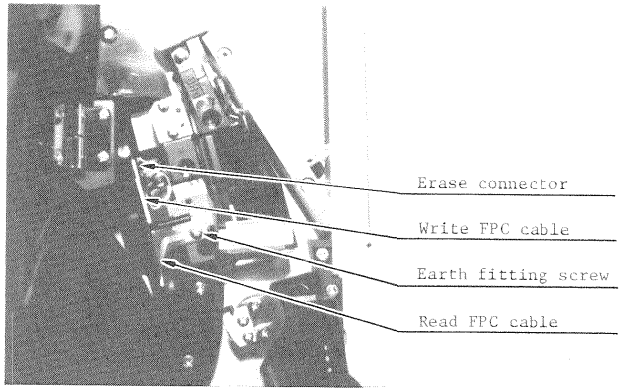


Fig. 1

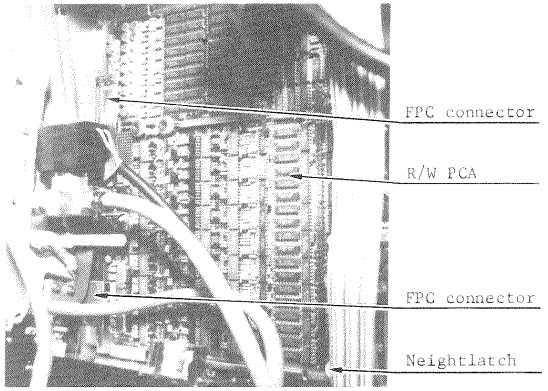


Fig. 2

L0040	Replacement of Threading Channel

Procedure:

[Removing]

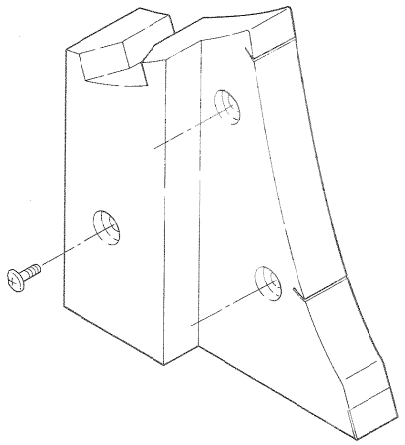
1. Open both the column covers and threading covers.
2. Remove either three setscrews and upper channel or two setscrews and lower channel.

[Mounting]

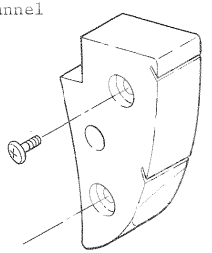
Place the upper or lower channel onto its positioning pin, and tighten screws. (Note: Use three screws for mounting upper channel, while use two screws for lower channel.)

Fig.

Upper channel



Lower channel



L0050	Replacement of Tape Cleaner

Procedure:

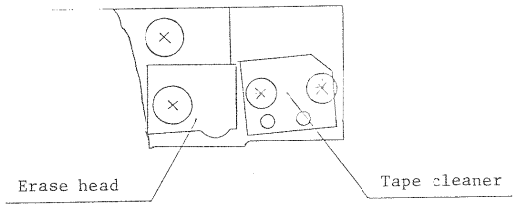
[Removing]

Remove two screws and tape cleaner.

[Mounting]

Place the tape cleaner onto its positioning pin, then tighten two screws.

Fig.



L0060	Replacement of EOT/BOT Sensor

Procedure:

[Removing]

1. Pull out connector (CNJ54) from the photosensor-block.
2. Loose the two screws and remove the photosensor-block.

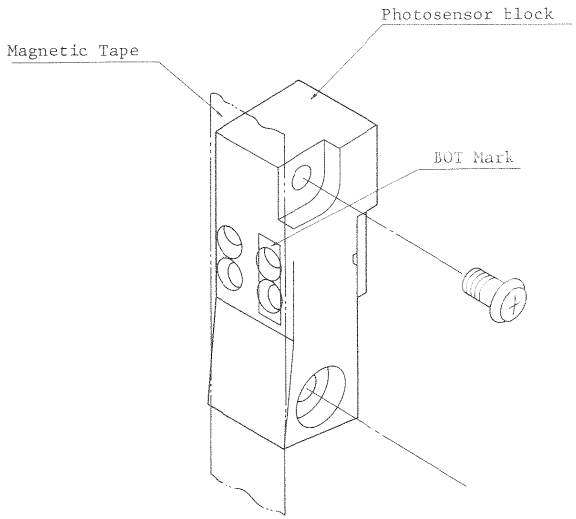
[Mounting]

1. Place photosensor block onto its positioning pin, and tighten two screws.
2. Insert the connector into photosensor block.

Checkout:

Check and adjust the BOT and EOT detector circuits.

Fig.



L0070-1	Replacement of Fix Upper and Lower Tape Guides (6250/1600 rpi MTU)

Procedure:

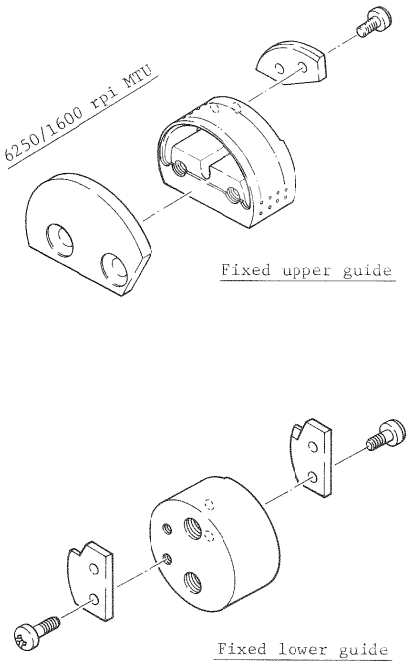
[Removing]

1. Remove two setscrews and the upper or lower guides.
2. Remove fixed flange from the guide.

[Mounting]

Perform the reverse procedure above.

Fig. 1



L0070-2	Replacement of Moving Upper and Lower Tape Guides (1600/800 rpi MTU)

Procedure:

[Removing]

1. Remove two setscrews and the upper or lower guide.

   Note: Each moving guide has a spring at its flange. Keep the spring when handling moving guides.

2. Remove moving flange from the guide by removing setscrew from the insulator.

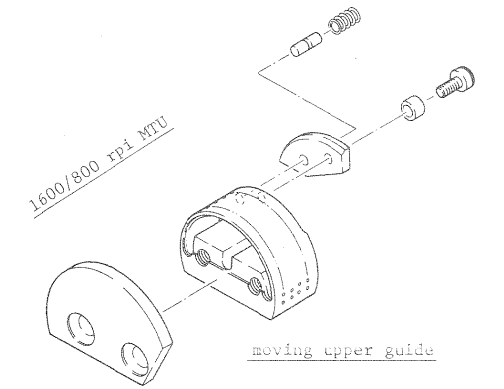
[Mounting]

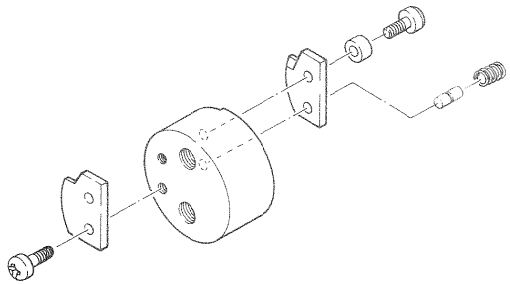
Perform the reverse procedure above.

Checkout:

Check to be sure that the assembled moving flange moves smoothly.

Fig. 1





L0070-3	Checking Guides

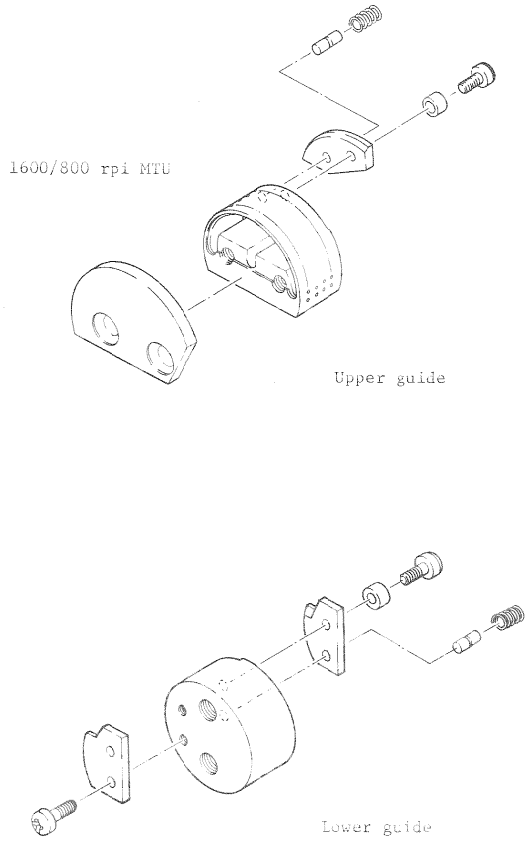
Procedure:

(1) Remove upper and lower channels, and clean upper and lower guides and around of them. (See Manual Sheet L0070-2 for cleaning procedure.)

(2) Check for scratches or grooves due to wear on the guide face and flange.

(3) Replace damaged parts (L0070-2).

Fig.



L0080	Replacement of Roller Guide

Procedure:

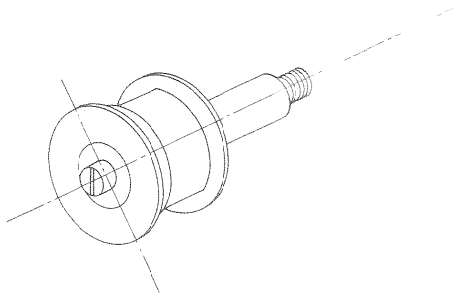
[Removing]

Insert the flat-blade screwdriver into the slit of roller guide and rotate it counterclockwise.

[Mounting]

Insert and rotate the flat-blade screwdriver to tighten the roller guide.

Fig. 1



L0110	Replacement of Auto Cleaner

Procedure:

[Removing]

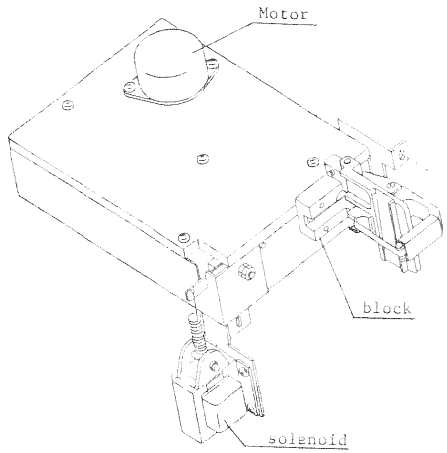
1. Remove two setscrews.
2. Remove auto cleaner.

   Note: Do not contact auto cleaner to the head when removing it.

[Mounting]

1. Place auto cleaner onto its positioning pin at the rear of block, and push down the cleaner until it reaches block.
2. Tighten two setscrews.

Fig. 1



L0130-1	Replacement of Capstan Motor (1)

Procedure:

(Removing)

1. Disconnect connectors CNJ51 and CNP82.
2. Loosen the nut of spring section and remove both vasher and spring.
3. Carefully take out the motor.
   Note: Take care not to damage the capstan roller.
4. Remove the tube or hose.

(Mounting)

1. Connect the tube to the air suction pipe. (incase of 200ips MTU)
2. Mount the motor onto the shaft of spring section and insert the motor until it atops at the bolt.
   Note: Take care not to damage the capstan roller
3. Mount the spring and whasher, and then tighten the nut 9 to 9-1/2 turns to compress the spring from its free length.
4. Connect connectors CNJ51 and CNP82.

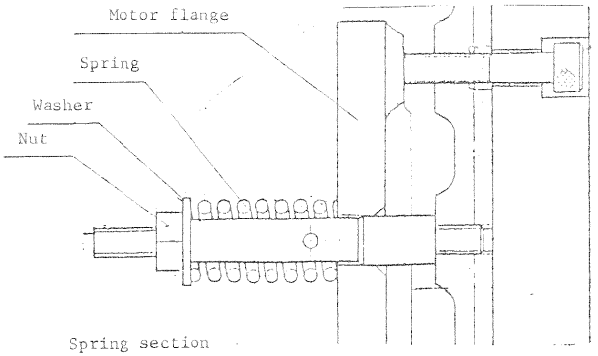
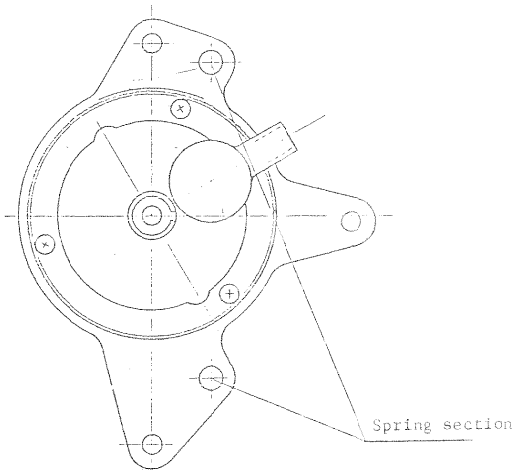


Fig. 2

Fig. 1



Capstan motor rear view

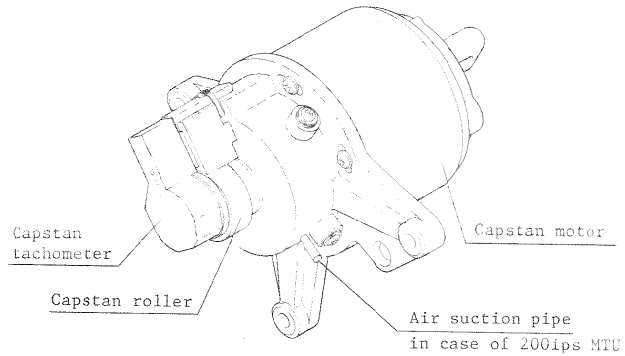


Fig. 3

L0130-2	Replacement of Capstan Motor (2)

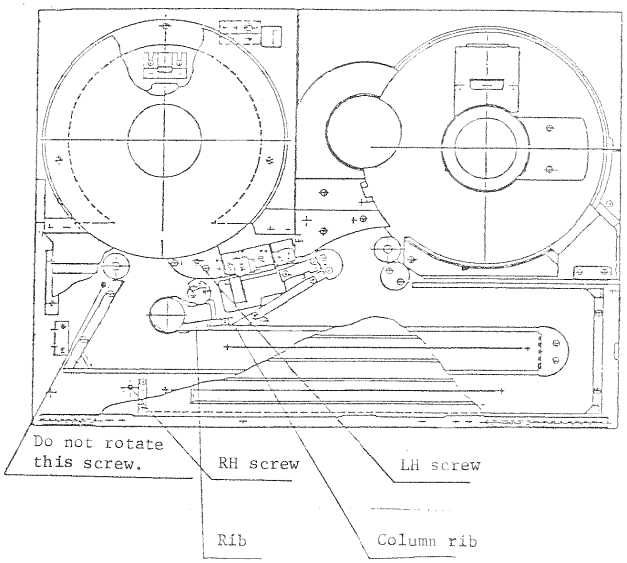
Precautions:

1. Perform alignment adjustment whenever the capstan motor has been replaced.
2. Use a tape in good order (do not use a worn tape) and being 12.63 to 12.65 mm wide.
3. Mount against the rib onto column rib so that the largest clearance is obtained between capstan and rib (X018A).
4. If the adjusting screw is required to be rotated two turns or more, take care the clearance between capstan, rib and casting face, or the capstan may be damaged.
5. During adjustment, check for the correct tape speed.

Adjustment Procedure:

1. Load the tape and set column-in, then remove the threading cover and lower channel.
2. Remove the front flange of lower tape guide, and mount the tape guide.
3. Feed the tape in FWD (Cont) mode, and adjust the adjusting LH screw so that the front edge of tape is just at the edge of tape guide.
4. Select the REW (Cont) mode, and adjust the adjusting RH screw so that the front edge of tape is just at the edge of tape guide.
5. Repeat an item 3 and 4 until the front and rear of tape does not move when switch over FWD (Cont) and REW (Cont) modes.

Fig. 4

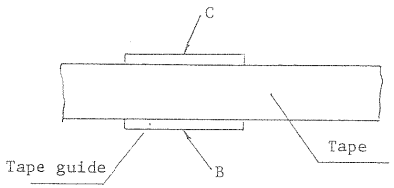


6. After the adjustment above, rotate both the RH and LH adjusting screws clockwise. When the tape is in FWD (Cont) or REW (Cont) mode, the surface guide of its portions B and C must slightly be observed (for type A), or the surface guide of portion B must slightly be observed (for type E).

   Note: An excessive tape edge shaking in the transverse direction requires to perform the adjustment again.

7. Remove the tape and mount all the remaining parts.

Fig. 5



L0130-4	Electrical Check of Capstan Motor (1)

I Check of Capstan Starting Time/Stop Time (Normal mode)

1. In the servomechanism-on state(means tape loaded), set command code $E0 with a field tester to put the unit in Normal mode.

2. Set command code $30 and perform Forward Start/Stop operation.

3. Trigger the leading edge of signal CAPGO (at 1A05 AAV), and then check that the time T shown in Fig. 1 satisfies the specifications in Table 1.

4. Check the time Ts shown in Fig. 2 satisfies the specifications in Table 2.

5. Set command code $6A and perform the Backward Start/Stop operation, and then check the time T, Ts in the same manner as above.

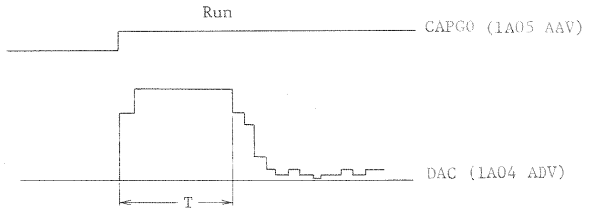


Fig. 1 DAC output

Table 1 Specification of starting time T

Running direction	Starting time T			Check position
	75 ips MTU	125 ips MTU	200 ips MTU	
FWD	1.50 ∿ 2.00 ms	0.70 ∿ 1.10 ms	0.70 ∿ 1.10 ms	DAC (1A04 ADV)
BWD	1.80 ∿ 2.70 ms	0.90 ∿ 1.25 ms	0.80 ∿ 1.20 ms	

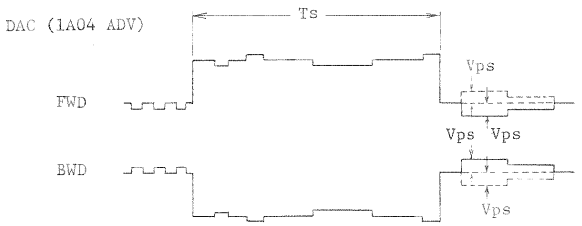


Fig. 2 DAC output

Table 2 Specification of stop time Ts

Model	Stop time Ts (FWD/BWD)	Vps	Check position
75 ips	2.15 ± 0.2 ms	Max. 1.0 V	DAC (1A04 ADV)
125 ips	1.30 ± 0.2 ms	Max. 1.7 V	
200 ips	1.20 ± 0.3 ms	Max. 1.7 V	

II Check of Capstan Starting Time/Stop Time (Streaming mode)

1. Set command code $E4 with a field tester and put the unit in the Streaming mode.

2. Set command code $25 and perform the Forward Start and Stop operation. (See Fig. 3.)

3. Trigger the leading edge of signal ACT (at 1A05 BE7), and then check that the time Tst and Tsp shown in Fig. 3 or Fig. 4 satisfies the specification in Table 3.

4. When it is in Streaming mode, the start and stop time can be measured by moving the tape in forward or backward direction.

   The Backward Start/Stop operation is performed by command code $65. (See Fig. 4.)

Table 3 Specification of starting time Tst and stop time Tsp

Model	Direction	Tst	Tsp	Vco
125 ips	FWD	2.8 ∿ 3.9 ms	1.3 ± 0.2 ms	±1.7 V or less
	BWD	2.4 ∿ 3.6 ms		
200 ips	FWD	1.4 ∿ 1.9 ms	2.5 ± 0.2 ms	±1.7 V or less
	BWD	1.3 ∿ 1.8 ms		

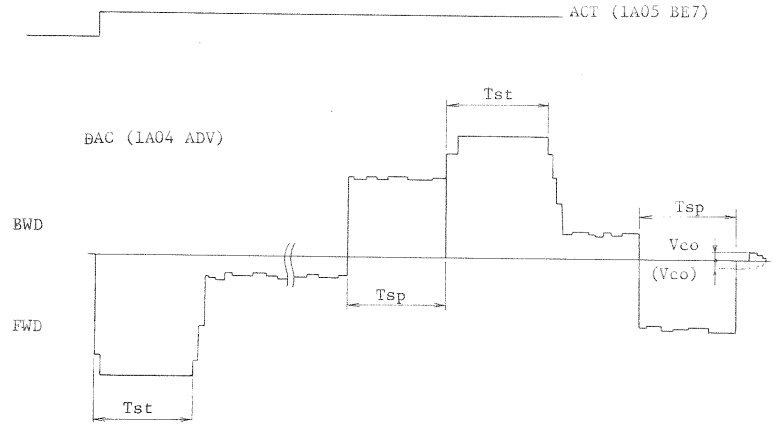


Fig. 3 DAC output (Forward Start/Stop)

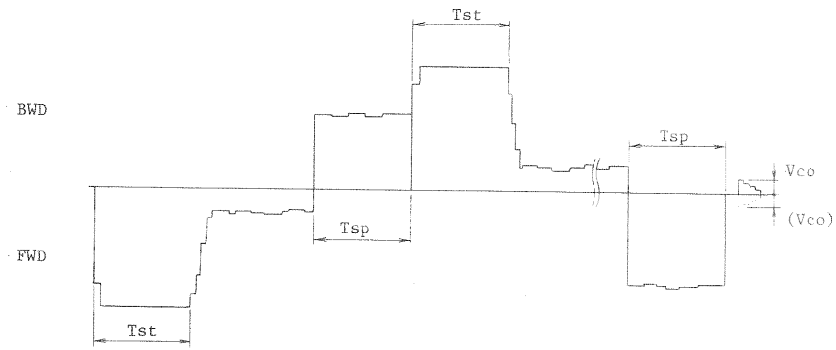


Fig. 4 DAC output (Backward Start/Stop)

L0140	Replacement of Threading Chute and Restraint Member

Procedure:

[Removing]

Remove three threading chute mounting screws and four restraint member mounting screws.

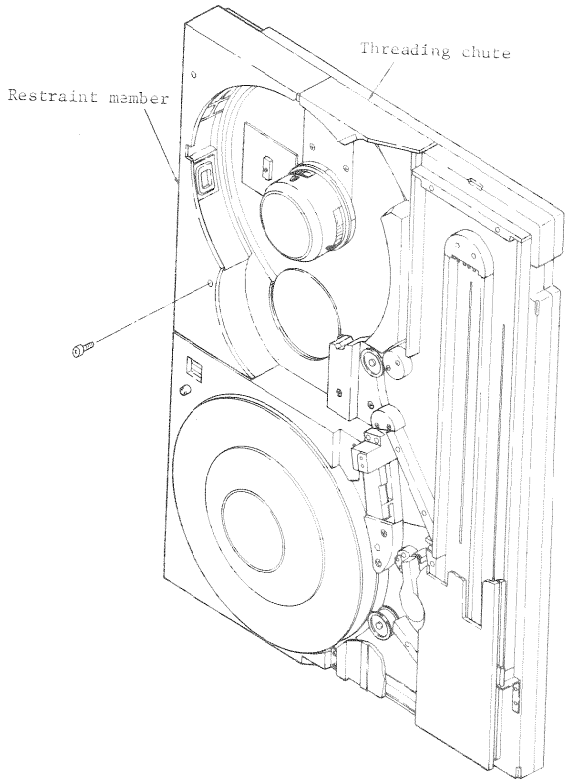
[Mounting]

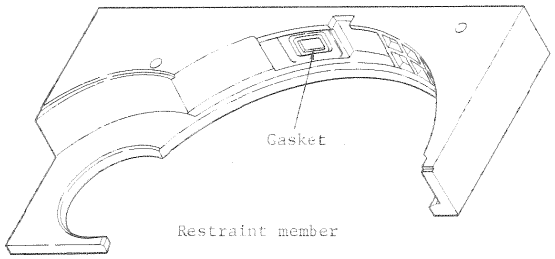
Mount the separated threading chute and restraint member onto their positioning pins.

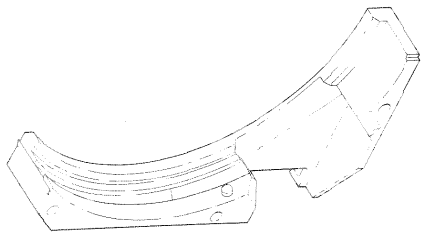
Checkout:

Press the gasket of the restraint-member with a finger, release it, and confirm that gasket is restored to the original shape.

Fig. 1







L0150	Replacement of Cartridge Opener

Procedure:

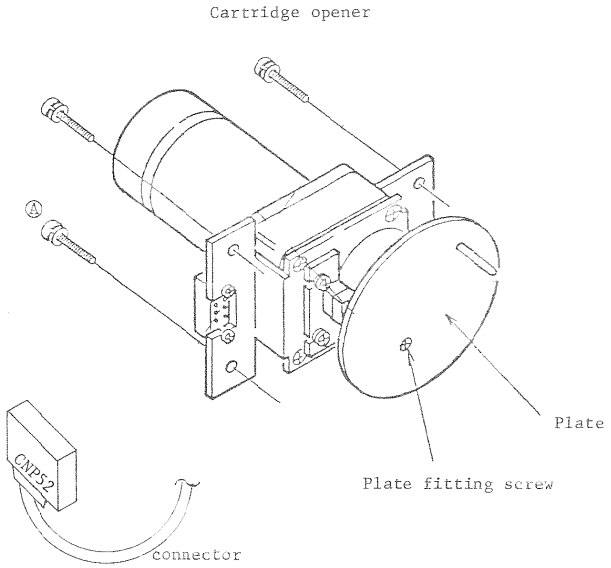
[Removing]

1. Remove the plate fitting screw, and remove the plate.
2. Open the rear plate and detach the connector [CNP52].
3. Remove the three screws Ⓐ , and remove the cartridge opener.

[Mounting]

1. Secure the cartridge opener on the casting panel with three screws Ⓐ .
2. Insert the connector [CNP52].
3. Fit the plate with the plate fitting screw.

Fig. 1



L0160	Replacement of Error Marker

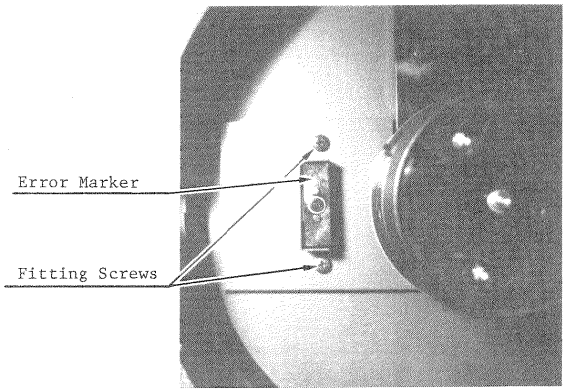
Removal:

Open the rear door, detach the connector CNP53 above the file reel motor, remove the two error marker fitting screws, and remove the error marker.

Mounting:

Carry out the above procedures in the reverse sequence.

Fig. 1



L0170	Replacement of File Protection and Microswitch

Removal the file protection:

1. Remove the two fitting screws that are securing the file protection on the panel. (Fig. 1)
2. Pull out the whole file protection, and remove the air tube and microswitch. (Fig. 2)
3. Disconnect the microswitch lead wires.

Mounting of the file protection:

1. Remove the fitting metal assembly with microswitch from the file protection.
   Note: Do not detach the microswitch from the fitting metal.
2. Connect the lead wires to the microswitch.
3. Screw the fitting metal assembly with microswitch onto the file protection.
4. Insert the air tube.
5. Screw the file protection to the panel.

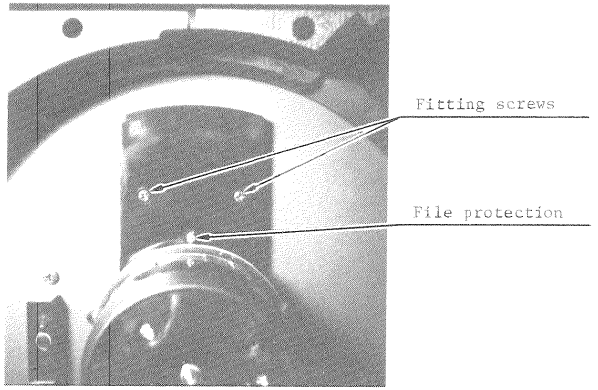
Removal of the microswitch:

Carry out the same procedure as above "Removal of the file protection".

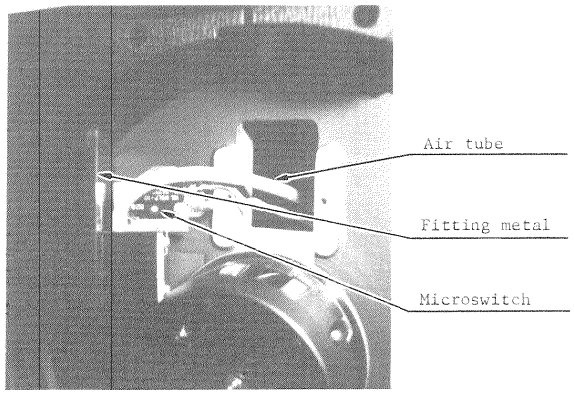
Mounting of the microswitch:

1. Connect the lead wires to the microswitch.
2. Mount the microswitch on the file protection, inserting vanish glass cloth into between the microswitch and metal fitting.
3. Insert the air tube.
4. Screw the file protection to the panel.
5. Check and adjustment
   Check and adjust the file protection mechanism (refer to K0260).

(Fig. 1)



(Fig. 2)



L0180	Replacement of Auto-hub and Reel Boss

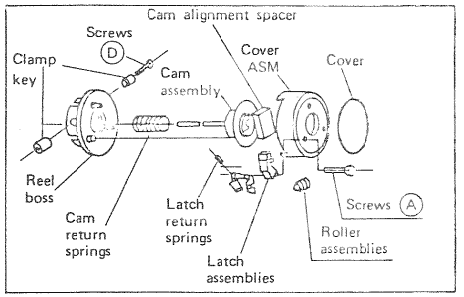
Removal:

1. Peel off the cover.
2. Insert the cam alignment spacer (B960-011C-X085A, thickness 6.5mm) between th cover assembly and the cam.
3. Loosen the screws Ⓑ , and remove the rear cover.
4. Loosen the screw Ⓒ , and remove the clamping.
5. Remove the rear housing assembly.
6. Remove the bushing.
7. Loosen the three screws Ⓐ , and remove the cover assembly. When removing these screws, be sure to keep the cover assembly pressed lest it should jump out by the force of the cam return spring.
8. Pull out the cam assembly and cam return spring.
9. Pull our the latch assemblies together with the latch return spring and roller assemblies, from the pins. (Refer to L0200 Latch assembly)
10. Loosen the screw Ⓓ , and remove the reel boss from the motor shaft.

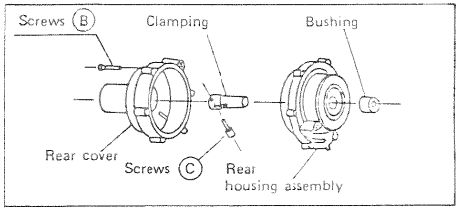
Mounting:

1. Mount the reel boss to the reel motor shaft using a clamp key, and adjust the reel boss position as shown in Fig. 3.
2. Mount the roller assemblies and latch assemblies to the reel boss pins and then mount latch return spring. (Refer to L0200 Latch assembly).
3. Mount the cam assembly and cam return spring so that the three notches of the cam assembly are aligned with the pin positions.
4. While pressing the cover assembly with hand, screw the three cup fitting screws Ⓐ into the reel boss pin.
5. Insert the cam alignment spacer between the cover assembly and the cam.
6. Put the bushing on the reel motor shaft.
7. Mount the rear housing assembly so that the bushing is inserted into the bearing of the rear housing assembly. At this time, the housing assembly should be oriented so that the stopper screw on the rear side of the file reel (see Fig. 2 in L0220) may be inserted into the screw hole on the housing.
8. Insert the clamping into the rear housing assembly, and push the clamping so as to hit the bushing. Then, fasten the screw Ⓒ .
9. Place the rear cover, and secure it with the screws Ⓑ .
10. Take out the cam alignment spacer.
11. Stick a new cover.

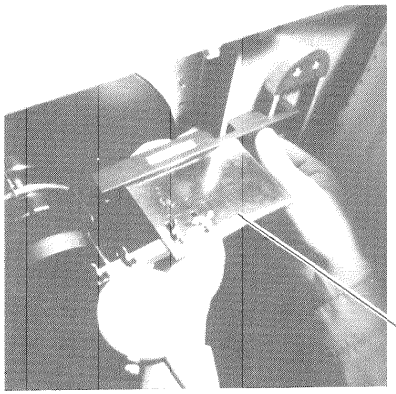
(Fig. 1)



(Fig. 2)



(Fig. 3)



Adjusting method

1. Remove the threading chute.
2. Set the short pointer of dial gauge 4mm to 6mm and adjust the long hand of dial gauge 0.79mm on the main column surface.
3. Fit the adjustment tool on the column surface.
4. Adjust the reel boss position so that the distance between the column surface and the rubber ring on the reel boss surface is 2.79±0.05mm, then the long pointer of dial gauge indicates 0±0.05mm.

Adjustment Tool
(B960-0110-T015A) or (B960-0110-T030A)

Note: B960-0110-T015A; for checking
B960-0110-T030A; for adjusting

L0190	Replacement of Cover Assembly

Removal:

Peel off the cover, and remove the screws (A). (Fig. 1)

Mounting:

1. While pressing the cover assembly, screw the three screws (A) into the reel boss pin.
2. Stick a new cover.

L0200	Replacement of Latch Assembly

Removal of the latch assembly:

1. Peel off the cover, loosen the screws (A), and remove the cover assembly. (Fig. 1)
2. From the reel boss pin, remove the latch assembly together with the latch return spring and roller assemblies.
   Take sufficient care not to lose the latch return springs. (Fig. 2)

Mounting of the latch assemblies:

1. Mount the latches and roller assemblies and then mount latch return springs. (Fig. 2)
2. Mount the cover assembly (Refer to L0190).
3. Stick a new cover.

L0210-1	Cam Assembly Exchange (1)

Removal of cam assembly:

1. Peel off the cover.
2. Insert the cam alignment spacer between the cover assembly and the cam. Fig. 1, page L0210-2
3. Loosen the screws (A), and remove the rear cover.
4. Remove the screw (B), and remove the clamping.
5. While pressing the cover assembly, loosen the screws (C), remove the cover assembly, and pull out the cam assembly. Fig. 2, page L0210-2

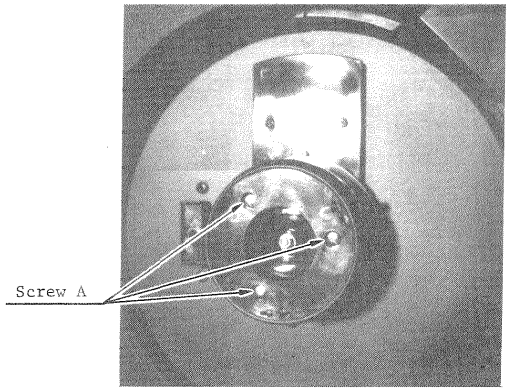


Fig. 1 (Cover is removed)

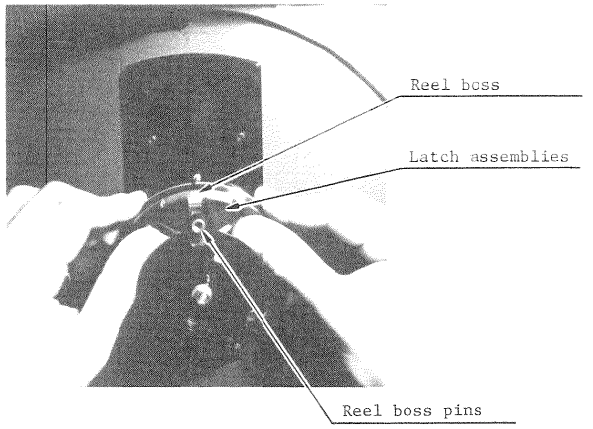


Fig. 2 (Cam assembly is removed)

L0210-2	Cam Assembly Exchange (2)

Mounting of the cam assembly:

1. Set the cam return spring on the cam assembly, and insert the cam shaft through the bushing and clamping (Fig. 1, Fig. 2).
2. Align the three bosses of the cover assembly with the notches of the cam and the reel boss pins, and while pressing the cover assembly, fasten the screws (C).
3. Insert the cam alignment spacer between the cover assembly and the cam.
4. Push the clamping till the clamping hits the bushing, secure the clamping by fastening the screw (B).
5. Place the rear cover, and secure it with the screws (A).
6. Remove the cam alignment spajer between the cover assembly and the cam.
7. Stick a new cover.

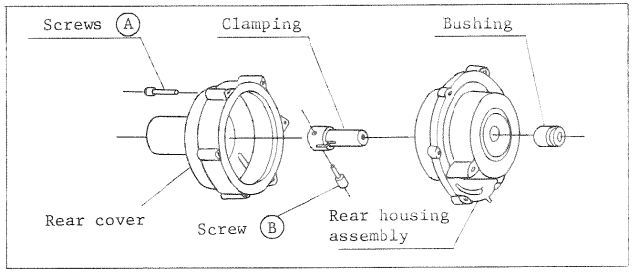


Fig. 1

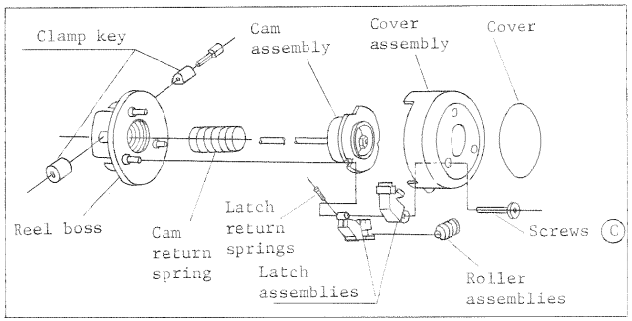


Fig. 2

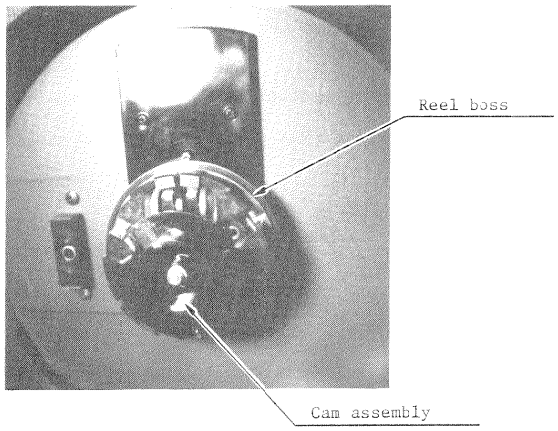


Fig. 3

LO220	Replacement of Rear Housing Assembly

Removal (Fig. 1)

1. Peel off the cover.
2. Insert the cam alignment spacer between the cover assembly and the cam.
3. Loosen the screws (A), and remove the rear cover.
4. Loosen the screw (B), and remove the clamping.
5. Remove the rear housing assembly.
6. Remove the bushing.

Mounting (Fig. 1, Fig. 2)

1. Put the bushing on the reel motor shaft. (Fig. 1, Fig. 2)
2. Mount the rear housing assembly so that bushing is inserted into the bearing of the housing.

   Note: At this time, the housing should be oriented so that the stopper screw on the right of the reel motor may be inserted into the hole on the rear housing.
3. Insert the clamping into the rear bearing.
4. Push the clamping till clamping hits the bushing and then secure the clamping by fastening the screw (B).
5. Place the rear cover, and secure it with the screws (A).
6. Stick a new cover.

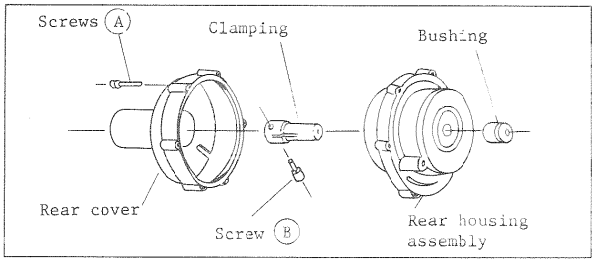


Fig. 1

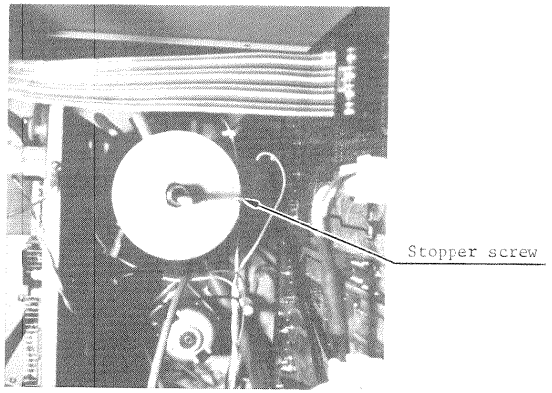


Fig. 2

L0230	Replacement of Machine Reel

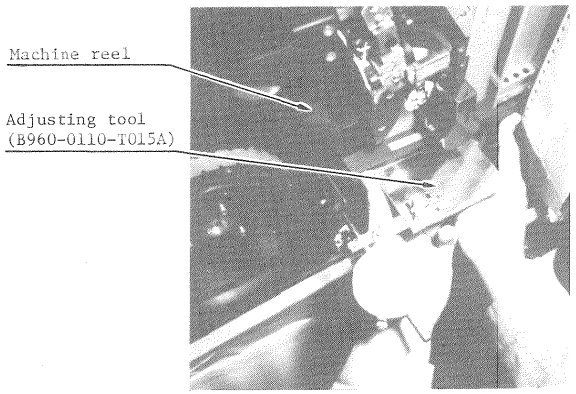
Removal (see Fig. 1):

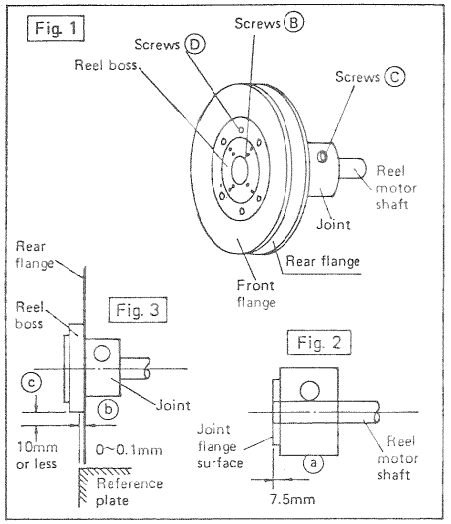
1. Remove the three screws (B) , and remove the machine reel.
2. Loosen the screws (C) , and remove the joint from the reel motor shaft.

Mounting:

1. Measure the distance between the joint flange surface and the tap of the reel motor shaft ((a) in Fig. 2) with calipers. Adjust the distance to 7.5mm, and tentatively secure the joint with the screws (C) .
2. Secure themmachine reel with the screws (B) . Remove the screws (D) and remove front flange.
3. At (c) in Fig. 3, adjust the distance between the rear flange and the reference plate (subcolumn) ((b) in Fig. 3) to from 0 to 0.1mm using the adjusting tool (B960-0110-TC10A) shown in Fig. 4.
4. Finally secure the joint.
5. Mount the front flange.
6. Attachethe cover, and stick a new cover.

(Fig. 4)





Adjusting method:

1. After steps 1 and 2 of "mounting", remove the left threading channel.
2. Carry out zero adjustment of the adjusting tool on the main column surface. (Short pointer of dial gauge must indicate 4mm or 5mm).
3. Fit the adjusting tool on the reference plate, and hold it so that the dial gauge pin comes into contact with the rear flange at (c) in Fig. 3.
4. While manually rotating the machine reel, check whether the dial gauge reading including fluctuation is within the specified range.
5. Slightly pull out the whole assembled part prior to the adjustment, and adjust the distance (b) into the specified range by gradually pushing in the whole assembled part while measuring the distance.

L0250	Replacement of Low Tape Sensor

Procedure:

[Removing]

1. Remove three reel boss setscrews, and remove front disk plate, reel boss, and rear disk plate.
2. Remove two low tape sensor mounting screws and the low tape sensor.
3. Disconnect connector [CNJ56].

[Mounting]

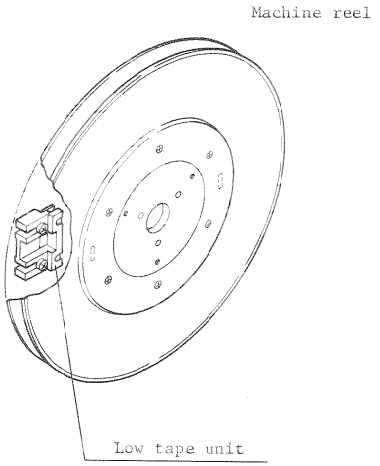
Perform the reverse procedure given above.

Note: When mounting the low tape sensor, hold down the sensor onto the casting base.

Checkout:

Check the low tape detector level (see K0220)

Fig. 1



L0260	Replacement of Machine Reel Motor, File Reel Motor

Removal of file reel motor:

1. Remove the error marker. (Refer to L0160.)
2. Remove rear cover, clamping, rear housing assembly and bushing according to steps 1 to 6 of L0180.
3. Loosen the reel boss securing screw and pull out the auto-hub. (Refer to step 10 of Removal of L0180.)
4. Detach the connector CNP87 from the connector CNJ86 of the tape drive circuit (TVBMU at the middle portion of the right side).
5. Remove the four screws (A), and remove the motor.

Mounting of the file reel motor

1. Remove the air inlet pipe from the edge on the motor flange. (200 ips MTU only)
2. Mount the reel motor so that the lead wires and stopper screw may be oriented as shown in Fig. 1 when looked at from the reel motor rear side.
3. Fasten the four screws (A), and attach the connector CNP86.
4. Mount the auto-hub by following the step 1 of Mounting of L0180.
5. Mount bushing, rear housing assembly, clamping, rear cover, and cover according to steps 6 to 11 of Mounting of L0180.

Removal of the machine reel motor

1. Remove the machine reel. (Refer to L0230.)
2. Detach the connector CNP88 from the tape drive circuit (TVBMU at the middle portion of the right side).
3. Remove the four screws (B), and remove the motor.

Mounting the machine reel motor:

1. Mount the reel motor with its lead wires going out from its top, and faster the four screws (B).
2. Mount the connector CNP88 to TVBMU.
3. Mount the machine reel. (Refer to L0230.)

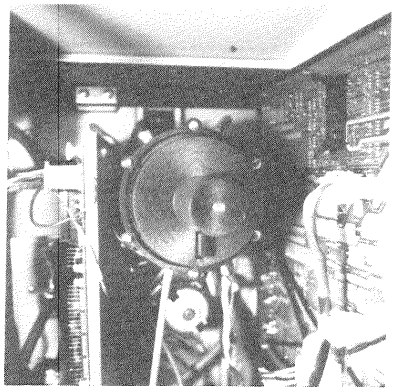


Fig. 1 (File reel motor)

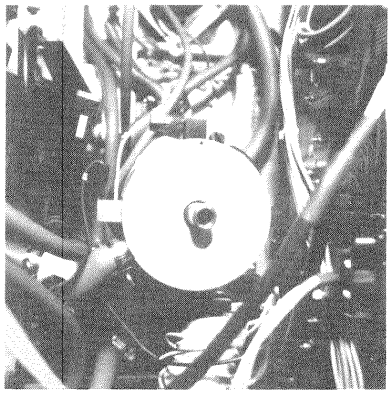


Fig. 2 (Machine reel motor)

L0270	Replacement of Column Cover

Procedure:

[Removing Glass Plate]

1. Open the column cover and remove five glass plate (setscrews).
2. Remove the spring which holds the glass plate.

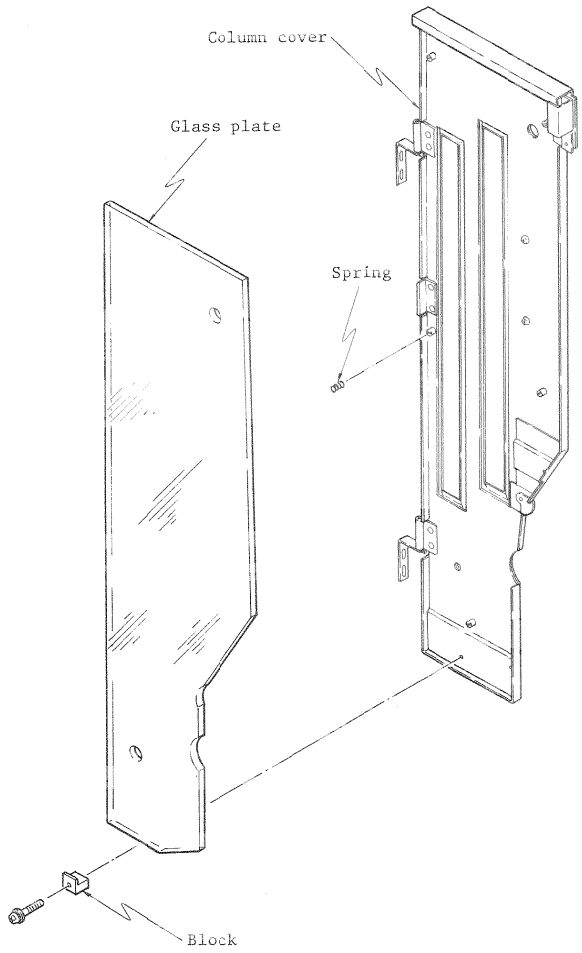
[Mounting Glass Plate]

Place the spring between the column cover and glass plate, and tighten five glass plate mounting screws using screw blocks.

Checkout:

Press the glass plate by your hand and (cheak) it moves smoothly and returns to its position.

Fig. 1



L0280	Replacement of Vacuum Column Section

Replacement of Roller Catch

Removal:

Remove two Roller Catch's, which are fitted at the top and bottom left side of the column, by detaching the fitting bolts.

Mounting:

Mount Roller Chath's with fitting bolts.

Check and adjustment

When the cover is closed, check that the roller catch is firmly installed and that there is no gap between the column rib and the glass. If they are not satisfied, adjust them by the oval whole on the roller catch.

Fig. 1

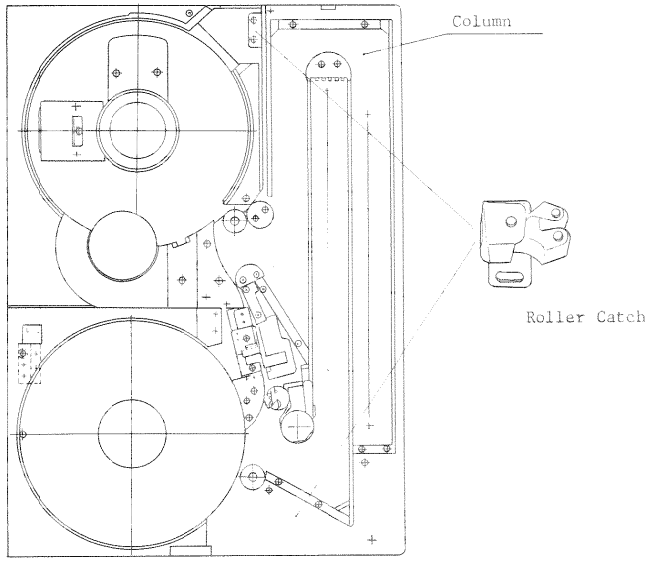


Fig. 1

L0300-1	Replacement of Micro Switch for Opening/Closing Slider

Removal:

1. Remove the cover of the front door.
2. Remove the micro switch to be replaced.
   Detach the lead from the terminal.

Mounting:

Mount to micro switch by soldering its terminal and the lead at the proper position.

Check and adjustment

1. In the detecting status of the micro switch (Fig. 3), adjust the gap between the micro switch and the actuater to be from 0.33 mm to 0.55 mm by loosening two bolts of the fitting board.

   Note: Before putting the micro switch in the detecting status, loosen the bolts of the fitting board to prevent the actuater part from being bent.

2. When the power supply is turned on and the door slider is opened and closed, check that the top of the slider touches the sponge surface and that it is 0 ∿ 2 mm above the bottom. (Fig. 2)
   If they are not satisfied, do the adjustment given above.

Note: When the micro switch is being adjusted, the power supply must be turned off.

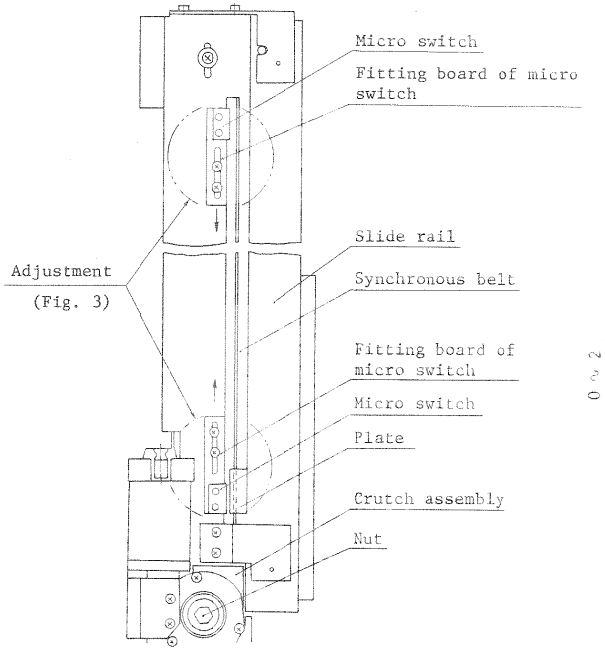


Fig. 1

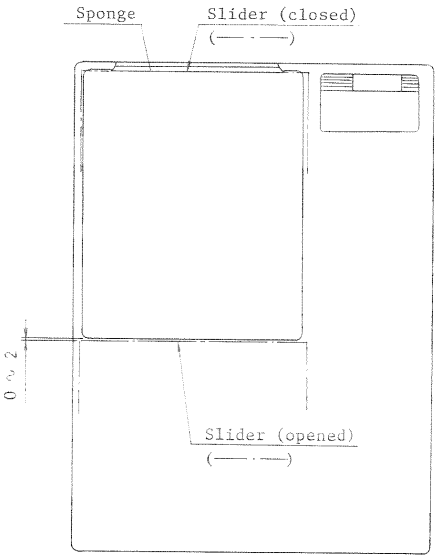
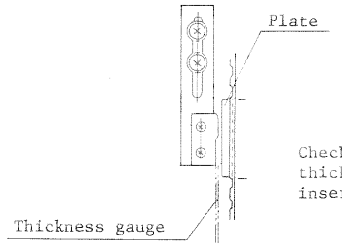


Figure observed in front of the unit

Fig. 2



Check under the status shown that a thickness gauge of 0.33 mm can be inserted but 0.55 mm.

Fig. 3

LO300-2	Replacement of Front Door Auto Window

Procedure:

[Removing]

1. Open the front door, and remove six cover setscrews and covers.
2. Remove three slider setscrews.
3. Disconnect connector[CNP57].
4. Remove three auto window setscrews and loosen one screw of it. Then slide to the left and remove the auto window.

[Mounting]

1. Mount the auto window onto the loosen screw and tighten the remaining four screws.
2. Mount the slider and tighten three screws, and then connect connector [CNP57].
3. Mount covers and tighten six screws.

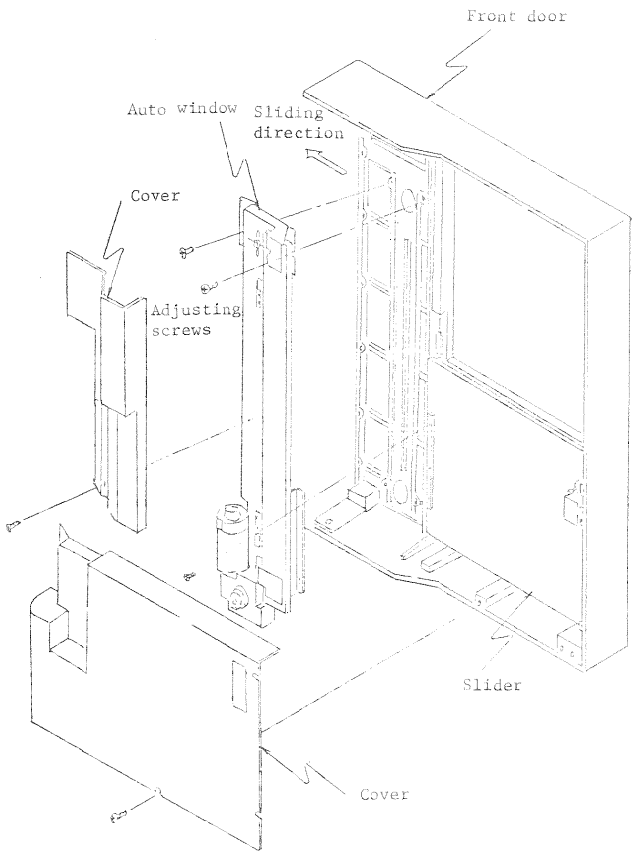
CAUTION:

When mounting covers, do not place wires and cables between the cover and door.

Checkout:

After assembling, check to be sure that the window operates correctly.

Fig. 1



L0310-1	Replacement of Front Door Clutch Section (1)

Procedure:

[Removing]

1. Loosen hex socket screw of moving pulley to decrease belt tension.
2. Remove the belt from the fixed pulley, then loosen hex socket screw and remove the fixed pulley.
3. Remove four microswitch setscrews.

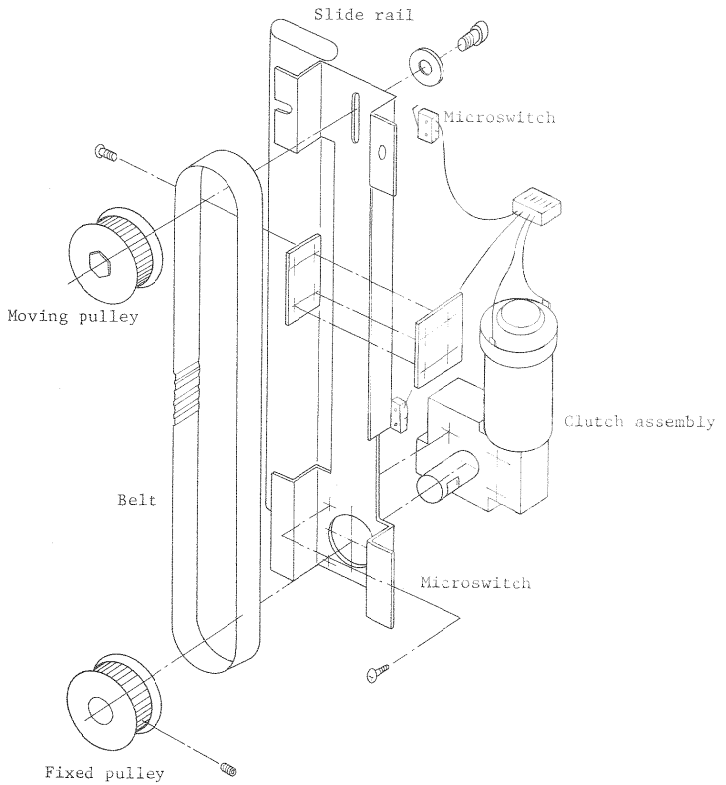
   Caution: Never remove or loosen any screws on the base plate, as they have been adjusted for proper positioning.
4. Remove cable clamping screws.
5. Remove four clutch ASM setscrews and the clutch section.
6. When replacing the belt, remove four screws from the slide rail mounting plate and mounting plate. Then remove the belt.

[Mounting]

Mount in sequence the clutch ASM, microswitch, fixed pulley, belt, and moving pulley.

Note: Mount the belt so that the belt is horizontal when it is held by pulleys.

Fig. 1



L0310-2	Replacement of Front Door Clutch Section (2)

Checkout:

1. Check that the belt tension is 0.11 ~ 0.17 kg with deflection of 7.8 mm at position 242 mm away from the center of pulley.
2. Check that the mounting plate contacts in parallel to the microswitch.

REPLACING SLIDE RAIL

How To Replace Slide Rail:

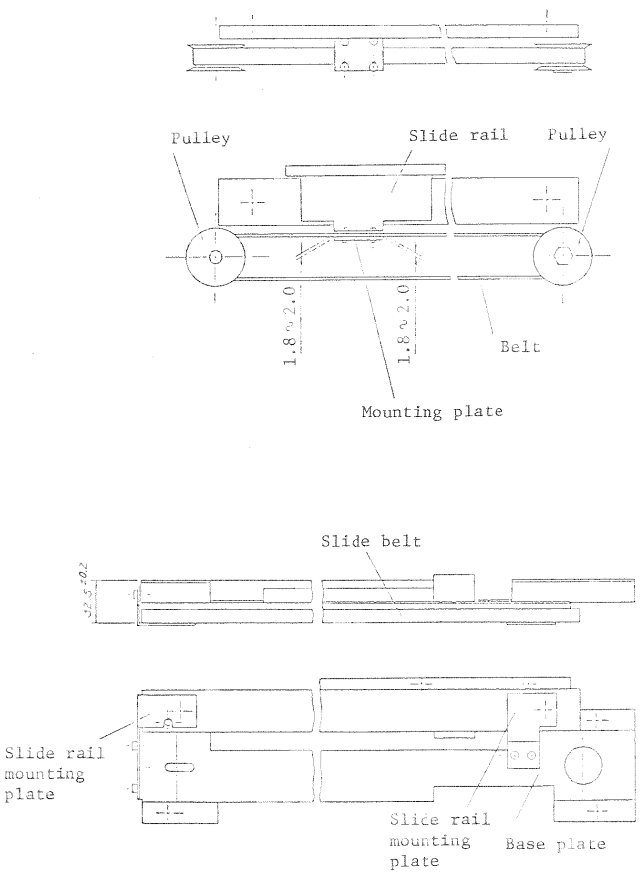
[Removing]

Remove two slide rail setscrews (flat-head screws) and the slide rail.

[Mounting]

Mount the slide rail in position and tighten two screws.

Fig. 1



L0330	Replacement of Valve ASM Vacuum and Pressure

Procedure:

[Removing]

1. Disconnect hoses, tubes and connector [CNP66] from the rear of Valve ASM Vacuum and Pressure.
2. Remove Valve ASM Vacuum and Pressure setscrews (six screws of Valve ASM Vacuum and four of Valve ASM Pressure and the Valve ASM Vacuum and Pressure.

[Mounting]

1. Mount the Valve ASM Vacuum and Pressure (first, mount the Valve ASM Vacuum and then mount Valve ASM Pressure according to the center shaft).
2. Connect hoses, tubes and connector [CN66].

Checkout:

Check for the correct air pressure and adjust it if needed. Refer to Manual Sheet K0190 for adjustment procedure.

NEW TYPE

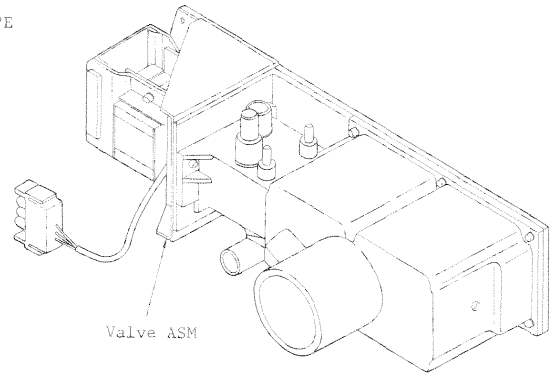
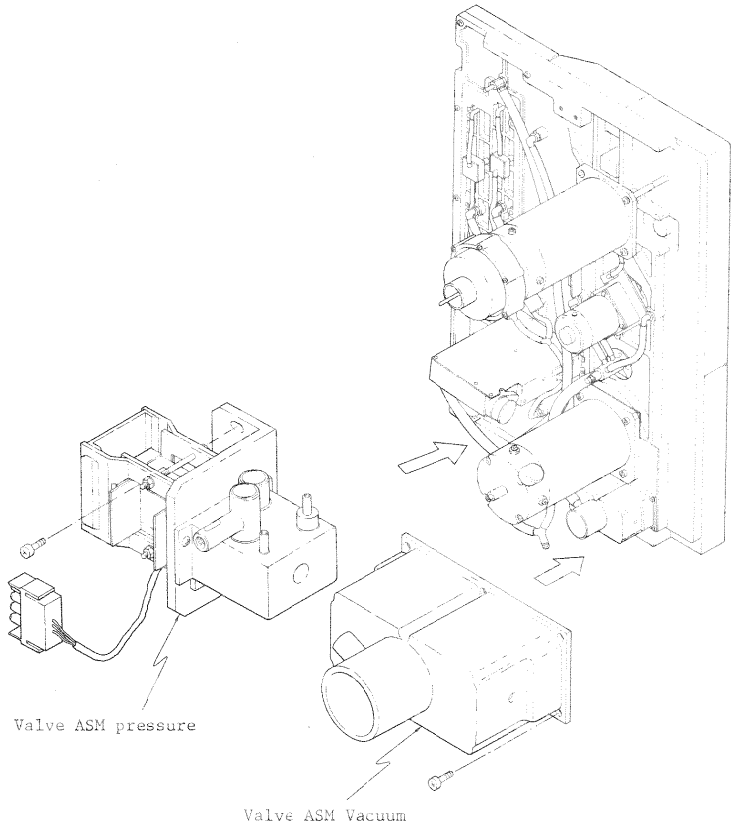


Fig.



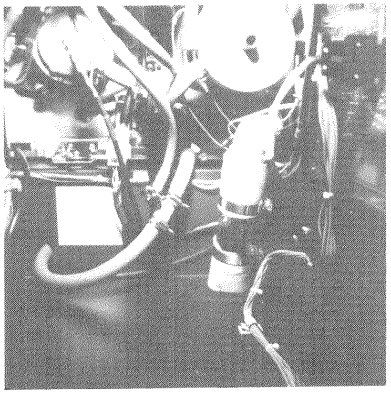
L0350	Replacement of Restrictor

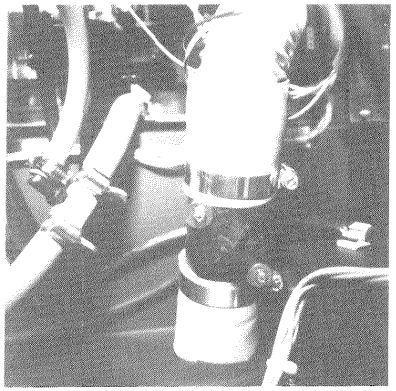
Removal and mounting:

Loosen the hose bands at the both ends of the restrictor, and remove the restrictor. When attaching the restrictor, connect the hoses to the both ends, and fasten them with the hose bands.

Check and adjustment:

Check and adjust the pressure and vacuum level .... K0190 (Pressure and Vacuum level check and adjustment during tape loading)





Restrictor

L0360-1	Replacement of Fans (1)

Procedure:

(1) MTC and MTU gate fans

[Removing]

1. Open the MTC front door and disconnect connectors from the fan.
2. Remove four fan mounting screws and take out the fan with finger guard.

[Mounting]

1. Mount the finger guard and fan onto the frame shelf and tighten four screws.
2. Connect all connectors.

(2) Air supply cooling fan

[Removing]

1. Open the Front panel and internal doors by removing two screws, and then disconnect connector [CNJ42].
2. Remove the filter and then remove four screws to remove the fan.

[Mounting]

1. Mount the fan in the frame and tighten four screws. Then mount the filter.
2. Connect connector [CNJ42], close and fix the internal door by two screws, and close front door.

Fig. 1

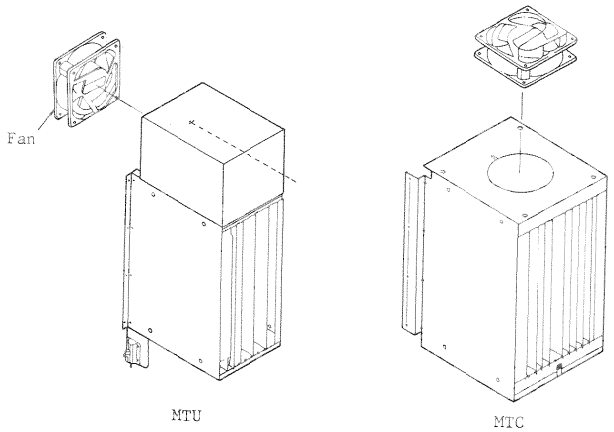
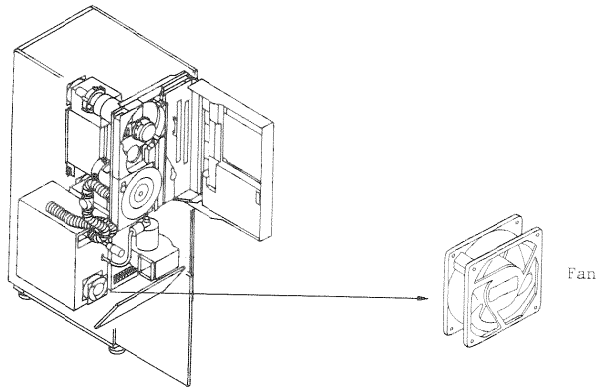


Fig. 2



L0360-2	Replacement of Fans (2)

(3) Fan on rear door

[Removing]

1. Disconnect connector [CNP46].
2. Loosen six nuts and remove the duct from the rear door.
3. Remove two setscrews and remove the fan from duct.

[Mounting]

1. Mount the fan onto duct and tighten two screws.
2. Mount the duct onto rear door and tighten six duct (setscrews).
3. Connect connector [CNP46].

(4) Fan unit

[Removing]

1. Open the cabinet front panel, and open internal door by removing two screws.
2. Disconnect connector [CNP43].
3. Remove two fan (setscrews) and fan unit.

[Mounting]

1. Mount fan unit in the frame and tighten two screws.
2. Connect connector [CNP43].
3. Close and tighten internal door by two screws, and close front door.

Fig. 1

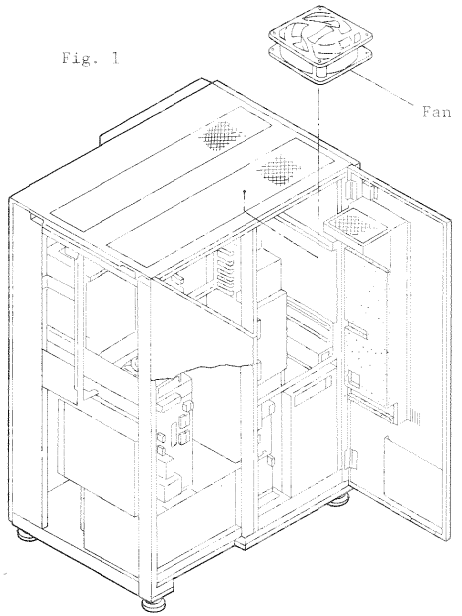
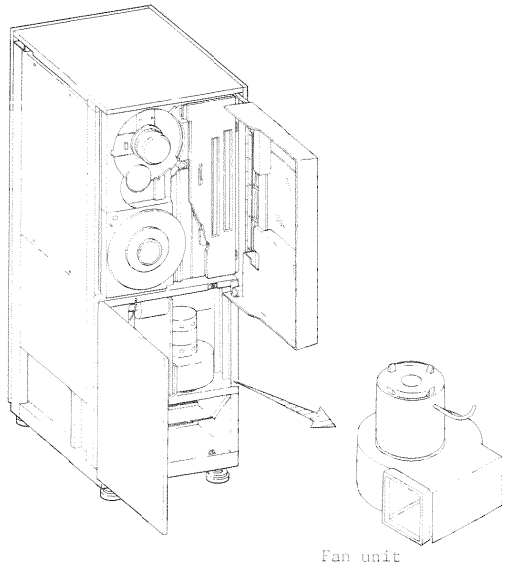


Fig. 2



L0370	Replacement of Cooling Air Filter

Removal:

1. Open the front door and remove the filter.
2. Clean the filter with a cleaner.

Mounting:

1. Set the filter on the guide rail and fit it at the proper position.

Fig. 1

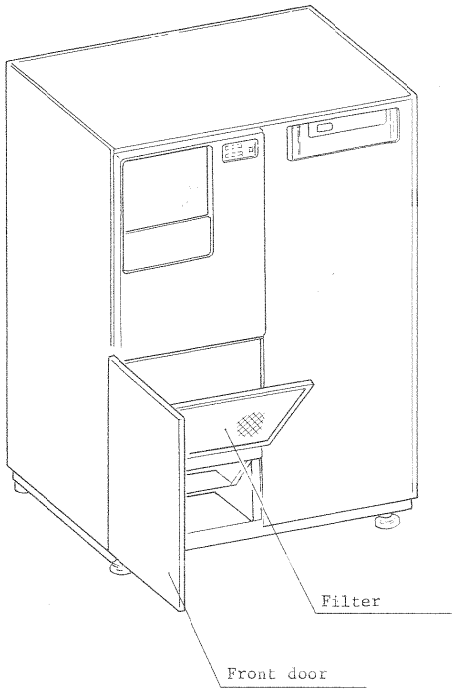


Fig. 1

L0380	Replacement of Absolute Filter

[Renoving]

1. Remove the joint, and remove the tube.
2. Remove the setscrew and remove the absolute filter.

[Mounting]

1. Mount the absolute filter and tighten the setscrew.

   CAUTION: When mounting the absolute filter, turn the hose tap below.

2. Connect the tube and connect the joint.

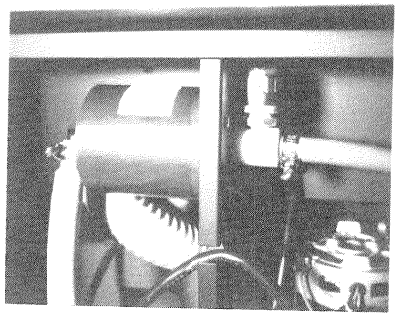


Fig. 1

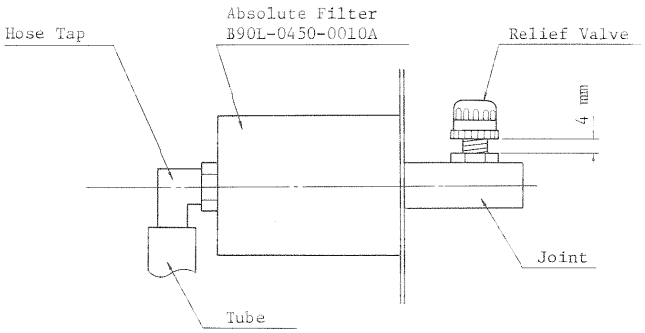


Fig. 2

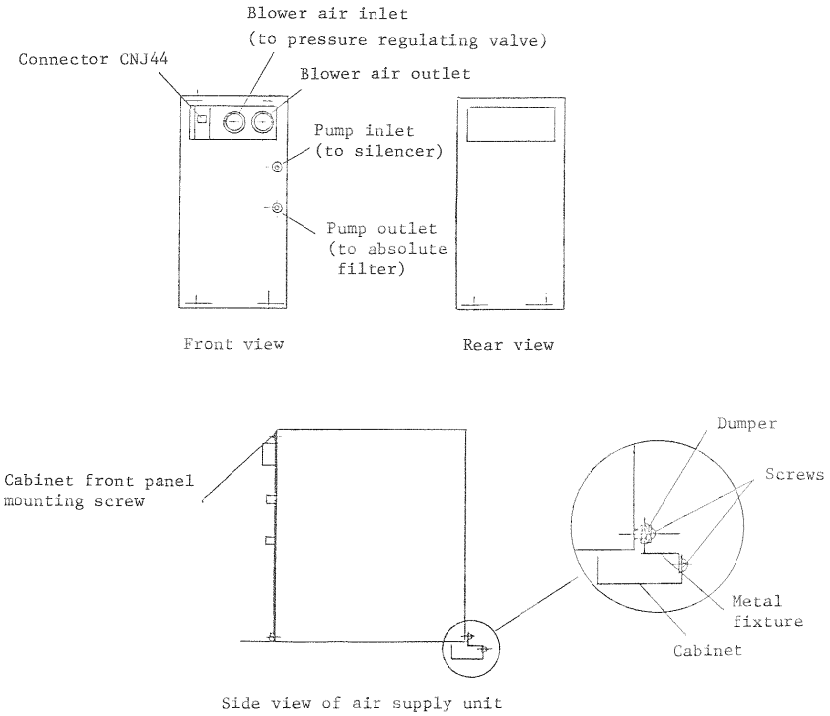
L0400-1	Replacement of Air Supply Unit (1)

Procedure:

[Removing]

1. Remove the hose band of vacuum regulating valve.
2. Pull the hose from the blower exhaust duct.
3. Loosen the tube band and disconnect the pump tube coming from the absolute filter.
4. Disconnect the silencer tube.
5. Open the rear door and remove two screws to remove air-supply mounting metal fittings. Remove two metal fittings mounting screws from the air supply, and then remove metal fittings including dumper rubber.
6. Disconnect power connector [CNP44] of air supply.
7. Remove four air supply mounting screws located at the front of frame, and take out the air supply from the rear of frame.
8. Remove both the hose bands of blower inlet and outlet, then disconnect two hoses.

Fig. 1

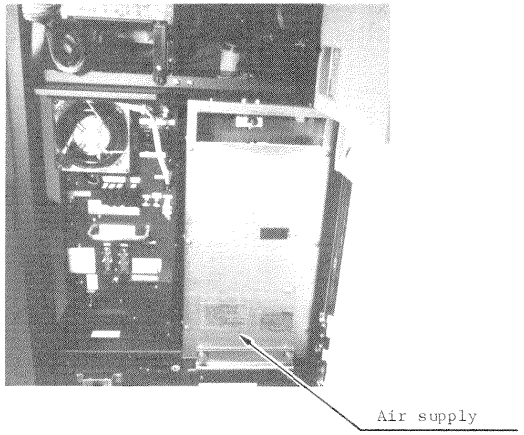


L0400-2	Replacement of Air Supply Unit (2)

[Mounting]

1. Connect two hoses to the blower and tighten the hose band.
2. Mount the air supply on the cabinet and tighten two cabinet front panel mounting screws.
3. Mount and tighten the metal fittings and rubber dumper at the rear of cabinet.
4. Connect connector [CNP44].
5. Connect silencer tube to the pump inlet.
6. Connect the tube (coming from absolute filter) to the pump outlet.
7. Place the hose of blower air outlet in the frame exhaust duct.
8. Connect the hose of blower inlet to the pressure regulating valve.
9. Follow the instructions of pressure regulation given on Manual Sheet K0190.

Fig. 2



L0400-3	Replacement of Air Supply Belt

Procedure:

[Removing]

1. Remove air supply unit.
2. Remove screws from the air supply belt cover.
3. Loosen blower/pump (setscrews), and remove the belt.

[Mounting]

1. Set the belt in position and tighten bolts with keeping an appropriate belt tension.
2. Mount air supply belt cover and tighten its screws.
3. Mount air supply unit.

Setting Belt Tension:

Push a spring balancer against the belt at its center and adjust the belt tension to 29 ∿ 34 lbs.

Caution: Do not push or pull the belt beyond the head of pulley.

Fig. 1

Front View

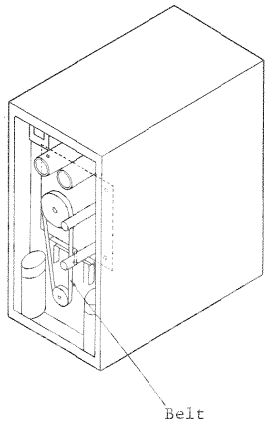
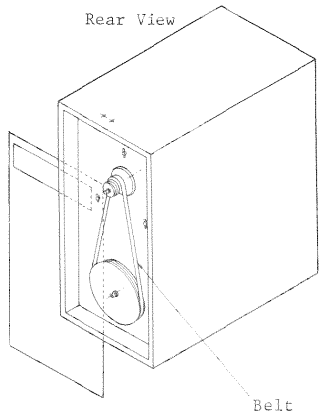


Fig. 2

Rear View



L0410	Replacement Threading Cover

Procedure:

[Removing]

1. Open the column cover and threading cover.
2. Remove two setscrews from the upper hinge, and slightly pull up the threading cover and remove it.

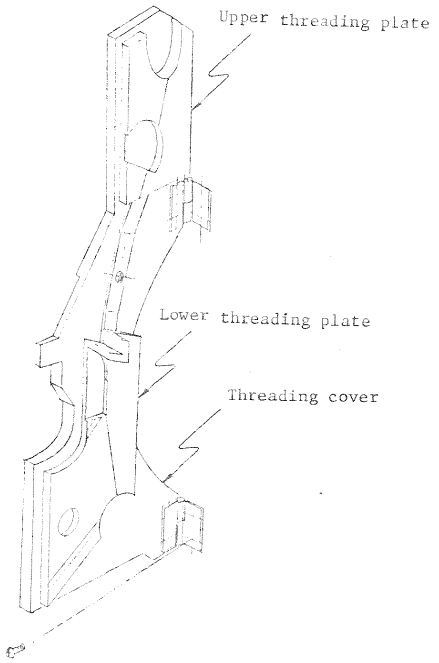
[Mounting]

Place the lower hinge of threading cover in position, and then tighten two setscrews of upper hinge.

Checkout:

Check to be sure that no interference occurs between the column cover and threading cover.

Fig. 1



L0420	Replacement of Cartridge Sensor

Procedure:

[Removing]

1. Open the rear door, and remove two cartridge sensor setscrews and the cartridge sensor.
2. Remove three setscrews of microswitch leads and the leads.

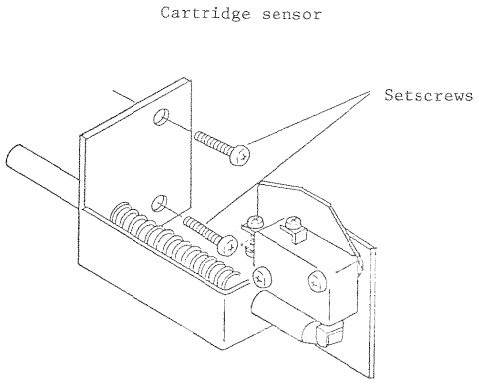
[Mounting]

Perform the reverse procedure given above.

Checkout:

Make sure that the cartridge detector rod can operate smoothly and return by the spring force.

Fig. 1



L0430	Replacement of Capacitive Sensor

Procedure:

Note: Replace the sensor at the rear of systen unit.

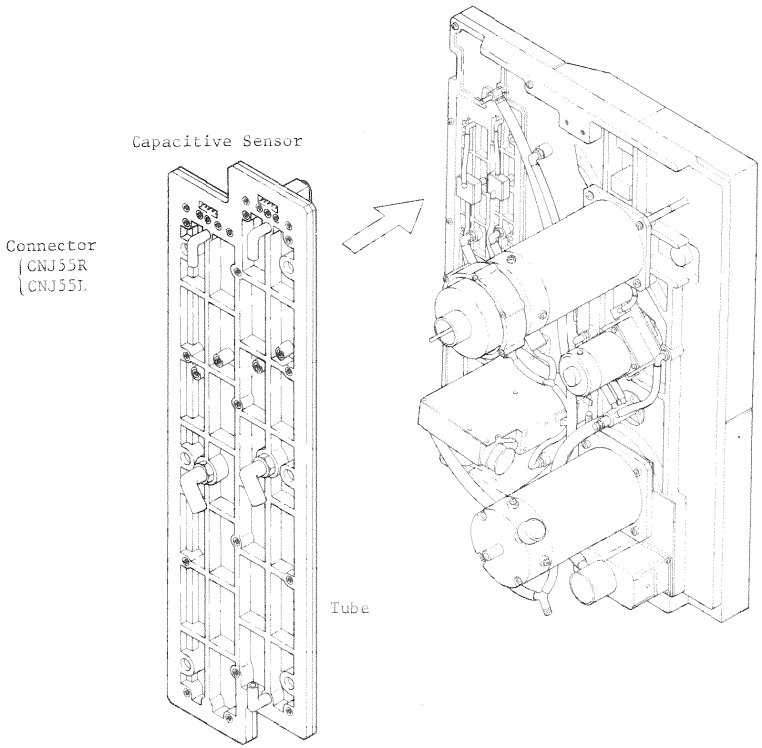
[Removing]

1. Disconnect tube, connectors [CNJ55R and CNJ55L], and terminals SWP1 and SWP2 from the capacitive sensor.
2. Remove six capacitive sensor mounting screws and the capacitive sensor.

[Mounting]

1. Mount the capacitive sensor and tighten six screws.
2. Connect tube, connectors and terminals.

Fig.



L0440	Replacement of Power Supply Unit

Procedure:

[Removing]

1. Disconnect all the connectors and terminals from the power supply.
2. Remove two screws and metal fittings, and take out the power supply.

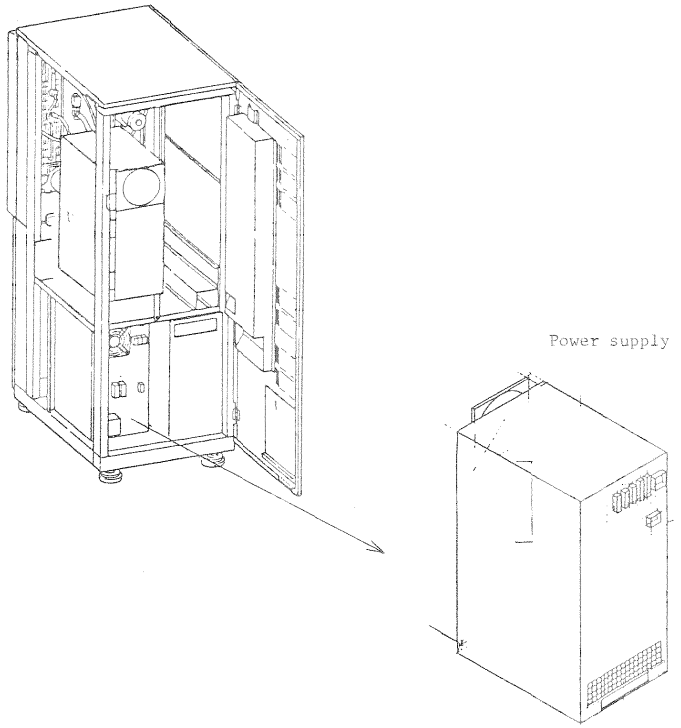
[Mounting]

1. Mount power supply in the frame and tighten two front screws. Then fix the metal fittings onto power supply and fix to the frame.
2. Connect terminals and connectors.

   Caution: In case of 50 Hz connect CNP66 to CNJ66A, and CNP66C to CNJ66B.

   In case of 60 Hz connect CNP66 to CNJ66B. and CNP66C to CNJ66A.

Fig. 1



L0450	Replacement of Operator Panel

Procedure:

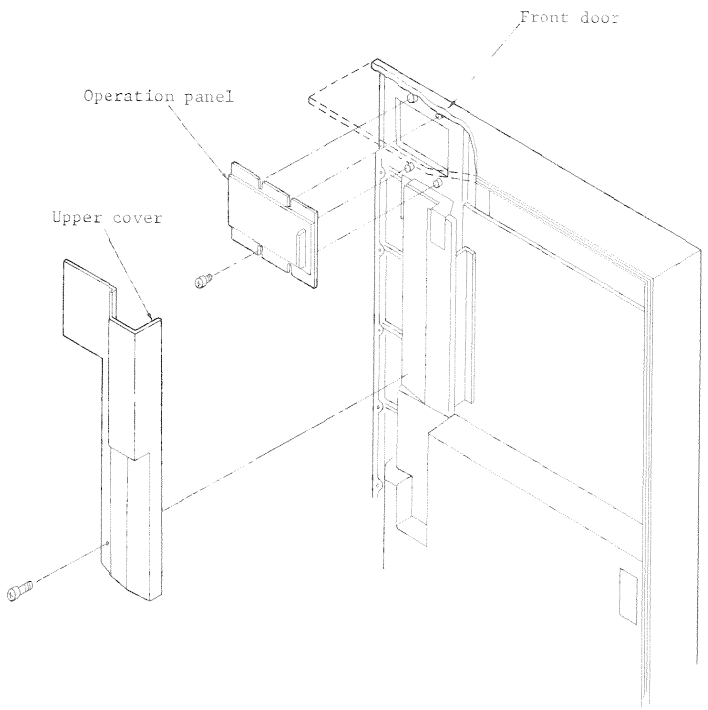
[Removing]

1. Open the front coor, and remove two upper cover setscrews and the upper cover.
2. Disconnect connector [CNJ21].
3. Remove four operation panel (setscrews) and the panel.

[Mounting]

Perform the reverse procedure above.

Fig. 1



L0460	Replacement of Door Switch

Removal:

1. Detach three fitting bolts on the cover.
2. Detach the fasten terminals of door switch.
3. Remove the door switch by depressing it as shown at Fig. 1.

Mounting:

1. Attach the fasten terminals with the door switch.
2. Mount the door switch at the box window of the cover.
3. Fasten the cover with three fitting bolts.

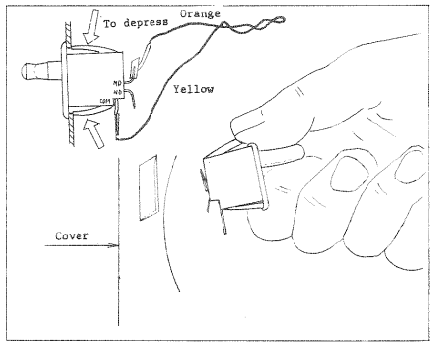


Fig. 1

L0470	Replacement of Rib

Procedure:

[Removing]

1. Remove rib mounting bolts and remove the rib from system panel.
2. Remove screws and metal fittings/flange.

[Mounting]

1. Mount the metal fittings/flange onto rib.
   Note: The metal fitting should not extrude from rib.
2. Mount the rib onto system panel using its bolts.

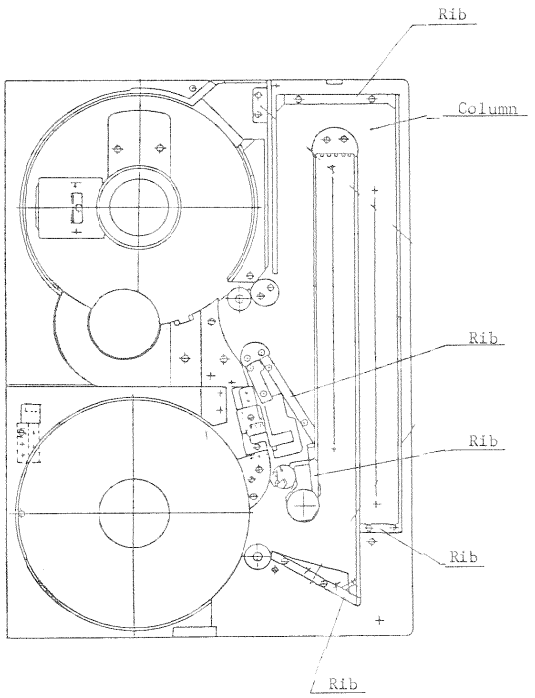


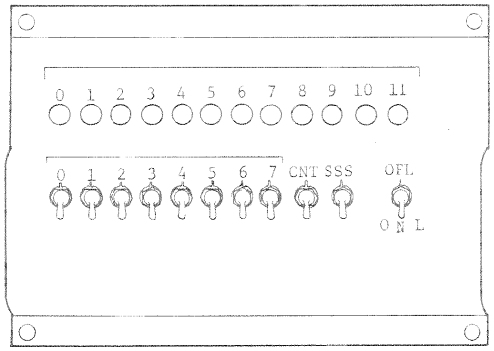
Fig. 1

M0000	Field Tester Operation

MTU field tester operation

M0001	View of Field Tester

Field Tester of MTC



M0002	Field Tester Functions - 1

1. The switch and lamp arrangenent of the field tester is shown on M0001, and their various functions are explained below.

   1. OFL/ONL (two-position toggle switch)

      OFL

      ONL

      This switch is used to change the MTC between the online and offline states. When it is switched, the MTC executes System Reset.

   2. S0-S7 (two-position toggle switch)

      0 1 2 3 4 5 6 7

      These switches are used to set the register address, command, byte count or start/stop address to be displayed and provide control information such as a command/microprogram control.

   3. CNT (two-position momentary toggle switch)

      CNT

      This nonlock-type switch is used to set the various control modes of the Field Tester. This is alsc used to display the contents of the internal register.

   4. SSS (two-position momentary toggle switch)

      SSS

      This nonlock-type switch is used to set the data necessary to control the internal register, to start a command excution, and to step the microprogram for various control functions provided on the Field Tester.

   5. L0-L11 (LAMPS)

      0 1 2 3 4 5 6 7 8 9 10 11

      These lamps are used to display the data of various display functions explained later. They are active when lit.

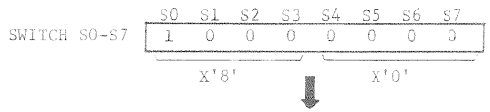
2. Display Functions

This section explains the various display functions equipped in the Field Tester. They are valid in both online and offline states of the MTC.

2.1 Display of Channel Interface Signals and Associated Signals

If switches S0 - S7 are set to X'80'[1], signals shown below are displayed on lamps L0 - L11.

Note 1: X'80' means that 80 in the hexadecimal notation is to be set. Switches are '1' when they are at "ON" (upwards in Fig. 1) and are '0' at "OFF" (downwards in Fig. 1).



SLIG; SELECT-IN-GATE Signal

When this signal is active (L0 lit), it indicates that the controller is selected from the channel.

$\overline{OPI}$; OPERATIONAL-IN Signal

When this signal is active (L1 lit), it indicates that the controller is connected to the channel and is in communication.

DXF$\overline{O}$; DATA-TRANSFER-OUT Signal

This signal indicates the data transfer direction between the channel and controller. When this signal is active (L2 lit), it means data is transferred from the channel to the controller (WRITE OPERATION).

RQIA; REQUEST-IN-A Signal

This signal is active (L3 lit), when the controller requests an interrupt at Channel-A interface side.

RTA; ROUTE-A Signal

This signal is active (L4 lit), when the controller is logically connected to Channel-A interface side.

DXRQ; DATA-TRANSFER-REQUEST Signal

This signal is active (L5 lit), when the controller is ready to transfer data to the channel.

MCY; MACHINE-CYCLE Signal

This signal is active (L6 lit), when the controller is controlling the MTU to execute a command.

B1600; 1600 BPI Signal

This signal is active (L7 lit), when the controller is in the 1600 BPI mode.

ERRF; ERROR FLAG Signal

This lamp informs operators of an error detected by the microprogram when the controller is offline.
This lamp lights when some error is detected during the execution.

ACMP; ADDRESS COMPARE Signal

This signal is active (L9 lit), if a microprogram has passed the address specified by the SAD Register explained later.
This signal can be reset by pressing the SSS switch.

PHLT; PROCESSOR HALT Signal

This signal is active (L10 lit), when the microprocessor is at HALT status.

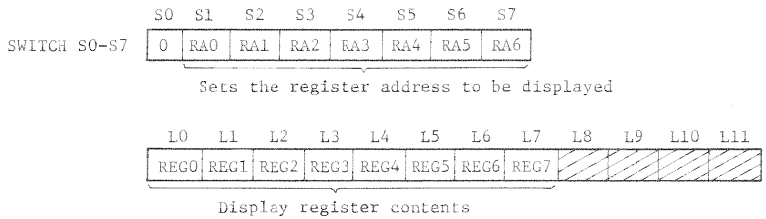
PERR; PROCESSOR ERROR Signal

This signal is active (L11 lit), if some error is detected within the hardware organizing the microprocessor.

2.2 Display of Microprogram Registers (Register display)

If switch 0 is set to '0', the contents of any of the microprogram register whose address is specified by switches S1 - S7 is displayed on lamps L0 - L7. Although the latest register contents is displayed if the microprogram is pausing, the microprograms is interrupted at the following timings and the contents at that moment is displayed while it is running:

- When the CNT switch is $\overline{\text{ON}}$.
- If the microprogram passes the stop address specified by the SAD Register when executing the Address Compare Display operation.



2.3 Display of Stop Address

If switches S0 - S7 are set to X'A1', the contents of the SAD Register is displayed on L0 - L11.

Switch	S0	S1	S2	S3	S4	S5	S6	S7
Setting	1	0	1	0	0	0	0	1
			A				1	

2.4 Display of Branch Address

If switches S0 - S7 are set to X'A2', the contents of the upper 4 bits of the branch address is displayed on L0 - L3.

Register Write Data 0 - 7 is displayed on L4 - L11.

Switch	S0	S1	S2	S3	S4	S5	S6	S7
Setting	1	0	1	0	0	0	1	0
			A				2	

2.5 Display of Microprogram Address

If switches S0 - S7 are set to X'A4', the contents of the microprogram address (CAD 0 - 11) is displayed on L0 - L11.

Switch	S0	S1	S2	S3	S4	S5	S6	S7
Setting	1	0	1	0	0	1	0	0
			A				4	

2.6 Display of Address Compare Control Flag

If switches S0 - S3 are set to X'C', the status of the Address Compare Control Flag is displayed on L4 - L7.

Switch	S0	S1	S2	S3	S4	S5	S6	S7
Setting	1	1	0	0	X	X	X	X
								X: Don't care

Lamp	L0	L1	L2	L3	L4	L5	L6	L7
Indication	1	1	0	0	S.DAC	B.ADC	I.ADC	W.ADC
			C			X		

S.ADC ;
B.ADC ;
I.ADC ;
W.ADC ;

} See 4.5. (M0009)

2.7 Display of Microprogram Control Flag

If switches S0 - S3 are set to X'E', the status of the Microprogram Control flag is displayed on L4 - L7.

Switch	S0	S1	S2	S3	S4	S5	S6	S7
Setting	1	1	1	0	X	X	X	X

Lamp	L0	L1	L2	L3	L4	L5	L6	L7
Indication	1	1	1	0	STEP	ROSF	SINH	SPARE
			E			X		

STEP ;
ROSF ; } See 4.1. (M0008)
SINH ;

2.8 Lamp Test

If switches S0 - S3 are set to X'F', lamps L0 - L11 light.

3. Execution of Offline Command Operation

The Field Tester can let the controller execute channel commands. Operations of the Field Tester for this function are described here. These functions are valid when the controller is in offline mode.

3.1 Write into the Microprogram Register

Using this function, any data can be written into any microprogram register.

(1) Setting the Register Write Mode

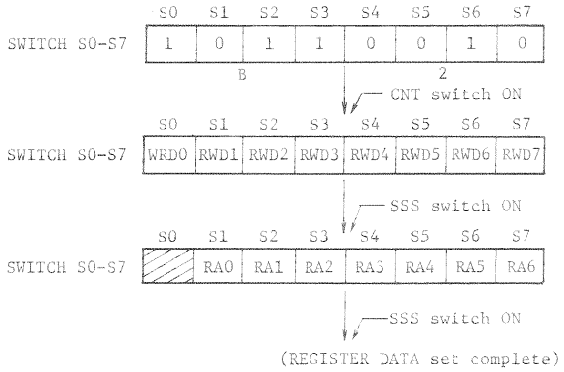
If switches S0 - S7 are set to X'B2' and the CNT switch is ON, Register Write Mode is set.

(2) Setting of data to be written in the microprogram register

After setting to Register Write Mode, data to be written is set onto switches S0 - S7 and the SSS switch is made ON. Then by setting switches S0 - S7 to X'A2', write data can be indicated on lamps L4 - L11.

(3) Write into the Microprogram Register

If S1 - S7 Register Address are set to SSS switch is ON.



(REGISTER DATA set complete)

. RWD0-7 REGISTER WRITE DATA0-7

. RA0-6 REGISTER ADDRESS0-6

3.2 Setting the Command Code

Using the Register Write function (See 3.1), any desired Command Code can be written into the Command Register whose register address is X'3D'.

3.3 Setting the Device Address

Using the Register Write function (See 3.1), any desired Device Address can be written into the Device Address Register whose register address is X'3E'.

Three bits (BIT 5 - 7) of the register are used to set the device address in binary notations.

Bit 0 indicates SBCT to be mentioned later.

3.4 Setting the Byte Count

Using the Register Write function (See 3.1), any desired Byte Count can be written into the Byte Count Register whose register address is X'3F'.

The Byte Count value set by switches S0 - S7 changes its weight depending on the bit 0 "SBCT" of the register whose address is X'3E'.

Weight of Byte Count Value

Switch / Weight of Byte Count	S0	S1	S2	S3	S4	S5	S6	S7
SBCT = True	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
SBCT = False	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4

3.5 Setting the Command Parameter

Any desired parameter for offline command execution can be set with the Register Write function (See 3.1).

Bit assignments of the microprogram registers whose register address are X'3C' and X'3E' are as follows:

Command Parameters

Bit / Reg. Name / Address	0	1	2	3	4	5	6	7
Off-line Control X'3C'	U.STP	UC.RP	UX.STP	UX.RW	UX.RV	RPOS	REPET	TUSCAN
Off-line Device Address X'3E'	SBCT					DVA0	DVA1	DVA2

U.STP ; UNIT CHECK, STOP

If Unit Check occurs during command execution, it stops after executing the command.

UC.RP ; UNIT CHECK, REPOSITION

If Unit Check occurs during command execution, Repositioning is performed to retry the command after completing the command execution.
If UCK occures during write command execution, Back Space and Erase operation is automatically performed.

UX.STP; UNIT EXCEPTION, STOP

If Unit Exception occurs during command execution, it stops after executing the command.

UX.RW ; UNIT EXCEPTION, REWIND

If Unit Exception occurs during command execution, Rewinding is done after completing the command execution.

UX.RV ; UNIT EXCEPTION, REVERSE

This is valid for the Read and Read Backward commands. If a Tape mark is detected when executing a command, the Read Command whose tape running direction is reversed is executed.

RPOS ; REPOSITION

After executing the command, it automatically repositions to process the same block again.

REPET ; REPEAT

The command is repeatedly generated as long as this bit is '1'. However, it is not generated if SINH bit is true.

TUSCAN; TAPE UNIT SCAN

If this bit is active, the device address is incremented after executing each command. After that, when a restart is indicated, the command is executed on the device whose address is the incremented value. If execution is impossible, the device address is increased until a device on which the command can be executed appears: When the device address becomes '8', the device address after increment is '0'.

SBCT ; SHORT BYTE COUNT

This determines the weights of bits of the Byte Count used in the offline command control. Refer to MAP M0006 "Set of Byte Count".

3.6 Start of Command Execution

After performing the operations described in sections 3.2 - 3.5, if SINH bit (See 4.1) is at flase, a command is issued by the SSS switch in ON. If the SINH bit is true, a command is not issued by the SSS switch in ON.

A command is executed once unless "REPET" is specified. After that, each time the SSS switch is made ON, a command is executed once. The result can be monitored using the indication function shown in MAP M0003 ~ M0005.

If "REPET" is specified, command execution starts when the SSS switch so set is "ON" and, next command is automatically issued without making the SSS switch ON. This is valid as long as "REPET" or SINH bit is specified.

"REPET" bit may be made OFF to stop issuing command.

Registers related to offline command execution are as follows:
Detail information of these registers are described on MAP M0011.

Table 1

Register Name	SDIA0	SDIA1	SDIA2	SDIA3	OFLCNT	OFLCMD	OFLDVA	BCT
Address	38	39	3A	3B	3C	3D	3E	3F
bit 0	DMW/DMR				STP.UCK		SBCT	
1	MARG	INV	•MASK track	GDT lower	RPS.UCK	CMD code		BYTE Count
2	IPOST/XFR		•Marginal Address or		STP.UEX		(RPSCY)	
3	GDT		•GDT Upper		REW.UEX		(REVCY)	
4	IPRE/MARA				REV.UEX		(OFSCY)	
5	SLWR	MASKP			RPS		OFDVA0	
6	MASK				REPEAT		OFDVA1	
7	TMTC				TUSCAN		OFDVA2	

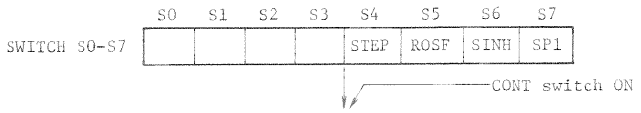
4. Control of Microprogram

Pause, single step, and address comparison of microprogram can be executed from the Field Tester. These functions are explained in this section. Functions described in this section are valid regardless of the MTC condition (online or offline) and they are not reset when ONL/OFL is switched.

4.1 Specify/Release of Microprogram Control Function

After setting switches S0 - S3 to X'E' and setting the necessary bits of switch S4 - S7, control functions of the microprogram are specified when the CNT switch is made ON, and the lamps of the corresponding bits between L4 - L7 light.

In order to release the specified control functions, set S0 - S3 to '1110' and the necessary bits of S4 - S7 to '0' and make the CNT switch ON.



STEP ; Set to '1' to put the microprogram into the single step mode. Single step is executed with the SSS switch.

ROSF ; READ ONLY STORAGE FUNCTION

While this bit is active, data is continuously read from the control ROM in the microprocessor and is parity checked.

When any parity error occurs, it stops at the address where 1 is added to the address where the error was detected.

SINH ; START INHIBIT

When this bit is active, command issue in the offline mode is inhibited.

SP1 ; SPARE 1

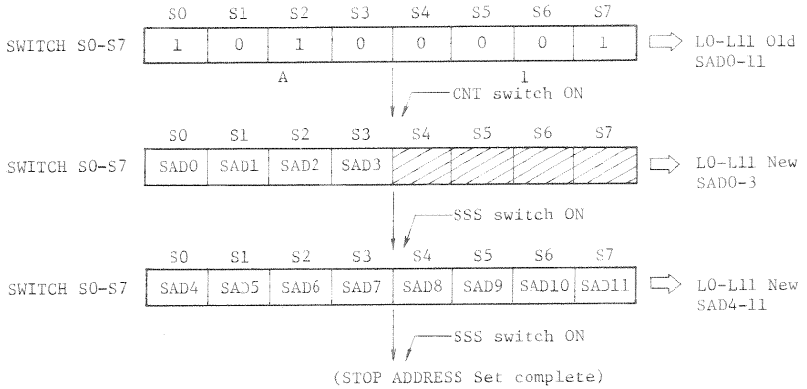
4.2 Setting the Stop Address

(1) Setting the Stop Address Mode

If switches S0 - S7 are set to X'A1', the stop address at SAD0 - SAD11 is indicated on L0 - L11 (See 2.3). To change the stop address, set switches S0 - S7 to Stop Address Mode by making the CNT switch ON.

(2) Setting the Stop Address

After setting to the Stop Address Mode, set the upper 4 bits of a stop address (SAD 0 - 3) on switches S0 - S3 and make the SSS switch ON. Also, set the lower 8 bits of the stop address (SAD 4 - 11) on switches S0 - S7 and make the SSS switch ON. The set stop address can be confirmed with the Stop Address Display function.



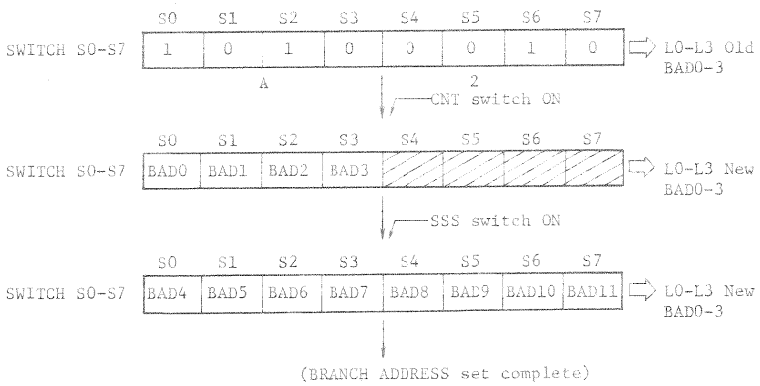
4.3 Setting the Branch Address

(1) Setting the Branch Address Mode

If the CNT switch is made ON with setting switches S0 - S7 to X'A2', the Branch Address Mode is set to.

(2) Setting the Branch Address

After setting to the Branch Address Mode, set the upper 4 bits of the branch address on switches S0 - S3 and make the SSS switch ON. The Branch Address of the upper 4 bits set can be confirmed with the Branch Address Display function (See 2.4). The lower 8 bits of the branch address are set by switches S0 - S7. (The Branch Address Register is provided only for the upper 4 bits.)



4.4 Setting the Microprogram Address

When the microprogram is in the step mode, the microprogram can be branched to a certain address from the Field Tester by changing the contents of the CS address the Field Tester by changing the contents of the CS address register. After changing the CS address, if the program is single-stepped using the SSS switch, maintaining the step mode, the program is executed from the changed address. If the step mode is released, the microprogram starts from the changed address.

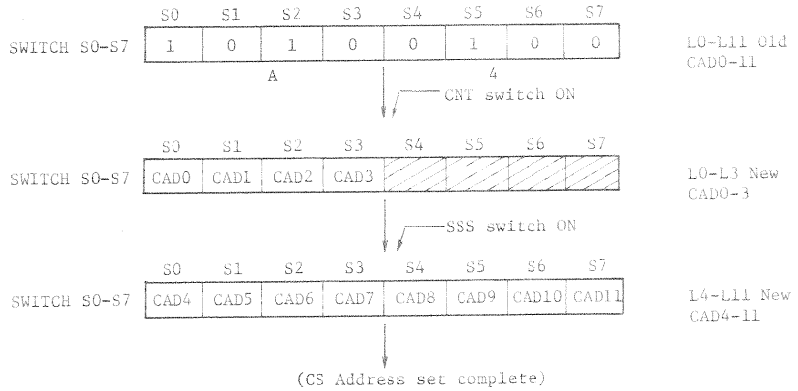
(1) Setting the Microprogram Address Mode

After setting the microprocessor into the Step Mode and setting switches S0 - S7 to X'A4', switches S0 - S7 are set to the CS address mode by making the CNT switch ON.

(2) Setting the CS Address Register

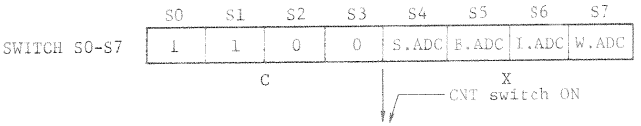
After setting Microprogram Address Mode, set the upper 4 bits of the CS address (CAD0 - 3) on switches S0 - S3 and make the SSS switch ON. Further, set the lower 8 bits of the CS address on switches S0 - S7 and make the SSS switch ON. Thus, the CS address is set into the CS address register.

The address set can be confirmed using the Microprogram Address Display function (See 2.5).



4.5 Setting the Address Compare Control Flag

Set switches S0 - S3 to X'C' and set the desired Address Compare Control Flag on S4 - S7. Then, make the CNT switch ON.



(ADDRESS COMPARE CONTROL FLAG Set complete)

S.ADC ; STOP, ADDRESS COMPARE

When the address of the microprogram coincides with the address specified by the Stop Address Register, it stops the microprogram.

B.ADC ; BRANCH, ADDRESS COMPARE

When the microprogram coincides with the address specified by the Stop Address Register, the microprogram is forced to branch to the address indicated by the Branch Address Register and SW0 - SW7.

I.ADC ; INDICATE, ADDRESS COMPARE

When the microprogram coincides with the address specified by the Stop Address Register, the contents of the register whose address is specified by SW1 - SW7 is displayed on L0 - L7.

W.ADC ; WRITE, ADDRESS COMPARE

When the microprogram coincides with the address specified by the Stop Address Register, the contents of the RWD (Register Write Data) register is written into the register whose address is specified by SW1 - SW7.

5. LAMP TEST/SYSTEM RESET

If switches S0 - S3 are set to '1', lamps L0 - L11 turn ON. Thus, System Reset is performed when the CNT switch is mode ON.

Note: Since System Reset causes Specify/Release of the Microprogram Control function (See 4.1) depending on conditions of S4 - S7, exercise care.

— Offline command execution parameters —

See MAP M0007.

(1) SDIA0 ∿ SDIA3 are the same as the 4 byte diagnostic flag specified in set diagnose command.

When MTC is in offline status, if diagnostic flag bytes are set directly in these registers (without executing the above commands), the specified diagnostic operation may be carried out by executing the command operation without chaining to SDIA command. The SDIA data once set, is not be altered till MTC is set to online status or system reset.

(2) Tape Unit Scan

When the OFLCNT register TUSCAN byte is set '1', the OFLDVA register (OFDVAO∿2 byte data) is advanced by +1. If repeat bit has also been set '1', commands are issued serially to all MTU's.

(3) REPEAT

When OFLCNT register, REPEAT bit is reset '0', a command is executed everytime the SSS switch is pressed.

Unless this bit is reset ('0'), (while REPEAT bit is '1'), the command activated by SSS switch is repeated continuously.

In this case all the functions specified by bits other than the REPEAT bit are valid.

(4) Reposition

The following offline repositioning operation is carried out irrespective of the end status when the OFLCNT register RPS bit is set.

The commands and addresses entered in OFLCMD and OFDDVAO∿2 remain unchanged even after offline repositioning operation.

Table 1 Offline Reposition

Commands set in OFLCMD register	Offline Reposition Operation
01 (Write)	Back space command is executed after a Write Command. However if TDBCK (ID Burst check) at sense byte 5 bit 3 or SAGC (byte8, bit4) is activated, Rewind Command will be executed instead of the Back Space Command.
02 (Read)	Back Space Command follows the Read Command. However, if NCAP (Not capable) has occurred, Rewind Command will be executed.
0C (Backward Read)	Space Command follows the Backward Read Command.
Other commands	No operation.

(5) UEX Function

The following operation is executed when UEX bit is included in the END status by using combinations of STP, UEX, REW, UEX, REV.UEX in OFLCNTL register.

Table 2 UEX Functions

STP .UEX	REW .UEX	REV .UEX	UEX Function Description
1	X	X	Processing is looped within the offline service routine from the time UEX bit turned ON till STP.UEX bit is reset '0' or SINH is specified.
0	0	0	No operation (UEX bit is not checked)
0	0	1	When UEX bit is set '1' the OFLCMD register command codes are replaced by Reverse Commands as follows: Old OFLCMD → New OFLCMD WT(01) → BRD(0C) RD(02) → " BRD(0C) → RD(02) SP(37) → BSP(27) BSP(27) → SP(37) ERS(17) → BRD(0C) WTM(1F) → BSPF(2F) DSE(97) → BSPF(2F) NOP(03) → BRD(0C) Others → Not changed
0	1	0	Rewind Command is issued when UEX bit is set '1'.
0	1	1	Rewinds MTU by issuing a rewind command when UEX bit is set ('1'). At this stage F617/F618 MTUs are reversed from Normal Speed to High Speed or from High Speed Mode to Normal Speed.

(6) UCK Function

If UCK bit is included in End Status, the operations shown in the following table 5.13 are carried out. The operations are specified by combinations of STP.UCK, RPS.UCK bits. ERRF lamp is turned ON when the UCK bit is set '1' (Errors may be detected by checking this lamp).

Table 3

STP .UCK	RPS .UCK	UCK Function Description
0	0	UCK bit is not checked.
0	1	The repositioning operation described in (4) is executed when the UCK bit is set '1'. Any errors in this operations are iquored (UCK).
1	0	Processing is looped within the offline service route from the time UCK bit is set '1' till STP.UCK bit is reset or SINH is specified.
1	1	The repositioning operation in (4) is executed when the UCK bit is set. Any new errors (UCK) during repositioning operation are looped in the offline service routine till STP.UCK bit is reset '0' or SINH is specified.

(7) SINH (Start Inhibit)

When SINH bit on the field tester is ON, commands from SSS switch are inhibited.

A loop created by STP.UCK or STP.UEX bits may be released by setting the SINH bit. (If SINH is turned OFF again, commands will be issued again (in case of REPEAT)).

Commands are temporarily inhibited if SINH bit is set (ON) when REPEAT has been specified. This fascilitates temporary stopping or starting of commands in manual mode.

M0100	Example of Field Tester Operation

Table 1 is a list of various functions of field tester operation.

Practical examples of field tester operation will be described in M0110 through M0200. The method of the description used in these examples will be explained below.

Expression X'0F' indicates that S0 - S7 are to be set to a hexadecimal '0F', and expression X'0F' CNT indicates that after S0 - S7 are set to '0F' and the switch CNT is turned on.

Similarly, expression X'3B' SSS indicates that S0 - S7 are set to a hexadecimal '3B' and switch SSS is turned on.

Expression "ONL/OFL = ONL" indicates that the switch ONL/OFL of field tester is turned to the ONL position.

Accordingly, expression "ONL/OFL = OFL" indicates that this switch is turned to the OFL position.

The practical examples given hereinafter are those considered effective for maintenance, which do out, however, encompass the examples explaining all the functions of field tester listed in Table 1.

Table 1 A list of operational functions of field tester

Item	Switch S0	S1	S2	S3	S4	S5	S6	S7	Hex. code	Set key		Display L0	L1	L2	L3	L4	L5	L6	L7	L8	L9	L10	L11
1	0	RA0	RA1	RA2	RA3	RA4	RA5	RA6	00∿7F	CNT	Register display	REG 0	REG 1	REG 2	REG 3	REG 4	REG 5	REG 6	REG 7				
2	1	0	0	0	0	0	0	0	80		Interface signal display	SLIC	OP1	DXFO	RQIA	RTA	DXRQ	MCY	B1600	ERRF	ACMP	PHLT	PERR
3	1	0	1	0	0	0	0	1	A1		Stop address display												
	1	0	1	0	0	0	0	1	A1	CNT	Stop address mode	SAD 0	SAD 1	SAD 2	SAD 3	SAD 4	SAD 5	SAD 6	SAD 7	SAD 8	SAD 9	SAD 10	SAD 11
	SAD 0	SAD 1	SAD 2	SAD 3					XX	SSS	Set upper SAD												
	SAD 4	SAD 5	SAD 6	SAD 7	SAD 8	SAD 9	SAD 10	SAD 11	XX	SSS	Set lower SAD												
4	1	0	1	0	0	0	1	0	A2		Branch address display												
	1	0	1	0	0	0	1	0	A2	CNT	Branch address mode	BAD 0	BAD 1	BAD 2	BAD 3	RWD 0	RWD 1	RWD 2	RWD 3	RWD 4	RWD 5	RWD 6	RWD 7
	BAD 0	BAD 1	BAD 2	BAD 3					XX	SSS	Set upper BAD												
	BAD 4	BAD 5	BAD 6	BAD 7	BAD 8	BAD 9	BAD 10	BAD 11	XX		Set lower BAD												
5	1	0	1	0	0	1	0	0	A4		CS address display												
	1	0	1	0	0	1	0	0	A4	CNT	CS address mode	CAD 0	CAD 1	CAD 2	CAD 3	CAD 4	CAD 5	CAD 6	CAD 7	CAD 8	CAD 9	CAD 10	CAD 11
	CAD 0	CAD 1	CAD 2	CAD 3					XX	SSS	Set upper CAD												
	CAD 4	CAD 5	CAD 6	CAD 7	CAD 8	CAD 9	CAD 10	CAD 11	XX	SSS	Set lower CAD												
6	1	0	1	1	0	0	1	0	B2		Register write display												
	1	0	1	1	0	0	1	0	B2	CNT	Register write mode	BAD 0	BAD 1	BAD 2	BAD 3	RWD 0	RWD 1	RWD 2	RWD 3	RWD 4	RWD 5	RWD 6	RWD 7
	RWD 0	RWD 1	RWD 2	RWD 3	RWD 4	RWD 5	RWD 6	RWD 7	XX	SSS	Register write data												
		RA0	RA1	RA2	RA3	RA4	RA5	RA6	XX	SSS	Register address												
7	1	1	0	0	S. ADC	B. ADC	I. ADC	W. ADC	CX	CNT	Address compare control & display	S0	S1	S2	S3	S. ADC	B. ADC	I. ADC	W. ADC				
8	1	1	1	0	STEP	ROSF	SINH	SP2	EX	CNT	MP control RSL & display	S0	S1	S2	S3	STEP	ROSF	SP1	SP2				
9	1	1	1	1					FX		Lamp test	1	1	1	1	1	1	1	1	1	1	1	1
10	1	1	1	1	STEP	ROSF	SINH	SP2	FX	CNT	System reset & MP control	1	1	1	1	1	1	1	1	1	1	1	1

RA0 ∿ RA6 : Register address
SAD0 ∿ SAA11: Stop address
BAD0 ∿ BAD11: Branch address
CAD ∿ CAD11 : CS (microprogram) address
RWD ∿ RWD7 : Register write data

- Address Compare Function -

S.ADC : Stop with address compare
B.ADC : Branch with address compare
I.ADC : Indicate address compare
W.ADC : Write register address compare

- Microprocessor Control Function -

STEP : Microprocessor step
ROSF : Read only strage function
SINH : Start inhibit
SP2 : Spare 2

M0110	Example of Field Tester Operation (Register Display)

Register Display

The microprocessor of the MTC aims at accomplishing a predetermined work through the control of 104-byte register (out of which 64 bytes are used for the RAM. (See M0111.)

Using a field tester, the contents of these registers can be displayed at any time.

The procedure for display is to set the objective register address to S0 - S7 and turn on CNT switch.

If the microprocessor in the MTC is in the halt status[1)], what is to be done is only to set the register address to S0 - S7 and the CNT switch does not have to be operated, so the operation is simpler.

Through this operation, the content of the register is displayed on L0 - L7.

Note 1: When the microprocessor in the MTC is set in the STEP status or when the microprocessor turns to the halt status by an address compare stop function, PHLT bit (the L10 to be used when S0 - S7 are set to X'80'.) lights.

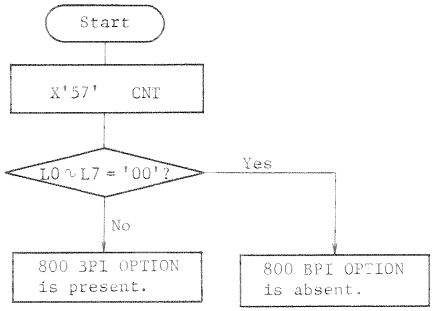
Register display:

```
X'YY'    CNT
     YY: Register address
```

Example 1: Inspection of the Presence or Absence of 800 BPI OPTION

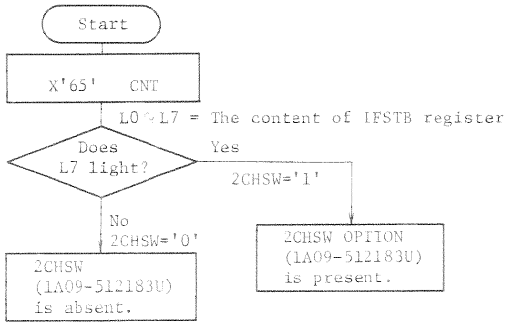
Whether the 800 BPI OPTION PCB is equipped can be ensured by observing whether the PCB of 512189 is inserted in column 1A01 of the MTC. To check whether the insertion of the PCB has been ensured by the microprocessor, it is intended to ensure it through register display

If a 800 BPI OPTION is present, the content of ZOP register (register address '57') can be one other than '00'. Now, let's display the content of register address 57.



Example 2: Inspection of the Presence or Absence of 2CH SWITCH OPTION

Similarly to the example 1 let's try to check 2CHSW bit (Bit 7 of IFSTB register - address '65')



M0111	MTC Register Table

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	
Nickname	DVENQ0	DVENQ1	DVENQ2	DVENQ3	DVENQ4	DVENQ5	DVENQ6	DVENQ7	MODEM	SCANP	DSB	LCMD	DVS0	DVS1	DVS3	DVS8	Nickname
0	0 RSVA0	Enquiry memory for each Device							1600A	CCF	(OST)		Device sense byte stack				0
	1 LENQA0								800A	INST	STM						1
	2 BENQA0								1600B	RMTU	CUE	LAST					2
	3 SENQA0								800B	WORK	BSY	COMMAND					3
	4 RSVB0								CUBMA		CHE	CODE					4
	5 LENQB0								CUBMB	DVA0	DVE						5
	6 BENQB0									DVA1	UCK						6
	7 SENQB0									DVA2	UEX						7
Nickname	W0	W1	W2	W3	W4	W5	W6	W7	MCYENT	CMDSEQ	SUB0	SUB1	PDSB(00)	Q1	Y0	Y1	Nickname
1	0	Temporary working register							Static working registers								0
	1																1
	2																2
	3																3
	4																4
	5																5
	6																6
	7																7
Nickname	SB0	SB1	SB2	SB3	SB4	SB5	SB8	SB9	SB10	SB11	SB22	SB23	R0	R1	CMD	DVA	Nickname
2	0 CMJ	NOIS	ET0	VRC	MPHE		IBGD	102CR	STRJ	RWTO							0
	1 IRQ	IUSA	ET1	MLT/LRC	RJTU		ET8	VLCG	CMRJ	MISP					Command	Device	1
	2 BOC	TUSE	ET2	SKW	TI	WIMC		XFBC	CIRJ	TAGTC					Code	Adrs	2
	3 EQC	(TOVR)	ET3	EDC/CRC	WVRC	IDBC	EBRC	CRC3	NBLK	REGE	(FRU1)	(FRU2)			Stack	Stack	3
	4 DCK	(BOT)	ET4	EVC		SRDC	SAGC	(6250CU)	DVRS	DMPE							4
	5 OVRN	(WRS)	ET5	1600	LWR	PREC	SBRC		TCSF	ROME	(E50)	(E51)					5
	6 WCZ	(FP)	ET6	BWD	TUC	POSE	SERC		(SRJF)	MPTRP							6
	7 (SPND)	NCP	ET7	PCMP	(WCALM)	(WEOVF)	VLRY		VLCK	(TUROM)							7
Nickname	ERC0	ERC1	ERC2	ERC3	ERC4	ERC5	ERC6	ERC7	SDIA0	SDIA1	SDIA2	SDIA3	OFLCNT	OFLCMD	OFLDVA	BCT	Nickname
3	0	Reserved (not used with F617/F618)							DMW/DMR				UC.STP		SBCT		0
	1								MARC	INV			UC.RP	OFFLINE			1
	2								IPVS/XFR		Diagnostic		UEX.STP	COMMAND	(RPSCY)	OFFLINE	2
	3								GDT		flag byte 2, 3		UEX.REW	CODE	(REVCY)	BYTE	3
	4								IPRE/MARA		stack		UEX.REV		(OFCY)	COUNT	4
	5								SLWR2	MSDKP			RPOS		OFLDVA0		5
	6								MASK				REPEAT		OFLDVA1		6
	7								TMTC				TUSCAN		OFLDVA2		7
Nickname	TMCTL	TIMER	DVSEL	DVRSV	DVTAG	DV30	DVB1	DVSNS	MASK	DACTL	WTCTL	RDCTL	MODE	RDSNS	CRCST	FMERR	Nickname
4	0 MCT0	CT0/8	TAG1	RSV0	GO	DB00	DB10	GAPC	MASK0	DMW	WTM	ROK	MCY	HNOIS	*MCRC	*SRDC	0
	1 MCT1	CT1/9	XCAL	RSV1	TAGVL	DB01	DB11	CPFWD	MASK1	DMR	IBW	STPHR	BWD	HBLK	*MCRCZ	*EDC	1
	2 CQTP	CT2/10	*DVENB	RSV2	TAG0(STS)	DB02	DB12	MPXBO	MASK2	IHPRE	WEC	VFOS	WRS	HTM	*EP=CR	*SLIPC	2
	3 ERRF	CT3/11	SLTAG	RSV3	TAG1(CTL)	DB03	DB13	MTCS	MASK3	IHPOS	ALIWT	IHDXF	ERD	WIND	*B=D	*NOISC	3
	4 RCNT/SCNT	CT4/12	DVBSY	RSV4	DBMPX	DB04	DB14	VLOK	MASK4	INVLD	WOK	IHCOR	6250	PHOK	*B=C	*WBOC	4
	5 RCTRU/CTRU	CT5/13	DVA0	RSV5	TSP0	DB05	DB15	RVLC/VLCG	MASK5	ALMSK	'0'	*HIG	1600	PREA	*MCRCC	*WVRC	5
	6 RFTP/DFTP	CT6/14	DVA1	RSV6	TSP1	DB06	DB16	TCSG	MASK6	MASK	BFUL	ISPHE	CMCY	POSA	*A=B	*OVRN	6
	7 RQTP/DQTP	CT7/15	DVA2	RSV7	VHSP	DB07	DB17	TCSP	MASK7	MASK8	RBCY/BCY	SKWMG	CBR	EPOSA	*XBIC	*CMP	7
Nickname	TSNS	POINT	ELFMT	RDERR	ZETK	ZCTL	ZMRG	ZOP	TCADA	OUTAG	CHBO	IFSTA	INTAG	CEB1	IFCTL	XFCTL	Nickname
5	0 *TSNS0	*DET0	*IORCR	*VRCE	ETK0	SFCRC	*NVRCE		CADA0	ADO	CBO0(RCT0)	CUBSA	OPI	CB10	RRSA/OVR2	DXF1	0
	1 *TSNS1	*DET1	*DET8	*MLTE	ETK1	LRC	ETK8	8000P	CADA1	CMO	CBO1(RCT1)	SPOA	MADI	CB11	S.BCT/*XTAC	DXF0	1
	2 *TSNS2	*DET2	*TSNS8	*SKWE	ETK2	CRC	*NSKEW	8000P	CADA2	SVO	CBO2(RCT2)	SERA	MSVI	CB12	SBCT/DXFE	MPRD	2
	3 *TSNS3	*DET3	*DIBG	*DBCR	ETK3	HBLKN	SDRST/*LRCE	CANY1	CADA3	SLIG	CBO3(RCT3)	SYRA	MSTI	CB13	SUCT/DXRQ	SCAN	3
	4 *TSNS4	*DET4	*DNOIS	*DROE	ETK4	BLKEJ	TM0		CADA4(CM0)	OPOA	CBO4(RCT4)	IFONA	RQIAF	CB14	SDCT/BIBSY	EBOP1	4
	5 *TSNS5	*DET5	*DBOB	PNMLT	ETK5	CRCHG	TM1		SBMC (CM1)	RQSPE	CBO5(RCT5)	RTA	RQIBF	CB15	CISTP/*ABPC	CMROM	5
	6 *TSNS6	*DET6	*DARA	*POJAE	ETK6	CRCRG	TM2		CPBL (CM2)	QIS	CBO6(RCT6)	JRTO/RTB	DSC1	CB16	RRCT/*BOPC	ROM2	6
	7 *TSNS7	*DET7	*DIM		ETK7	RRDB/RDBS	TM3		*OFS (CM3)	INS	CBO7(RCT7)	WRTO/URRT	DCN	CB17	RCRY/CRCT	ROM1	7
Nickname	TRAP	MPERR	VFSNS	UQID	TCADB	IFSTB	RTSNS	RTCTL									Nickname
6	0 T.INT	MRER/RENB	SINH	*MRX	CADB0	CUBSB	(INHA)	DSOKA	Not used								0
	1 T.TMR	RPER/OFL	SP2	*IBRY	CADB1	SPOB	(INHB)	DSOKB									1
	2 T.INS	CSPE	F.C=S	*AGAP	CADB2	SERB	(*BWE)	CRVA									2
	3 T.PER	REGE	M	1800	CADB3	SYRB	(BFRE)	CRVB									3
	4 M.INT	MEC0	SW7		CADB4	IFONB	(RQIB)	SSW/SW									4
	5 M.TMR	MEC1	VFOH		SP5	OPOB	0	RUSE/*WE									5
	6 M.INS	MEC2	VFOM		SP6	'0'	GINHB	RRSB									6
	7 TMSK	MEC3	VFOL		SP7	2CHSW	GINHA										7

M0120	Example of Field Tester Operation (Interface Signal Display)

Interface Signal Display

Principal signals of interface that indicate the operational condition of the MTC and signals indicating the status of the microprocessor can be displayed by a field tester.

The display function is available when the MTC is in any status.

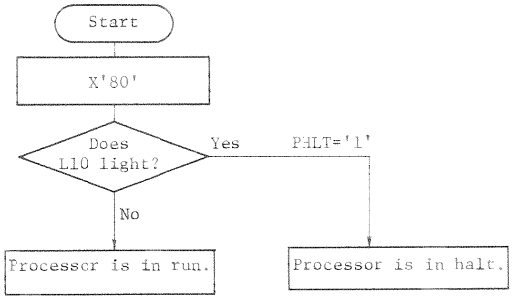
The procedure for display has only to set a hexadecimal '80' to S0 - S7. Then, an objective signal can be displayed on L0 - L11. (See M0003.)

Interface Signal Display:

X'80'

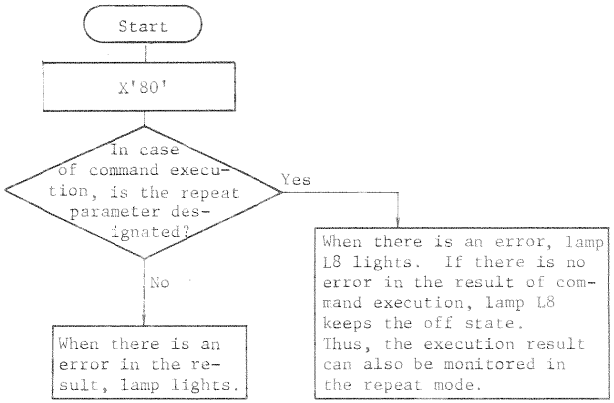
Example 1: The Microprocessor is Inspected Whether It is in the Halt Status.

When PHLT signal is '1', it indicates that the microprocessor is in the halt status.



Example 2: Monitoring of ERRF Bit

When setting the MTC in the offline status and executing a command from a field tester, the MTC is informed of the result of the execution through ERRF bit. When ERRF='1', it indicates that there is an error.



M0130	Example of Field Tester Operation (Microprogram Address Display)

Microprogram Address Display

A microprogram for the MTC is stored in the ROM which plays a role of control storage (CS). The processor takes out microinstructions of the microprogram from the CS. The content of the address register for reading out microinstructions from the CS can be displayed using a field tester.

When the processor is in the 'STEP' status, the step forwarding of the program sequence can be ensured, while if the processor is in the 'RUN' status the you can see the lighting condition of L0 , which is effective for maintenance.

The procedure for display has only to set S0 - S7 at 'A4'.

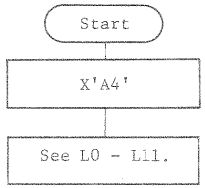
CS ADDRESS DISPLAY:

X'A4'

The CS address can be set at a desired value only when the processor is in the 'STEP' status, and instruction can be stepped forward (To do such things, it is necessary to know the detail of the microprogram). The CS address set functions are as follows.

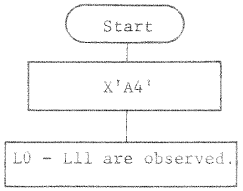
(X'E8'	CNT ..... STEP)	
X'A4'	CNT	
X'&x'	SSS	X: Arbitrary
X'mn'	SSS	
	Set address '&mn'.	

Example 1: Lets try to inspect the CS address with the processor being in the 'RUN' status to investigate the idle state of the MTC.



- When the MTC is in the idle state, the idle program is stored in the lower address ('0XX' - '1XX') of CS. Accordingly, L0 - L2 are turned off, and L3 - L11 are half bit (half lighting of '1FF').

Example 2: Observation of CS address during the execution of command



- In company with the execution of command, L0 - L11 blink.

M0140	Example of Field Tester Operation (Register Write)

Register Write

Arbitrary data can be written in registers controlled by the microprocessor of the MTC using a field tester.

Using this function, the operator of field tester can provide the microprogram of the MTC with various data. For example, in case of the execution of a command in the offline mode, various parameters necessary for the execution of a command can be specified by writing data in a particular register. For maintenance purpose, the register write function is important as a means of specifying parameters.

The method of writing predetermined data in a register is to execute the following procedure.

REGISTER WRITE:

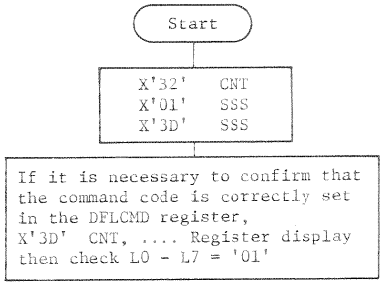
X'B2'	CNT	
X'dd'	SSS	dd: Write data
X'aa'	SSS	aa: Register address

Other applications of the register write function is to carry out the manual control on the MTC or the MTU by executing various register write operations according to a predetermined procedure. However, since such case requires the detailed knowledge about register, the register write function would not be 50 useful for maintenance purpose.

Example 1: Command Code Setting to Offline Command Register

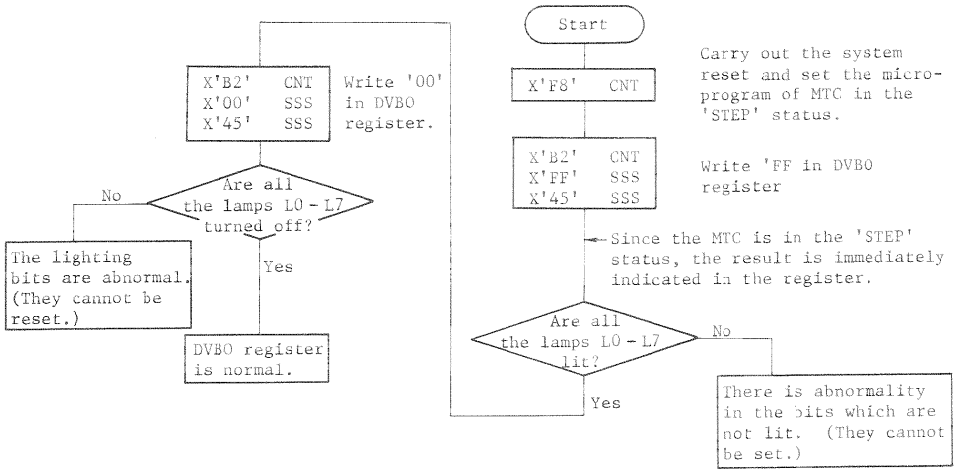
To issue a command from a field tester in the offline mode of the MTC, the command code needs to be set in the DFLCMD register (address '3D').

As an example, let's try to write the write command code ('01') in the DFLCMD register.



Example 2: Register Function Check

If there is doubt about the function of a register, a field tester is useful for writing data in the register by using the register write. Let's try to take DVB0 register (address '45') as an example.



M0150	Example of Field Tester Operation (CS Parity Scan)

With the use of a field tester, all the addresses ('000' - 'FFF') of CS can be scanned to check its parity.

To start CS parity scan, the ROSF bit has only to be set.

When the scan begins, it is repeated until the ROSF bit is reset or a parity error is detected.

CS Parity Scan Starts

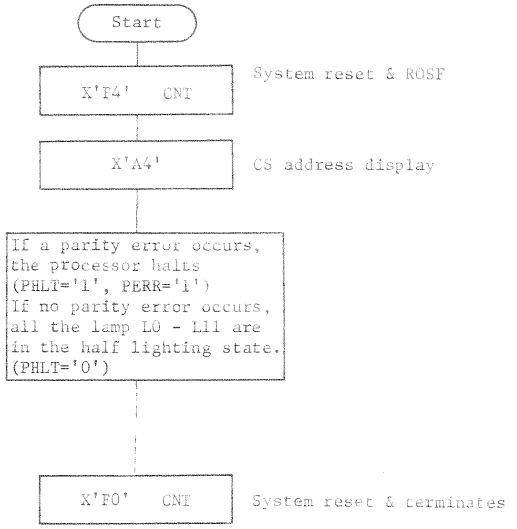
X'F4'	CNT

Ends

X'F0'	CNT

In addition, as STEP bit in conjunction with ROSF bit are set, the scan is stepped forward by switch SSS.

Example: Carrying out the parity scan of all the addresses of CS.



M0160	Example of Field Tester Operation (Address Compare)

A field tester can ensure that control passes a particular microprogram address. Also when control passes the address, field tester can direct the processor to halt, to carry out bypassing to another address, to display the content of register, to write data in a register, and so on.

However, to use these functions efficiently, it is necessary to have a knowledge of the contents of the microprogram and registers. In this sense, these functions are not usually used for the maintenance purpose. Here, an example of using these functions is introduced for reference.

Whether control passes a particular microprogram address can be ensured only by displaying the ACMP signal. (See M0003.) The ACMP signal can be reset by turning on the SSS switch.

Other functions are specified by the following procedure.

X'Cy' CNT

y:	0	1	2	3	4	5	6	7
	1	1	0	0	S.ADC	B.ADC	I.ADC	W.ADC
	'C'				y			

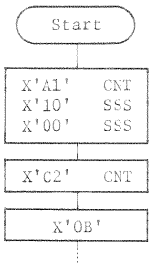
The compare address is set by the following operation.

X'A1'	CNT	
X'&x'	SSS	x: Arbitrary
X'mn'	SSS	&mn: Compare address

In addition, since the compare output appears at card pin BE2 of 1A07 (512185U), the passing timing can be observed by an oscilloscope.

Example 1: Confirmation of the Execution of a Trap Analysis Routine

When a trap occurs in the processor of the MTC, control passes microprogram address '100'. The example of displaying the content of LCMD register (address '0B') at the time when a trap occurs is explained below.



Compare address = '100'

I.ADC

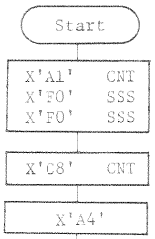
Indicate register address

Command execution

When initiation from the channel takes place, a trap occurs. Accordingly, every time the initiation takes place, the content of LCMD register, the code of the command executed the most recently, is displayed.

Example 2: Address Compare Stop

The example of halting the processor immediately after control passes microprogram address 'FF0' of the MTC is shown below. Address 'FF0' is the address which control passes when a reset routine is executed.



Compare address 'FF0'

S.ADC

CS address display

When it is intended to execute the reset routine, the processor halts. Then, L0 - L11 (CS address) display the next address. To release the processor from the halt status, switch SSS has only to be turned on. However, if the address compare is successful again, the processor will halt.

M0170	Example of Field Tester Operation (Command Execution in the Offline Status of the MTC)

If the MTC is in the offline mode, a command can be issued to the MTC by using a field tester. Command code, byte count, device address, and other parameters can be provided by writing appropriate data in predetermined registers.

All the registers concerned with command execution in the offline mode of the MTC are listed below.[1)]

SDIA0 (address '38')	}	Diagnostic flag bytes 0 - 3
SDIA1 (address '39')		
SDIA2 (address '3A')		
SDIA3 (address '3B')		
OFLCNT (address '3C')	...	Command execution control parameter
OFLCMD (address '3D')	...	Command code
OFLDVA (address '3E')	...	Device address
BCT (address '3F')	...	Byte count

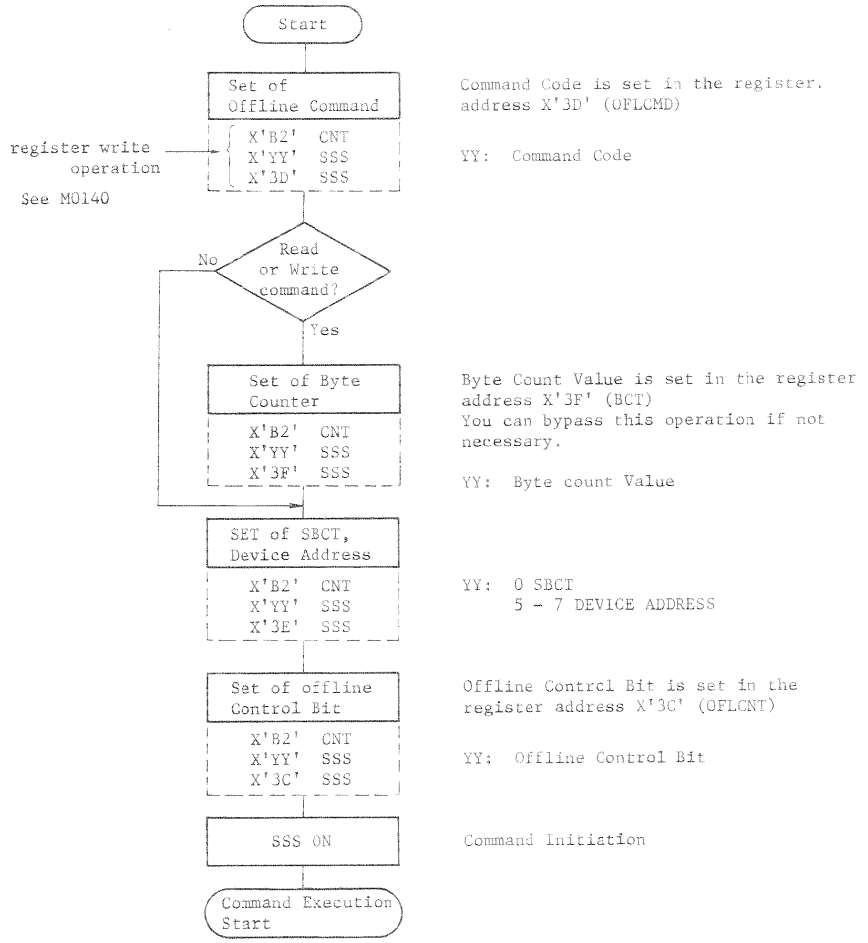
Since these registers are not reset[2)] except the case of the MTC power on, once they are set it is not necessary to set them again unless any change is required.

Note 1: The write data in a write command is always 'FF'. Also, the data read by a read command is not sent out to the channel.

Note 2: When the command reverse function (REV.UEX parameter) is specified, the content of OFLCMD register changes. Also, when TUSCAN parameter is specified the content of OFLDVA register changes.

Example: Command Execution

Contents of SDIA0 - SDIA3 are usually '00'. The following operation is carried out when it is ensured that the contents of these registers are '00'. Also, the content of SINH is '0'.



M0171	Example of Field Tester Operation (Unit-Check Parameter)

When a command is executed in the offline mode of the MTC by a field tester, the following operations can be done if the result of the command execution causes an error (Unit-check is set). These operations are specified by UC.STP and UC.RP bits (bit 0 and bit 1) of OFLLCNT register (address '3C').

Unit-Check Parameters

UC.STP	UC.RP		
0	0	....	No function
0	1	....	When UCK occurs the repositioning operation is carried out. Then, an error occurring during repositioning is disregarded. (See Note 1.)
1	0	....	When UCK occurs the microprogram carries out looping after executing a command. The looping continues until SINH bit is set, UC.STP parameter is reset, or the system reset is carried out. (See Note 2.)
1	1	....	When UCK occurs the repositioning operation is carried out. If there is an error newly occurring during repositioning, a microprogram performs looping after repositioning operation. The release condition for looping is the same as the above.

NOTE:

1) Repositioning operation

For the write command ⟶ After backspacing an error block, an erase command is executed. (In case an error occurs during IB writing, a rewind command is executed.)

For the read command ⟶ An error block is backspaced.

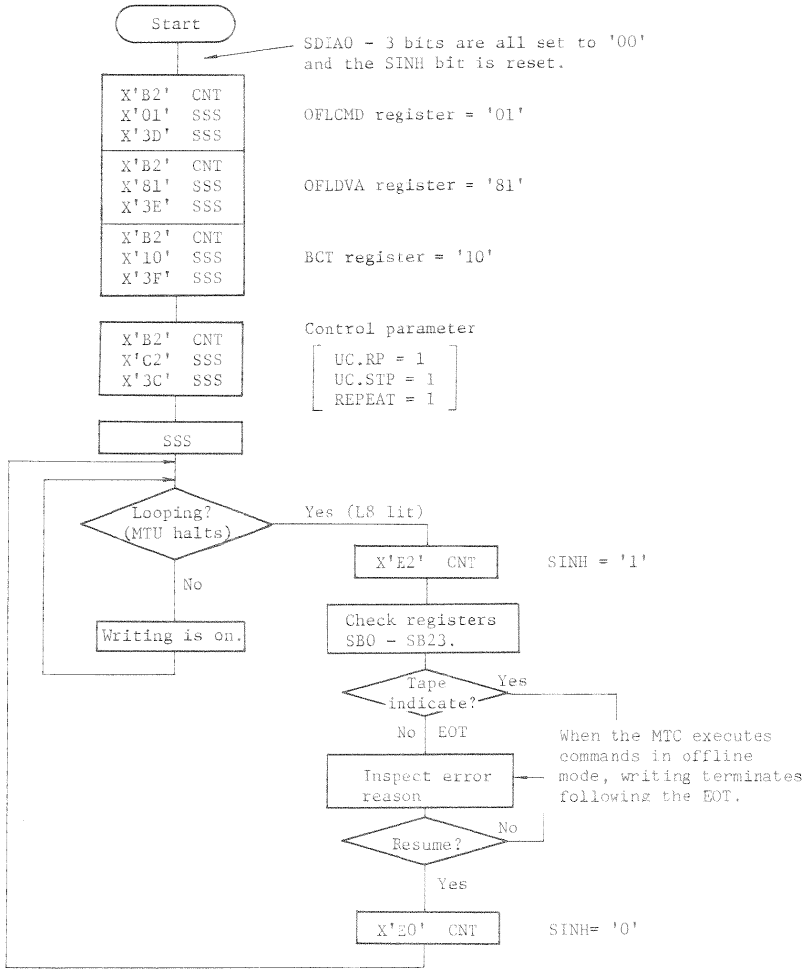
For the read backward command ⟶ An error block is spaced.

For other commands ⟶ No operation

2) SINH

If UC.STP or UEX.STP parameter is specified and a microprogram carries out looping, the loop is released when this SINH bit is set. If REPEAT parameter is specified the issuance of the next command is suppressed by setting this SINH bit on, so the command execution can be resumed by resetting the SINH bit again. (Refer M0008)

Example: Writing a 16-byte data pattern in the MTU of physical unit address. It is assumed that writing is carried out as far as the EOT and, when there is a write error, repositioning takes place. The example also assumes that when there is a repositioning error, writing is interrupted, looping is executed and then sense byte is checked.



M0172	Example of Field Tester Operation (Unit-Exception Parameter)

In case a field tester executes a command in the MTC offline mode, the following operations can be handled by the field tester if the terminate status contains 'Unit-Exception' parameter.

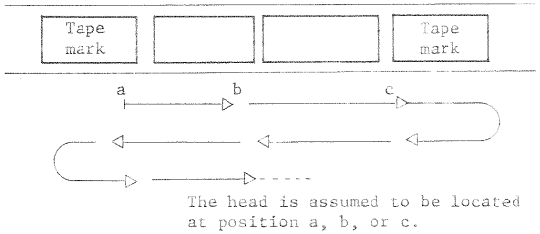
UEX Parameters

UEX.STP	UEX.REW	UEX.REV		
1	X	X	...	When detecting UEX, the micro-program is looped. Release from the loop can be done by resetting UEX.STP parameter, setting the SINH bit, or by the system reset.
0	0	0	...	No function
0	0	1	...	When detecting UEX, the content of OFLCMD register is converted into the reverse command code[1] and execution is continued.
0	1	0	...	When detecting UEX, the REWIND command is executed.
0	1	1	...	When detecting UEX, the REWIND command is executed, and then the speed mode is reversed (Normal speed ↔ high speed) to continue the command execution.

NOTE 1)
Reverse commands

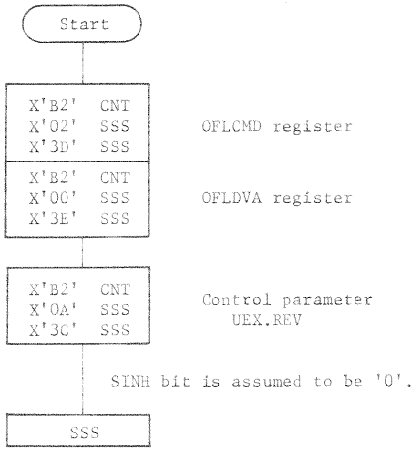
Old OFLCMD		Reversed new OFLCMD	
WRT (01)	⟶	RDB (0C)	..... At the time of detecting the EOT
RDF (02)	⟶	RDB (0C)	..... At the time of detecting a tape mark
RDB (0C)	⟶	RDF (02)	..... At the time of detecting a tape mark
SP (37)	⟶	BSP (27)	..... At the time of detecting a tape mark
BSP (27)	⟶	SP (37)	..... At the time of detecting a tape mark
ERS (17)	⟶	RDB (0C)	..... At the time of detecting the EOT
WTM (1F)	⟶	BSPF(2F)	..... At the time of detecting the EOT
DSE (97)	⟶	BSPF(2F)	
NOP (03)	⟶	RDB (0C)	
Others		No change	

Example: Repetitive forward and backward read of blocks between two adjacent tape marks on such tape as shown in Fig. 1.



The head is assumed to be located at position a, b, or c.

Fig. 1



M0173	Example of Field Tester Operation (TUSCAN Parameter)

When the MTC is in the offline mode, a field tester can issue a command to all the MTUs connected to the MTC sequencially.

The parameter used for this purpose is TUSCAN bit (Bit 7 of OFLCNT register address '3C').

When TUSCAN parameter is specified, the device address of OFLDVA register is increased by 1 (when the address was #7 it is changed to #0) when the microprogram of MTC completes the execution of a command given to a particular MTU (including the execution of such operation as the repositioning to be caused by control parameters if they are specified).

If a REPEAT parameter is not set, every time the SSS switch is operated commands are successively issued to all the MTUs connected to the MTC. If a REPEAT parameter is specified, what must be done is to operate only SSS switch once in the beginning.

It is not much practical to use TUSCAN parameter together with UC.STP parameter, for UCK is reported to the MTUs which are in the NOT READY status or which are not operational and therefore looping is not carried out every time a command is issued to the address of such MTU.

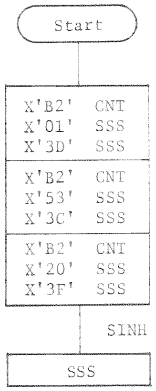
It is recommended to use TUSCAN parameter together not with UC.STP parameter but with UC.RP parameter and REPEAT parameter to operate a number of MTUs concurrently and observe their operation.

Example: Writing a 1024-byte data on tapes loaded on the MTUs numbered #0 - #3

When writing reaches the EOT, rewinding is to be carried out on the MTU and then writing is to be continued. (UEX.REW parameter)

When an error occurs during the write operation, repositioning is assumed to be carried out. (UC.RP parameter)

However, when an error occurs during the repositioning, looping is assumed to be prohibited.



When the command execution is executed by a field tester, the MTC is assumed to be always offlined.

OFLCMD register = 01

Control parameter
UEX.REW, UC.RP
REPEAT, TUSCAN

BCT ... 1024 bytes

SINH bit must be '0'.

Although the MTU which is not in the READY status is set in UCK (IRQ), the command issuance is executed. (No looping) Accordingly, the MTU may be set in the READY status after executing the above operation. In this case, when the MTU is set in the READY status, the write operation can start.

M0174	Example of Field Tester Operation (Go-Down-Time Parameter)

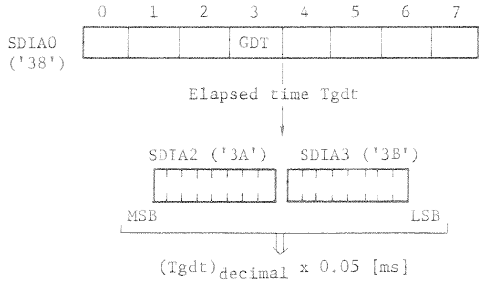
The diagnostic flag byte register (SDIA0 - SDIA3, address '38' - '3B') is always effective when the MTC is offlined.

(When the MTC is in the online mode, the diagnostic flag byte register is given by a SET DIAGNOSE command.)

Here, a practical example of the diagnostic flag byte register is shown by an example using the GDT (Go-Down-Time) parameter. (M0165 also explains TEST-MTC parameter).

GDT parameter aims at providing a predetermined elapsed time between the time when the execution of a command terminates and the time when the next command is issued.

This elapsed time is determined by the content of registers SDIA2 and SDIA3.



Example: Repetitive Forward Reading of Data Block N at Every 6.4 ms (Using RPOS parameter)

MTU #0 is loaded with such tape as shown in Fig. 1, and the magnetic head is assumed to be located at position a .

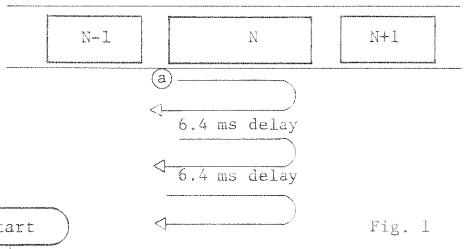
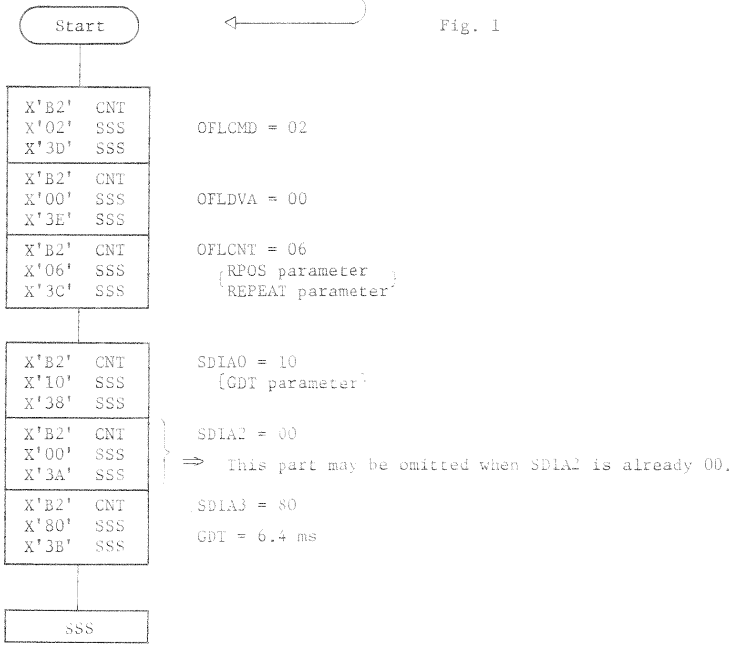


Fig. 1



M0175	Example of Field Tester Operation (TEST MTC)

When TMTC parameter is set at bit 7 of the diagnostic flag byte register 0 (SDIA0 - address '38') and a SET DIAGNOSE command (command code '4B') is issued, a diagnostic program for the hardware of the MTC can be executed.

	0	1	2	3	4	5	6	7
SDIA0 ('38')								TMTC

If there is an error in the diagnostic result, the unit check is contained in the end status. (EQC)

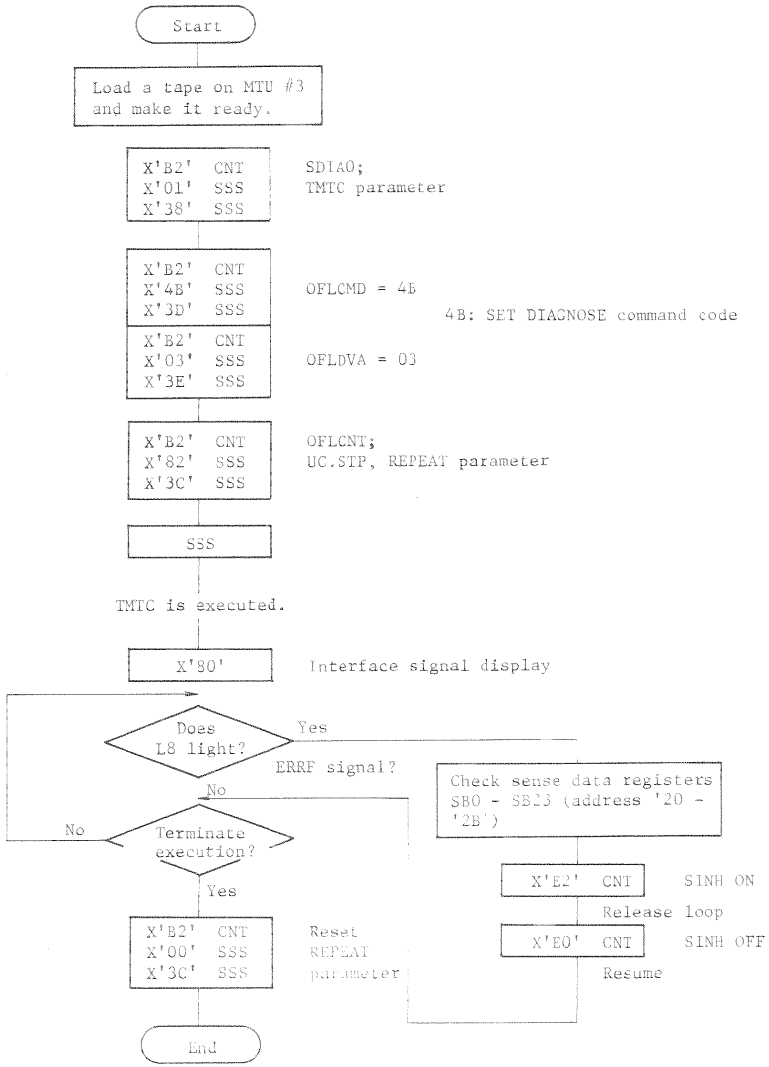
The operator of field tester can obtain the diagnostic result by checking whether ERRF (L8 at S0 ∿ S7 = '80'. See MAP M0120) is lit or DSB (address '0A').

To execute the TEST MTC, a SET DIAGNOSE command must be issued to the MTU being in the READY status.

SDIAD, bit 6 is other flag bits to direct diagnostic functions.
bits are from OLTE program.

Refer to M0111, REG ADRS '38', to each bit definitions.

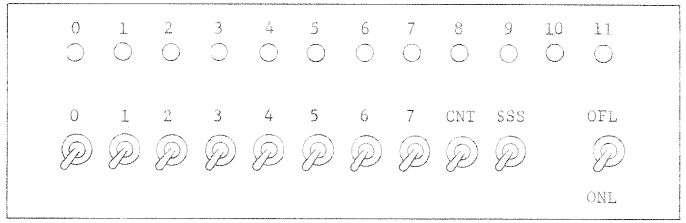
Example: TEST MTC is executed for the MTU #3. It is assumed that the execution uses REPEAT parameter and UC.STP parameter and is repeated until an error occurs.



M1000	Usage of Field Tester with MTU

The field tester is composed of LED lamps and switches, and by operating the switches, the internal signals of MTU can be displayed and the actions of MTU can be controlled (Command mode).

The field tester is connected with 1C05 on the gate part. (Lower connector of 512181U)



1. Display

The contents of the internal register file (address $00∿$1F) of MTU and the addresses of microprograms can be displayed by the following procedures.

1-1 To display the contents of register file:

(1) Set the address of register file by switches 0∿7 (one from $00 to $1F).

(2) Push CNT switch up and the contents are displayed on LED0∿7. And other LED lamps show the following;

LED8 : TMSR8 (illuminates upon detecting read data bit 8.)

LED9 : TEST (includes that the field tester is running.)

LED10: Spare (reserved for the maintenance use. It can be checked by connecting a signal with 1A05 BBV.)

LED11: UCKLP (same as the LED lamps of Unit Check on the operator panel.)

1-2 To display the address of microprogram:

(1) Set switches 0∿7 as follows;

$80 (displays the addresses continuously.)

$A0 (displays the proper address at the moment of running.)

$C0 (displays the address at the time Unit Check is generated.)

(2) Push CNT switch up and the address is displayed.

SVOK	Command	Switch 0	1	2	3	4	5	6	7	HEX	Contents
1	Forward read action	0	0	0	0	← Code →				0X	01 Forward Normal Continuous go to EOT
											02 Forward Streaming Continuous go to EOT
											07 Forward Fast go to EOT
											08 Load-Unload Repeat action
											09 Forward Normal Continuous · Rewind Repeat action
											0A Forward Streaming " "
0											0F Auto load
	Backward read action	0	1	0	0	← Code →				4X	41 Backward Normal Continuous go to EOT
											42 " Streaming " "
											47 Rewind
											49 Backward Normal Continuous · Forward Fast repeat
											4A " Streaming " "
											4F Unload
	Turn	0	Long/Short	0	1	← FWD time →	← BWD time →			1X	Short time turn
										5X	Long time turn
	Start/Stop	0	BWD/FWD	1	Long/Short	← Go up →	← Go down →			2X	Forward Start/Stop (Short time) · Rewind repeat
										3X	" (Long time) · "
										6X	Backward Start/Stop (Short time)·Forward Fast repeat
										7X	" (Long time)· "
1	Settling time of Turn and Start/Stop	Switch [4,5] [6,7]: 0 0	0 1	1 0	1 1						Mode: Short time 0 ms / 3 ms / 8 ms / 20 ms; Long time 50 ms / 150 ms / 400 ms / 1000 ms
	Write	1	0	0	0	WRT/ERS	SAGC	HD/LD	High/Low	8X	Continuous Write or Erase to EOT
	AGC or GSD	1	0	1	1	Error Stop	Sing1/Repeat	GSD/AGC	0	BX	SAGC or GSD action (Slice level is to be Normal.)
	DGC AMP	1	1	0	BWD/FWD	CN8	CN4	CN2	CN1	CX	Forward Read (Settle the gain of GCR.)
										DX	Backward Read (")
	Mode set	1	1	1	0	WRT/RD	STRMD	HD/LD	0	EX	Write/Read, Streaming/Normal, High/Low Density set
	Slice level set	1	1	1	1	0	LVLT0	LVLT1	LVLT2	FX	Set Slice level
						1	← Code →				F9 Set Slice level to 90%, FA " 100%, FB " 110%. Only GCR, PE
1/0	Photo sensor check	1	0	0	1	0	1	0	1	9X	BOT/EOT Sensor, Error Code check
						1	ERCUT	0	High/Normal		Capstan tacho pulse check of High/Normal Speed (When ERCUT is equal to 0, it stops once by error.)
	Air system action	1	0	1	0	0	AIRDV	SOLVL	PRSVL	AX	Air supply motor, Solenoid/Pressure Valve drive
						1	0	Capstan drive	BWD/FWD		For Check and Adjustment of Capacitive Sensor
0	Mechanism action	1	0	1	1	Repeat ←	← Code →			BX	B1/B9 Cartridge drive; B2/BA Auto cleaner drive; B4/BC Error marker drive; B6/BE Window drive; B7/BF Drive all of above
	Capstan circuit check	1	1	0	0	0	C	0	0	CO	D/A Converter action check
	Reel drive	1	1	0	1	Slow/Fast	BWD/FWD	MR	FR	DX	Machine and File reel drive
1/0	Reset	1	1	1	1	1	1	1	1	FF	Reset (same as Reset button of the operator panel)

2. Command Mode

Run MTU commands with the following procedures.

(1) Put MTU in offline mode.

(2) Set OFL/ONL switch of the field tester to OFL.

(3) Set a proper command on switches 0∿7. (See the Table.)

(4) Push SSS switch up. The operation starts and LED9 illuminates.

(5) The operation stops when LED9 is on if SSS switch is pushed up again.

2-1 Forward/Backward Single Motion ($0X, $4X)

During this operation, MTU enters Read status automatically.

Direction	SW0∿7 (Hex.)	Contents
Forward	01	Continuous running in Forward direction to EOT in Normal mode.
	02	Continuous running in Forward direction to EOT in Streaming mode.
	07	Continuous running in Forward direction to EOT at about 200 ips.
	08	Repeat actions of Auto load and Unload.
	09	Continuous running in Forward direction in Normal mode and Rewind upon EOT.
	0A	Continuous running in Forward direction in Streaming mode and Rewind upon EOT.
	0F	Auto load
Backward	41	Continuous running in Backward direction to BOT in Normal mode.
	42	Continuous running in Backward direction to EOT in Streaming mode.
	47	Rewind
	49	Continuous running in Backward direction in Normal mode and, upon BOT, Fast running in Forward direction.
	4A	Continuous running in Backward direction in Streaming mode and, upon BOT, Fast running in Forward direction.
	4F	Unload

2-2 Turn ($1X, $5X)

To perform bidirectional Start/Stop actions at a certain interval. The action time in Forward direction is set by SW4/5 and in Backward by SW6/7. And when SW1 is on (off), the action time is set to Long (Short). The settling time is measured from the time GAPCT (Gap Control) signal is set to 1.

SW 0	1	2	3	4	5	6	7
0	1:Long 0:Short	0	1	Forward time (Below table)		Backward time (Below table)	

SW 4,5 / 6,7 / Mode	0 0	0 1	1 0	1 1
Short	0 ms	3 ms	8 ms	20 ms
Long	50 ms	150 ms	400 ms	1000 ms

2-3 Start/Stop ($2X, $3X, $6X, $7X)

To perform Start/Stop actions in one direction at a certain interval.
The direction (forward/backward) is specified by SW1.
The action time (Short/Long) is specified by SW3.
The go-time is set by SW4/5 and Stop time by SW6/7.
The settling time is the same as shown at 2-2 Turn.

SW 0	1	2	3	4	5	6	7
0	1:Backward 0:Forward	1	1:Long 0:Short	Go time		Stop time	

In case of Block write, perform the command $2X or $3X after Mode setting (Refer to 2-7 Mode set).

2-4 Write action ($8X)

To write or erase to EOT with continuous running.

By SW4, whether to write or to erase is specified.

By SW5, whether SAGC is on or off at writing GCR is specified.

By SW6, whether High Density or Low Density is specified.

By SW7, write density is specified under each density mode.

SW							
0	1	2	3	4	5	6	7
1	0	0	0	1:Write	1:SAGC ON	1:High Density	1:High
				0:Erase	0:SAGC OFF	0:Low Density	0:Low

Record density / SW7	6250	1600	800
0: Low	3014 fci	1600 fci	200 fci
1: High	9042 fci	3200 fci	800 fci

2-5 AGC/GSD action ($BX)

To perform the actions of SAGC (Self Adjust Gain Control) and GSD (Gain Step Down after 1 Block Read/Write) at a proper interval when a magnetic tape written continuously with 9042 runs.

By SW4, whether to stop at the error or not is specified.

By SW5, whether Single or Repeat is specified.

By SW6, whether SAGC action or GSD one is specified.

Slice level is to be Normal.

SW							
0	1	2	3	4	5	6	7
1	0	1	1	1:Error Stop	1:Single	1:GSD	0
				0:Non Stop	0:Repeat	0:SAGC	

2-6 DGC AMP action ($CX, $DX)

To set count value of DGC AMP to any one in GCR mode.

By SW3, whether Forward or Backward is specified.

By SW4∿7, the count value is specified in hexadecimal notation.

SW							
0	1	2	3	4	5	6	7
1	1	0	1:Backward / 0:Forward	Count 8	Count 4	Count 2	Count 1

2-7 Mode set ($EX)

To set each mode of MTU.

By SW4, whether Write or Read mode is specified.

By SW5, whether Streaming or Normal mode is specified.

By SW6, whether High Density or Low Density is specified.

SW							
0	1	2	3	4	5	6	7
1	1	1	0	1:Write 0:Read	1:Streaming 0:Normal	1: High Density 0: Low Density	0

2-8 Slice level set ($FX)

To specify Slice level to any one.

SW							
0	1	2	3	4	5	6	7
1	1	1	1	0	LVLT0	LVLT1	LVLT2

To specify Slice level by the conbination of bit 5, 6, and 7.

Purpose	Level test	READ		WRITE	Methode
	0 1 2	FWD	BWD	FWD	
Diagnosis	1 1 1	125 ± 12%			GCR/PE
	1 1 0	100 ± 12%			
	1 0 1	80 ± 8%			
	1 0 0	64 ± 8%			
	0 1 1	51 ± 5%			
	0 1 0	41 ± 5%			
Marginal	0 0 1	15 ± 2%	10 ± 1% 15 (Note 1)	37 ± 4%	
Normal	0 0 0	10 ± 1%	7 ± 1% 10 (Note 1)	20 ± 2% 25 (Note 1)	
Marginal	X X 1	26 ± 4%		50 ± 5%	NRZI
Normal	X X 0	17 ± 2%		40 ± 5%	

For the adjustment of Read Amplifier, Slice levels of 90%, 100% and 110% are provided. And at each Slice level, it can be adjusted by observing the signals of TMSR0 ∿ 8 (To select $1E as a register address in Display mode).

SW0 ∿ 7 (Hex.)	Contents
F9	To set Slice level to 90% at the adjustment of the level.
FA	To set Slice level to 100% at the adjustment of the level.
FB	To set Slice level to 110% at the adjustment of the level.

Note 1: 512182U; AGC8 or more

512649U; AGCC or more

2-9 Photo sensor check ($9X)

To check BOT, EOT, error code indicator and capstan tachometer A/B. When checking the capstan tachometer, the motor can be rotated with insecure speed by setting SW5 on even if the error of a tachometer is detected.

SW0∿7 (Hex.)	Contents
95	To be used for check and adjustment of BOT/EOT and for check of error code indicator. BOT and EOT signals are output at bits 4 and 5 of address $14 of jump condition As for displaying error codes, the code is changing as follows; 00 → 11 → 22 ..... 99 → → 00
98 (9C)	To check duty and phase of the capstan tachometer. If an error is found, it is shown with an error code. In the case of error, setting SW0∿7 to $9C makes the motor rotate with fixed voltage.
99 (9D)	To check the capstan tachometer in high speed rotation. If an error is found, it is shown with an error code. In the case of error, setting SW0∿7 to $9D makes the motor rotate with fixed voltage.

2-10 Air System action ($AX)

To check and adjust the air system by activating air supply motor and valve.

SW							
0	1	2	3	4	5	6	7
1	0	1	0	0	1: Air Drive	1: Solenoid Valve Drive	1: Solenoid Valve Drive
					0: Off	0: Off	0: Off

It is also performed for the check and adjustment of the capacitive sensor.

SW							
0	1	2	3	4	5	6	7
1	0	1	0	1	0	1: Capstan Drive	1: Backward
						0: Coast	0: Forward

Note in the check and adjustment of the capacitive sensor:

(1) Set SW0∿7 to $A8, stop the tape loop at the center of each column sensor, and fix the reel.

(2) Then, set SW0∿7 to $AA or $AB, check it by moving tape loops.

M1005	Field Tester Function (5)

2-11 Mechanism action ($BX)

To perform the actions of Cartridge, Auto Cleaner, Error Marker and Window.

These actions can be performed once (SW4 off) or repeatedly (SW4 on).

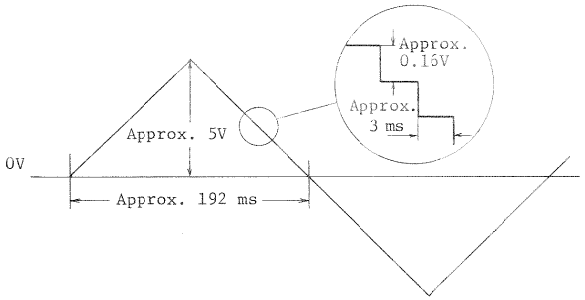
SW0∿7 (Hex.)	Contents
B1	To open Cartridge
B9	To repeat open and close of Cartridge
B2	To drive Auto Cleaner
BA	To repeat on and off of Auto Cleaner
B4	To drive Error Marker
BC	To repeat on and off of Error Marker
B6	To close Window
BE	To repeat open and close of Window
B7	To open Cartridge, to drive Auto Cleaner and Error Marker and to close Window
BF	To repeat above open and close or on and off

2-12 Capstan Circuit check ($C0)

To confirm the action of capstan drive circuit by checking DAC (D/A Converter).

Set SW0∿7 to $C0 and check DAC.

If DAC signal is a stepped waveform shown as below, the action is normal.



The measuring position is a check terminal, DAC, of 1A04 TKBM.

2-13 Reel Drive ($DX)

To confirm the action of Reel motor drive circuit by rotating Reel motor clockwise or counterclockwise with the servomechanism turned off.

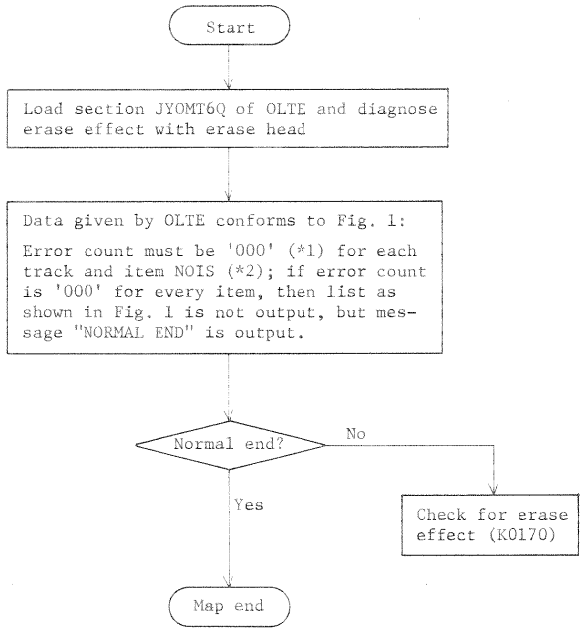
By SW4, Slow or Fast is specified.

By SW5, Forward or Backward is specified.

SW6 specifies Machine reel tc be drived and SW6 File reel.

SW							
0	1	2	3	4	5	6	7
1	1	0	1	1: Slow	1: Counter-clockwise	1: Machine Reel Drive	1: File Reel Drive
				0: Fast	0: Clockwise	0: Stop	0: Stop

TST6200	Diagnosis of Erase Effect [JYOMT6Q]



Note: Refer to section JYOMT6Q in the OLTE diagnostic manual for output formats and detailed diagnosis.

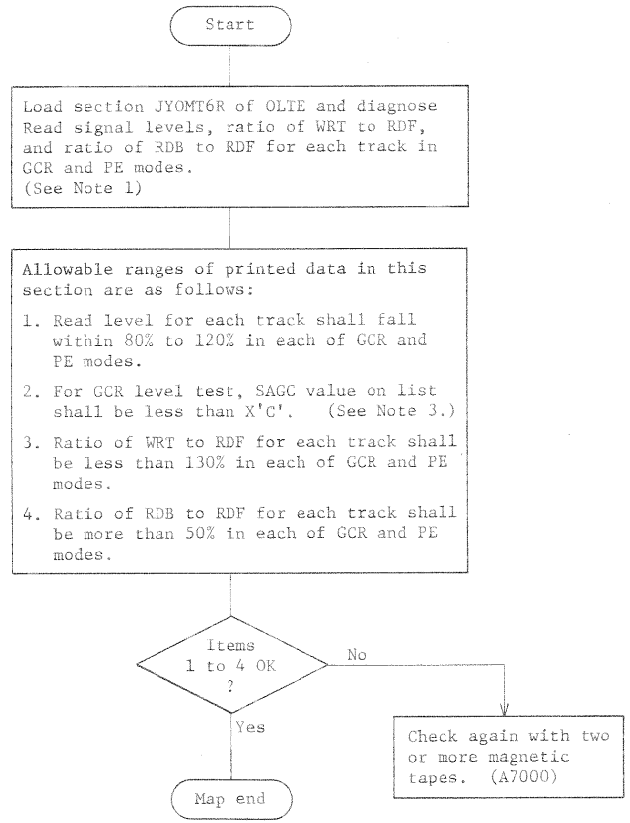
```
.....................(SL=00001, TL=001).....................
JYOMT6Q  V-02  RTN  01  DEV  0583  LEV  00  REF  NO  0

ERASE CHECK

ERASE CHECK          SLICE LEVEL = 10%

 TRK BIT ERROR COUNT (100 SAMPLE)

   1   5    000
   2   7    000
   3   3    000
   4   P    003
   5   2    000    (*1)
   6   1    000
   7   0    000
   8   6    000
   9   4    000
   NOIS     000    (*2)

REFER TST6200 IN MAINTENANCE MANUAL
```

Fig. 1 Example of printed data

```
HEU023I  S JYOMT6Q  DEV 01E0 13.44.37
NORMAL END
NORMAL END
HEU024I  T JYOMT6Q  DEV 01E0 13.45.12
```

Fig. 2 Example of printed data when no errors are counted

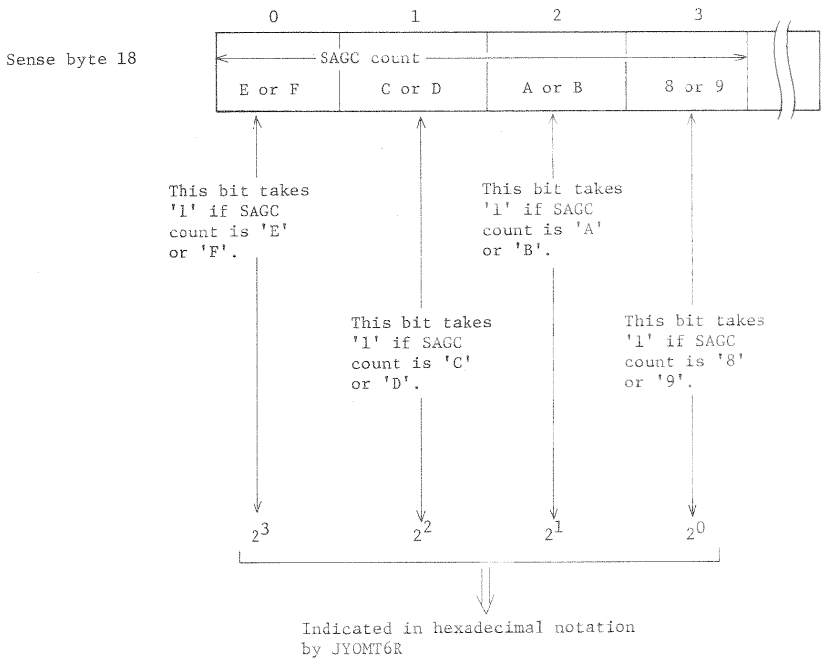
TST6210	Diagnosis of Read Signal Level [JYOMT6R]



Note 1: WRT: Write and Read
RDF: Read FWD
RDB: Read BWD

Note 2: Refer to section JYOMT6R in the OLTE diagnostic manual for output formats and detailed diagnosis.

Note 3: The SAGC count (bits 0 to 3 of MTU sense byte 5) is indicated at bits 0 to 3 of MTC sense byte 18.
The correspondence between the SAGC value in data to be printed out from JYOMT6R and the SAGC count indicated at bits 0 to 3 of MTU sense byte 5 is as follows:



- If the media and head take standard values, then the SAGC count of the MTU is '5' or '6'. Therefore, the SAGC value of printed data for JYOMT6 is '00'.
- The gain difference between two steps of the SAGC count of the MTU is about 20%.

TST6211	JYOMT6R Printed Out Data Example - 1

```
 JYOMT6R   V-01 L-00  RTN 01  DEV/LN 01E0  REFNO 0
WRITE,READ SLICE LEVEL CHECK

  WRITE SLICE LEVEL

        MTU SPEED   MODE = NORMAL
        MTU DENSITY MODE = GCR          SAGC = 00
                                          1    1    1    1    1    1
  TRK BIT  4    5    6    7    8    9    0    1    2    3    4    5
           0    0    0    0    0    0    0    0    0    0    0    0  (%)
   1   5   XXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
   2   7   XXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
   3   3   XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
   4   P   XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
   5   2   XXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
   6   1   XXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
   7   0   XXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
   8   6   XXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
   9   4   XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX

REFER TST6210 IN MAINTENANCE MANUAL
```

```
 JYOMT6R   V-01 L-00  RTN 01  DEV/LN 01E0  REFNO 0
WRITE,READ SLICE LEVEL CHECK

  READ  FORWARD SLICE LEVEL

        MTU SPEED   MODE = NORMAL
        MTU DENSITY MODE = PE
                                          1    1    1    1    1    1
  TRK BIT  4    5    6    7    8    9    0    1    2    3    4    5
           0    0    0    0    0    0    0    0    0    0    0    0  (%)
   1   5   XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
   2   7   XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
   3   3   XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
   4   P   XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
   5   2   XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
   6   1   XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
   7   0   XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
   8   6   XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
   9   4   XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX

REFER TST6210 IN MAINTENANCE MANUAL
```

The slice level for each of high/normal speed mode, GCR mode, and PE mode must fall within the following range:

$$80\% < \text{Slice level} < 120\%$$

TST6212	JYOMT6R Printed Out Data Example - 2

```
 JYOMT6R   V-01 L-00  RTN 01  DEV/LN 01E0  REFNO 0
WRITE,READ SLICE LEVEL CHECK

  WRITE/READ FORWARD LEVEL RATIO

        MTU SPEED   MODE = NORMAL
        MTU DENSITY MODE = GCR          SAGC = 00
                                        1   1   1   1   1   1
  TRK BIT  4   5   6   7   8   9   0   1   2   3   4   5
           0   0   0   0   0   0   0   0   0   0   0   0  (%)
   1   5   XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
   2   7   XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
   3   3   XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
   4   P   XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
   5   2   XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
   6   1   XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
   7   0   XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
   8   6   XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
   9   4   XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX

REFER TST6210 IN MAINTENANCE MANUAL
```

The WRT/RDF level ratio must be less than 130%.

```
 JYOMT6R   V-01 L-00  RTN 01  DEV/LN 01E0  REFNO 0
WRITE,READ SLICE LEVEL CHECK

  WRITE/READ FORWARD LEVEL RATIO

        MTU SPEED   MODE = HIGH
        MTU DENSITY MODE = PE
                                        1   1   1   1   1   1
  TRK BIT  4   5   6   7   8   9   0   1   2   3   4   5
           0   0   0   0   0   0   0   0   0   0   0   0  (%)
   1   5   XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
   2   7   XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
   3   3   XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
   4   P   XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
   5   2   XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
   6   1   XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
   7   0   XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
   8   6   XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
   9   4   XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX

REFER TST6210 IN MAINTENANCE MANUAL
```

TST6213	JYOMT6R Printed Out Data Example - 3

```
 JYOMT6R   V-01 L-00  RTN 01  DEV/LN 01E0  REFNO 0
WRITE,READ SLICE LEVEL CHECK

  READ BACKWARD/READ FORWARD LEVEL RATIO

         MTU SPEED   MODE = NORMAL
         MTU DENSITY MODE = PE
                                          1   1   1   1   1   1
  TRK BIT  4   5   6   7   8   9   0   1   2   3   4   5
           0   0   0   0   0   0   0   0   0   0   0   0  (%)
   1   5   XXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
   2   7   XXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
   3   3   XXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
   4   P   XXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
   5   2   XXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
   6   1   XXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
   7   0   XXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
   8   6   XXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
   9   4   XXXXXXXXXXXXXXXXXXXXXXXXXXXXXX

REFER TST6210 IN MAINTENANCE MANUAL
```

```
 JYOMT6R   V-01 L-00  RTN 01  DEV/LN 01E0  REFNO 0
WRITE,READ SLICE LEVEL CHECK

  READ BACKWARD/READ FORWARD LEVEL RATIO

         MTU SPEED   MODE = HIGH
         MTU DENSITY MODE = GCR         SAGC = 00
                                          1   1   1   1   1   1
  TRK BIT  4   5   6   7   8   9   0   1   2   3   4   5
           0   0   0   0   0   0   0   0   0   0   0   0  (%)
   1   5   XXXXXXXXXXXXXXXXXX
   2   7   XXXXXXXXXXXXXXXXXX
   3   3   XXXXXXXXXXXXXXXXXX
   4   P   XXXXXXXXXXXXXXXXXX
   5   2   XXXXXXXXXXXXXXXXXX
   6   1   XXXXXXXXXXXXXXXXXX
   7   0   XXXXXXXXXXXXXXXXXX
   8   6   XXXXXXXXXXXXXXXXXX
   9   4   XXXXXXXXXXXXXXXXXX

REFER TST6210 IN MAINTENANCE MANUAL
```

The RDB/RDF level ratio must be more than 50%.

TST6220	Diagnosis of Capstan Normal Start/Stop, Tape Speed

- Each of sections JYOMT6T, -U, and -V measures the capstan characteristics of an aiming MTU and outputs the results in the form of tables.

  They can print out the characteristics of the capstan in the form of graphs as well, though in this case the volume of lists printed may increase considerably.

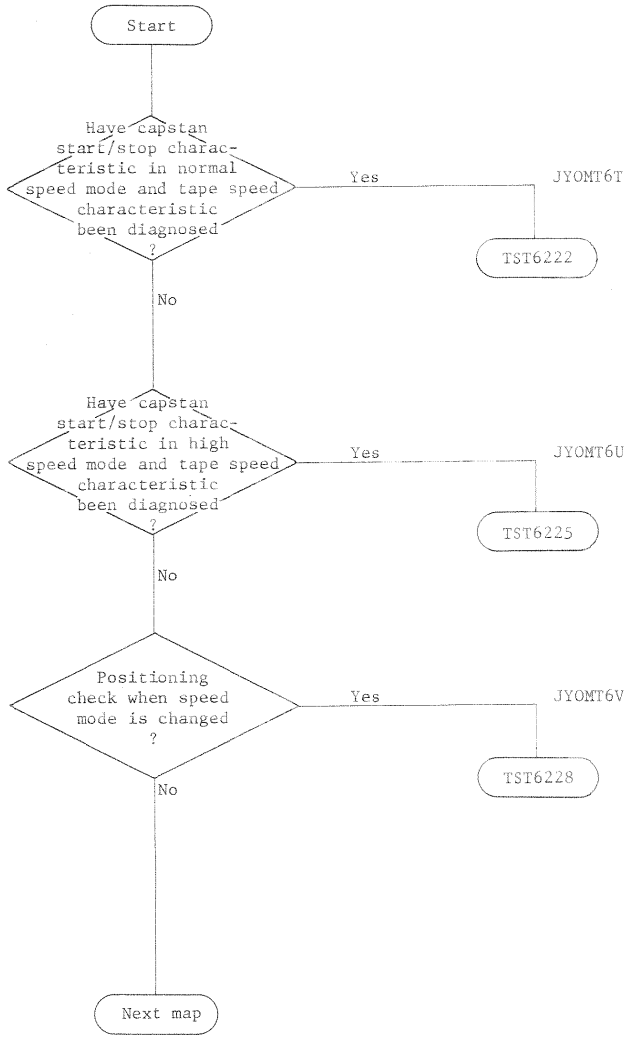
  For details on how to specify parameters, refer to OLTE manuals.

  These sections do not evaluate the results of measurement. So, the maintenance man should examine the values of lists output; judge their validity and the extent of degradation; take remedial actions.

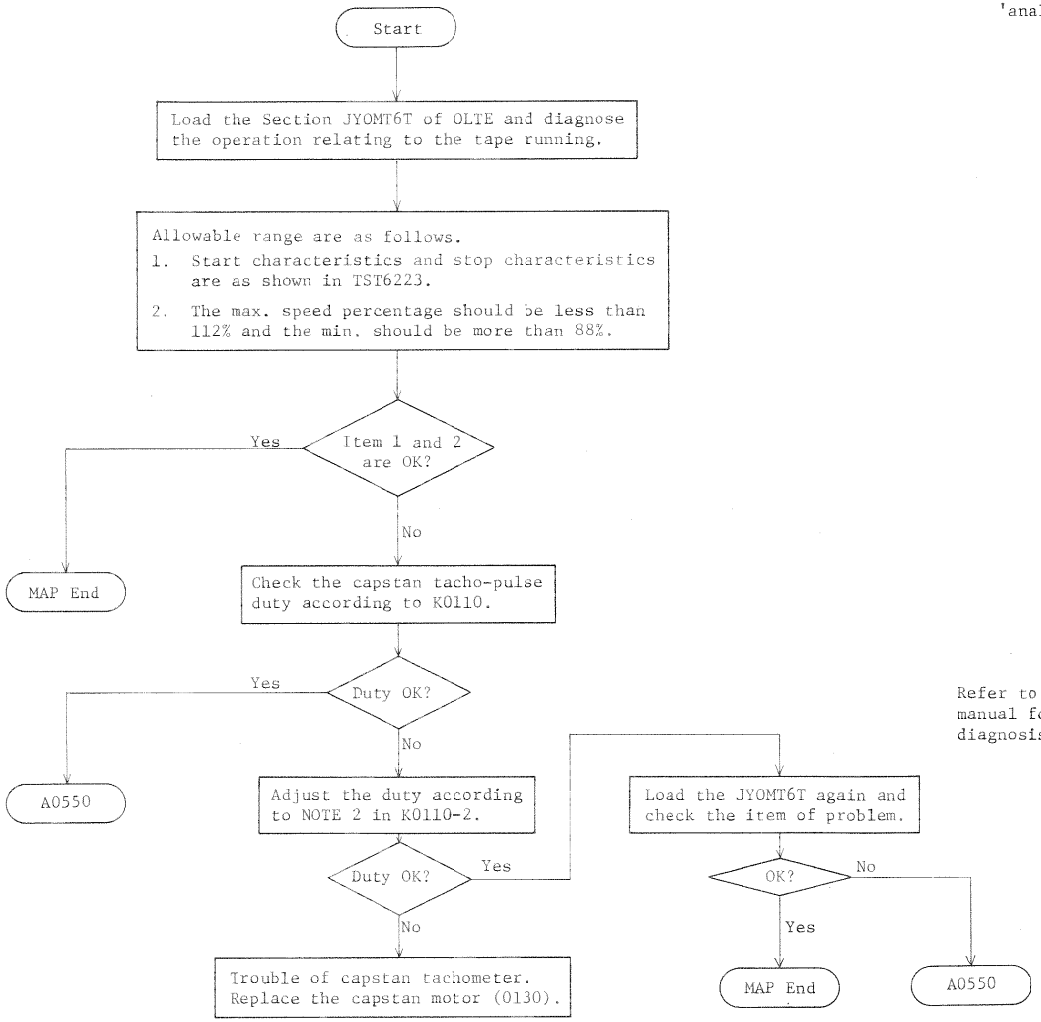
  Maps TST5221 to TST6229 show the criterions of the above judgement.

  If an error or unusual measurement data occurs during running these sections of OLTE, then error messages may be output so that no results of measurement are printed out.

  In such cases, most possible errors are due to execution of commands for diagnosis, which do not immediately affect usual read/write operation. Nevertheless, for close maintenance of the MTU/MTC functions, the maintenance man should follow up the cause of the error by examining error messages, determining the CCW data address, dumping measurement data, checking on the MTU for status, and performing other function tests.



TST6222	Diagnosis of Capstan Normal Start/Stop Characteristics and Tape Speed [JYOMT6T]



Note: To view start/stop characteristics with a scope, put input 'A' probe on 'analog +' of read amplifier and trigger on 'ACT' (1A05 BE7).

Refer to section JYOMT6T in OLTE diagnostic manual for output formats and detailed diagnosis.

TST6223	JYOMT6T Output

JYOMT6T V-01 L-00 RTN 01 DEV/LN 0780 REFNO 0
CAPSTAN NORMAL START/STOP, TAPE SPEED CHECK

<< CAPSTAN CHARACTERISTIC TEST >>

MTU SPEED MODE = NORMAL
MTU DENSITY MODE = GCR

TEST MODE	LAST MT STATUS	BLOCK	START TIME(MS)	START FTP	VELOCITY 125 IPS=100% MINIMUM	AVERAGE	MAXIMUM	STOP TIME(MS)	STOP FTP
WRT	WRT	1	1.2^{max}	10^{max}	118 IPS (094%)	124 IPS (099%)	126 IPS (100%)	4.0^{max}	25^{max}
RDB	RDB	1	4.0^{max}	25^{max}	125 IPS (100%)	126 IPS (100%)	126 IPS (100%)	2.2^{max}	17^{max}
RDB	RDB	2	"	"	125 IPS (100%)	125 IPS (100%)	126 IPS (100%)	"	"
RDB	RDB	3	"	"	125 IPS (100%)	125 IPS (100%)	126 IPS (100%)	"	"
RDB	RDF	1	4.0^{max}	25^{max}	125 IPS (100%)	125 IPS (100%)	126 IPS (100%)	2.2^{max}	17^{max}
RDB	RDF	2	"	"	125 IPS (100%)	126 IPS (100%)	126 IPS (100%)	"	"
RDB	RDF	3	"	"	125 IPS (100%)	126 IPS (100%)	126 IPS (100%)	"	"
RDF	RDF	1	1.2^{max}	10^{max}	124 IPS (099%)	124 IPS (099%)	125 IPS (100%)	4.0^{max}	25^{max}
RDF	RDF	2	"	"	122 IPS (097%)	124 IPS (099%)	126 IPS (100%)	"	"
RDF	RDF	3	"	"	123 IPS (098%)	124 IPS (099%)	125 IPS (100%)	"	"
RDF	RDB	1	1.2^{max}	10^{max}	124 IPS (099%)	125 IPS (100%)	126 IPS (100%)	4.0^{max}	25^{max}
RDF	RDB	2	"	"	123 IPS (098%)	125 IPS (100%)	126 IPS (100%)	"	"
RDF	RDB	3	"	"	124 IPS (099%)	125 IPS (100%)	125 IPS (100%)	"	"

REFER TST6220 IN MAINTENANCE MANUAL

Should be 88% ∿ 112%.

JYOMT6T V-01 L-00 RTN 01 DEV/LN 0780 REFNO 0
CAPSTAN NORMAL START/STOP, TAPE SPEED CHECK

<< CAPSTAN CHARACTERISTIC TEST >>

MTU SPEED MODE = NORMAL
MTU DENSITY MODE = PE

TEST MODE	LAST MT STATUS	BLOCK	START TIME(MS)	START FTP	VELOCITY 125 IPS=100% MINIMUM	AVERAGE	MAXIMUM	STOP TIME(MS)	STOP FTP
WRT	WRT	1	1.2^{max}	10^{max}	118 IPS (094%)	124 IPS (099%)	126 IPS (100%)	4.6^{max}	35^{max}
RDB	RDB	1	4.0^{max}	25^{max}	124 IPS (099%)	125 IPS (100%)	127 IPS (101%)	4.6^{max}	35^{max}
RDB	RDB	2	"	"	125 IPS (100%)	126 IPS (100%)	126 IPS (100%)	"	"
RDB	RDB	3	"	"	126 IPS (100%)	126 IPS (100%)	126 IPS (100%)	"	"
RDB	RDF	1	4.0^{max}	25^{max}	125 IPS (100%)	126 IPS (100%)	126 IPS (100%)	4.6^{max}	35^{max}
RDB	RDF	2	"	"	125 IPS (100%)	125 IPS (100%)	126 IPS (100%)	"	"
RDB	RDF	3	"	"	124 IPS (099%)	125 IPS (100%)	127 IPS (101%)	"	"
RDF	RDF	1	1.2^{max}	10^{max}	124 IPS (099%)	124 IPS (099%)	125 IPS (100%)	5.0^{max}	44^{max}
RDF	RDF	2	"	"	123 IPS (098%)	124 IPS (099%)	125 IPS (100%)	"	"
RDF	RDF	3	"	"	123 IPS (098%)	124 IPS (099%)	125 IPS (100%)	"	"
RDF	RDB	1	1.2^{max}	10^{max}	123 IPS (098%)	124 IPS (099%)	125 IPS (100%)	5.0^{max}	44^{max}
RDF	RDB	2	"	"	124 IPS (099%)	125 IPS (100%)	125 IPS (100%)	"	"
RDF	RDB	3	"	"	125 IPS (100%)	125 IPS (100%)	125 IPS (100%)	"	"

REFER TST6220 IN MAINTENANCE MANUAL

Should be 88% ∿ 112%.

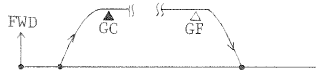
TST6224	JYOMT6T Graphic Option

When JYOMT6T runs, if characteristic graphs are output with specifying graphic option, the outlines of the graphs are to be as follows.

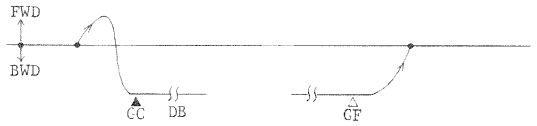
Each measurement condition is shown with the following format.

(Test mode ← Last-MT-status, density, speed mode)

(1) (WRT ← WRT, GCR, Normal)



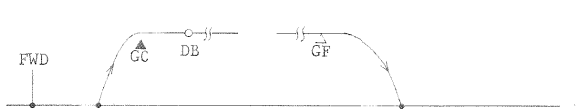
(2) (RDB ← RDB, GCR, Normal)



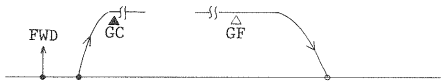
(3) (RDB ← RDF, GCR, Normal)

(4) (RDF ← RDF, GCR, Normal)

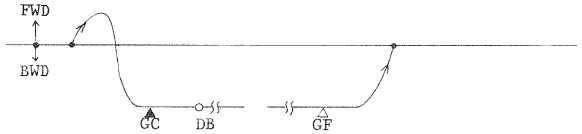
(5) (RDF ← RDB, GCR, Normal)



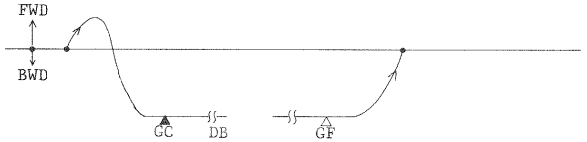
(6) (WRT ← WRT, PE, Normal)



(7) (RDB ← RDB, PE, Normal)



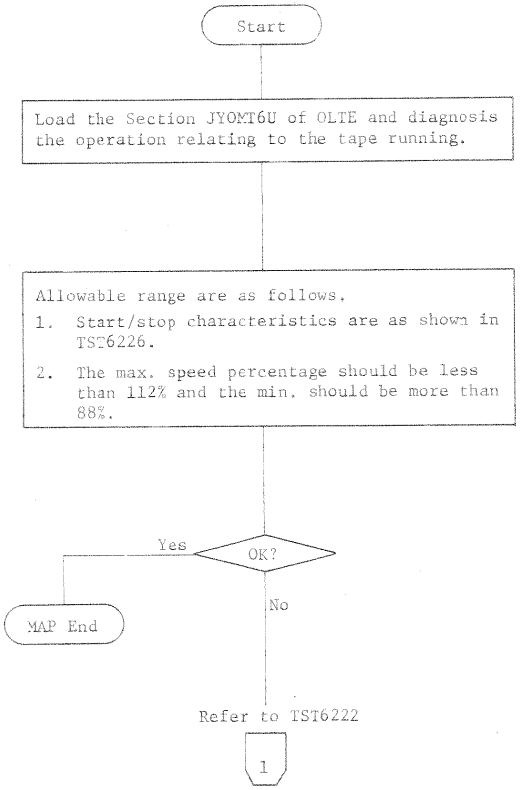
(8) (RDB ← RDF, PE, Normal)



(9) (RDF ← RDF, PE, Normal)

(10) (RDF ← RDB, PE, Normal)

TST6225	Diagnosis of Capstan High Start/Stop Characteristics and Tape Speed [JYOMT6U]



TST6226	JYOMT6U Output

JYOMT6U V-01 L-00 RTN 01 DEV/LN 0780 REFNO 0
CAPSTAN HIGH START/STOP, TAPE SPEED CHECK

<< CAPSTAN CHARACTERISTIC TEST >>

MTU SPEED MODE = HIGH
MTU DENSITY MODE = GCR

TEST MODE	LAST MT STATUS	BLOCK	START TIME(MS)	FTP	VELOCITY MINIMUM	125 IPS=100% AVERAGE	MAXIMUM	STOP TIME(MS)	FTP
WRT	WRT	1	6.4max	54max	199 IPS (099%)	200 IPS (100%)	202 IPS (101%)	24.0max	250max
WRT	RDF	2	24.0max	254max	199 IPS (099%)	200 IPS (100%)	201 IPS (100%)	"	"
WRT	RDB	3	24.0max	254max	199 IPS (099%)	200 IPS (100%)	201 IPS (100%)	"	"
RDB	RDB	1	15.0max	127max	200 IPS (100%)	202 IPS (101%)	204 IPS (102%)	7.8max	78max
RDB	RDB	2	"	"	200 IPS (100%)	202 IPS (101%)	203 IPS (101%)	"	"
RDB	RDB	3	"	"	201 IPS (100%)	201 IPS (100%)	202 IPS (101%)	"	"
RDB	RDF	1	15.0max	127max	202 IPS (101%)	202 IPS (101%)	203 IPS (101%)	7.8max	78max
RDB	RDF	2	"	"	201 IPS (100%)	202 IPS (101%)	204 IPS (102%)	"	"
RDB	RDF	3	"	"	201 IPS (100%)	203 IPS (101%)	204 IPS (102%)	"	"
RDF	RDF	1	7max	58max	199 IPS (099%)	199 IPS (099%)	200 IPS (100%)	18.0max	166max
RDF	RDF	2	"	"	200 IPS (100%)	200 IPS (100%)	201 IPS (100%)	"	"
RDF	RDF	3	"	"	200 IPS (100%)	200 IPS (100%)	201 IPS (100%)	"	"
RDF	RDB	1	7max	58max	200 IPS (100%)	200 IPS (100%)	201 IPS (100%)	18.0max	166max
RDF	RDB	2	"	"	200 IPS (100%)	200 IPS (100%)	201 IPS (100%)	"	"
RDF	RDB	3	"	"	200 IPS (100%)	200 IPS (100%)	200 IPS (100%)	"	"

REFER TST6220 IN MAINTENANCE MANUAL

Should be 88% ∿ 112%.

JYOMT6U V-01 L-00 RTN 01 DEV/LN 0780 REFNO 0
CAPSTAN HIGH START/STOP, TAPE SPEED CHECK

<< CAPSTAN CHARACTERISTIC TEST >>

MTU SPEED MODE = HIGH
MTU DENSITY MODE = PE

TEST MODE	LAST MT STATUS	BLOCK	START TIME(MS)	FTP	VELOCITY MINIMUM	125 IPS=100% AVERAGE	MAXIMUM	STOP TIME(MS)	FTP
WRT	WRT	1	6.4max	54max	197 IPS (098%)	200 IPS (100%)	201 IPS (100%)	26.0max	282max
WRT	RDF	2	24.0max	270max	199 IPS (099%)	200 IPS (100%)	201 IPS (100%)	"	"
WRT	RDB	3	"	"	199 IPS (099%)	200 IPS (100%)	202 IPS (101%)	"	"
RDB	RDB	1	15.0max	127max	202 IPS (101%)	203 IPS (101%)	204 IPS (102%)	7.8max	78max
RDB	RDB	2	"	"	203 IPS (101%)	203 IPS (101%)	204 IPS (102%)	"	"
RDB	RDB	3	"	"	203 IPS (101%)	204 IPS (102%)	204 IPS (102%)	"	"
RDB	RDF	1	15.0max	127max	204 IPS (102%)	204 IPS (102%)	204 IPS (102%)	7.8max	78max
RDB	RDF	2	"	"	203 IPS (101%)	204 IPS (102%)	204 IPS (102%)	"	"
RDB	RDF	3	"	"	202 IPS (101%)	203 IPS (101%)	204 IPS (102%)	"	"
RDF	RDF	1	6.8max	56max	199 IPS (099%)	200 IPS (100%)	200 IPS (100%)	18.0max	197max
RDF	RDF	2	"	"	199 IPS (099%)	201 IPS (100%)	202 IPS (101%)	"	"
RDF	RDF	3	"	"	199 IPS (099%)	200 IPS (100%)	201 IPS (100%)	"	"
RDF	RDB	1	6.8max	56max	199 IPS (099%)	200 IPS (100%)	201 IPS (100%)	18.0max	197max
RDF	RDB	2	"	"	200 IPS (100%)	200 IPS (100%)	201 IPS (100%)	"	"
RDF	RDB	3	"	"	200 IPS (100%)	201 IPS (100%)	202 IPS (101%)	"	"

REFER TEST6220 IN MAINTENANCE MANUAL

Should be 88% ∿ 112%.

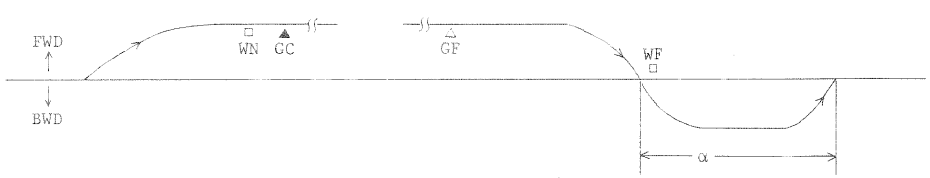
TST6227	JYOMT6U Graphic Option

When JYOMT6U runs, if characteristic graphs are output with specifying graphic option, the outlines of the graphs are to be as follows.

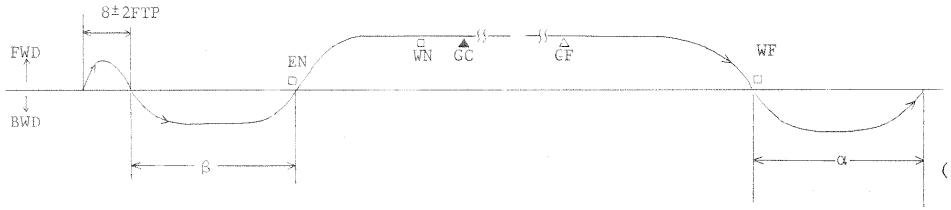
Each measurement condition is shown with the following format.

(Test mode ← Last MT status, density, speed mode)

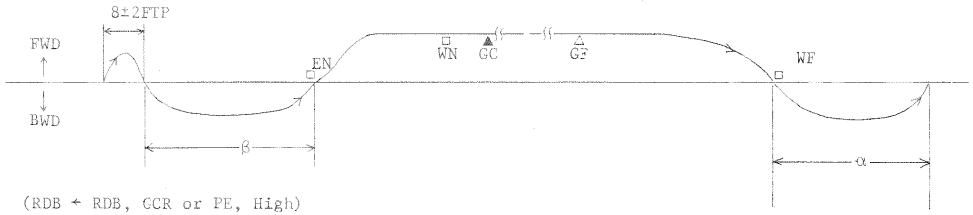
(1) (WRT ← WRT, GCR or PE, High)



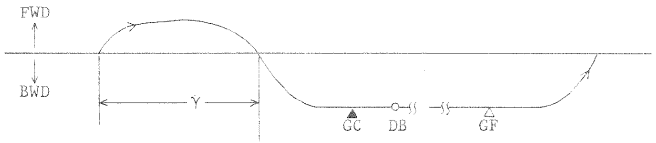
(2) (WRT ← RDF, GCR or PE, High)



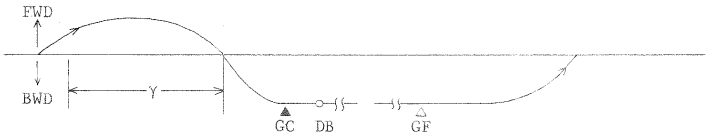
(3) (WRT ← RDB, GCR or PE, High)



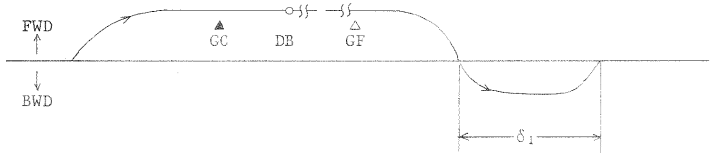
(4) (RDB ← RDB, GCR or PE, High)



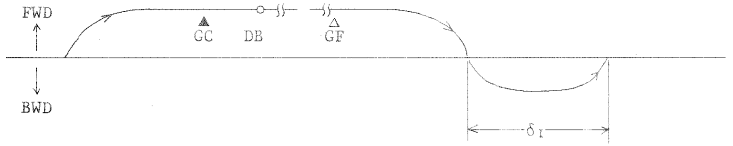
(5) (RDB ← RDF, GCR or PE, High)



(6) (RDF ← RDF, GCR or PE, High)



(7) (RDF ← RDB, GCR or PE, High)



α = { 138±5 FTP ... GCR ; 138±5 FTP ... PE }

β = { 90±5 FTP ... GCR ; 107±5 FTP ... PE }

γ = { 80±5 FTP ... GCR ; 80±5 FTP ... PE }

δ_1 = { 96±5 FTP ... GCR ; 96±5 FTP ... PE }

TST6228	Diagnosis of Capstan Positioning Characteristics Changing Speed Mode [JYOMT6V]

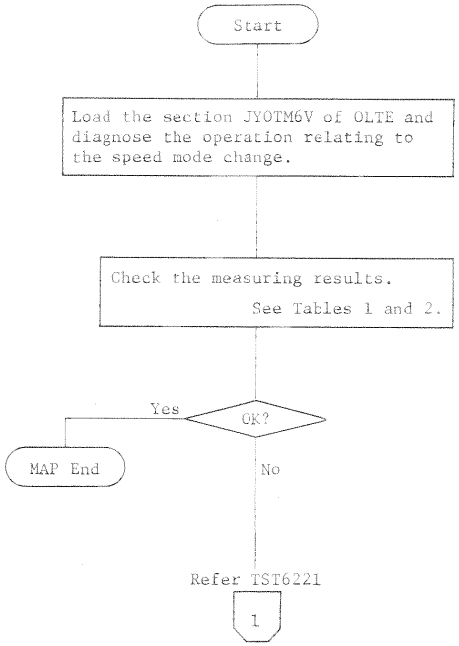


Table 1

JYOMT6V V-01 L-00 RTN 01 DEV/LN 0780 REFNO 0
CHANGE SPEED CAPSTAN POSITIONING CHECK

<< CAPSTAN CHARACTERISTIC TEST >>

MTU DENSITY MODE = GCR

TEST MODE	LAST MT STATUS	POSITIONING TIME(MS)	FTP
NORMAL SPEED	WRT	30.0 max	234±5
	RDB	10.0 max	56±5
	RDF	10.0 max	70±5
HIGH SPEED	WRT	10.0 max	70 5
	RDB	10.0 max	70±5
	RDF	10.0 max	57±5

REFER TST6220 IN MAINTENANCE MANUAL

Table 2

JYOMT6V V-01 L-00 RTN 01 DEV/LN 0780 REFNO 0
CHANGE SPEED CAPSTAN POSITIONING CHECK

<< CAPSTAN CHARACTERISTIC TEST >>

MTU DENSITY MODE = PE

TEST MODE	LAST MT STATUS	POSITIONING TIME(MS)	FTP
NORMAL SPEED	WRT	30.0 max	241±5
	RDB	10.0 max	37±5
	RDF	10.0 max	59±5
HIGH SPEED	WRT	10.0 max	36±5
	RDB	10.0 max	52±5
	RDF	10.0 max	45±5

REFER TST6220 IN MAINTENANCE MANUAL

TST6229	JYOMT6V Graphic Option

When JYOMT6V runs, if characteristic graphs are output with specifying graphic option, the outlines of the graphs are to be as follows.

Each measurement condition is shown with the following format.

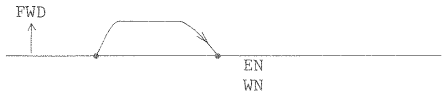
(Last MT status, test speed mode ← Last speed mode)

(1) (WRT, HSP ← NSP)

(2) (RDF, HSP ← NSP)

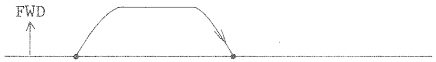
(3) (RDB, HSP ← NSP)

(4) (WRT, NSP ← HSP)



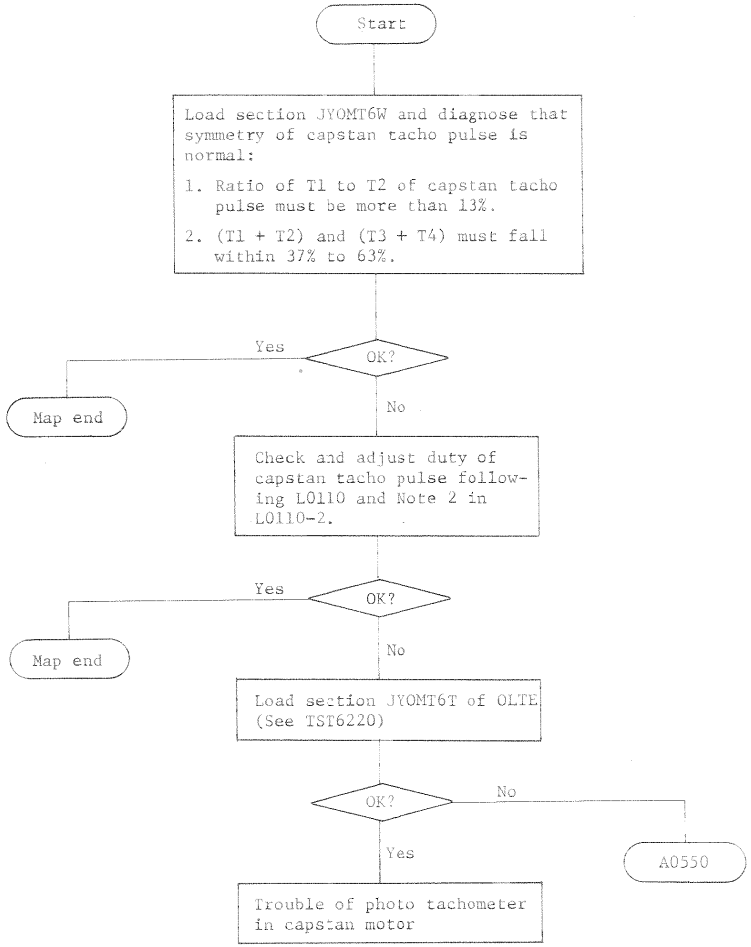
(5) (RDF, NSP ← HSP)

(6) (RDB, NSP ← HSP)



HSP: High speed
NSP: Normal speed

TST6230	Diagnosis of a Symmetry of Capstan Tacho Pulse [JYOMT6W]

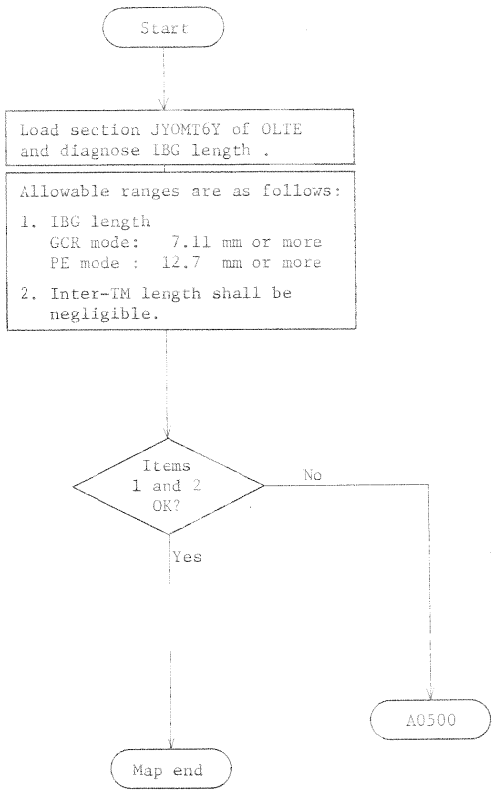


Note: Refer to section JYOMT6W in the OLTE diagnostic manual for output formats and detailed diagnosis.

```
A06   JYOMT6W   V-01 L-00  RTN 01  DEV/LN 01E0  REFNO 0
A06  CAPSTAN ASMMETRY CHECK
A06
A06   TACHO PULSE ASYMMETRY CHECK
A06
A06                 MTU SPEED   MODE = NORMAL
A06                 MTU DENSITY MODE = PE
A06
A06                MIN      AVG      MAX
A06
A06     T1       23.32    25.97    28.78    (%)
A06             912.00   976.25   568.00    (MM)
A06
A06     T2       21.24    24.23    26.13    (%)
A06             208.00   833.85   240.00    (MM)
A06
A06     T3       24.28    26.22    28.66    (%)
A06             160.00   292.41   360.00    (MM)
A06
A06     T4       21.41    23.94    26.25    (%)
A06             416.00   480.25   656.00    (MM)
A06
A06     T1+T2    48.82    50.21    50.84    (%)
A06             320.00   810.11   608.00    (MM)
A06
A06     T3+T4    49.15    50.17    51.17    (%)
A06             528.00   772.67   232.00    (MM)
A06
A06
A06  REFER TST6230 IN MAINTENANCE MANUAL
```

Fig. 1 Example

TST6240	Diagnosis of IBG (Interblock Gap) Length [JYOMT6Y]



Note: Refer to section JYOMT6Y in the OLTE diagnostic manual for output formats and detailed diagnosis.

Fig. 1 Output examples of JYOMT6Y

```
JYOMT6Y   V-01 L-00  RTN 02  DEV/LN 01E0  REFNO 0
IBG LENGTH CHECK TEST - 2

                                        MTU DENSITY MODE = PE
   IBG LENGTH CHECK                     MTU SPEED   MODE = NORMAL

        WRT-WRT-BSB    WRT-WRT-BSB-FSB     (MM)

   MIN      18.83           15.30

   AVG      19.07           15.48

   MAX      19.31           15.54

REFER TST6240 IN MAINTENANCE MANUAL
```

```
JYOMT6Y   V-01 L-00  RTN 01  DEV/LN 01E0  REFNO 0
IBG LENGTH CHECK TEST - 1

                                        MTU DENSITY MODE = GCR
   IBG LENGTH CHECK                     MTU SPEED   MODE = NORMAL

        BLOCK - BLOCK     TM -- TM    BLOCK - ERG - BLOCK     (MM)

   MIN      07.71           95.62          95.62

   AVG      07.77           95.73          96.09

   MAX      07.83           95.85          96.27

REFER TST6240 IN MAINTENANCE MANUAL
```

```
JYOMT6Y   V-01 L-00  RTN 02  DEV/LN 01E0  REFNO 0
IBG LENGTH CHECK TEST - 2

                                        MTU DENSITY MODE = GCR
   IBG LENGTH CHECK                     MTU SPEED   MODE = NORMAL

        WRT-WRT-BSB    WRT-WRT-BSB-FSB     (MM)

   MIN      09.26           09.26

   AVG      09.44           09.26

   MAX      09.62           09.32

REFER TST6240 IN MAINTENANCE MANUAL
```

APPENDIX

FRU CODE TABLE

How to use the FRU code table

The F617/8 MT subsystem provides a total of 24 sense bytes, sense bytes 22 and 23 of which indicate the FRU code. The meaning of the FRU code depends on the contents of the other sense bytes. The FRU code table summarizes the contents and meaning of the FRU code.

In the F617/8 MT subsystem, the FRU code (sense bytes 22 and 23) is set in the following two ways:

(1) When an error is detected and the sense bit associated with the error is set, the current status information is set in sense bytes 22 and 23 to help the user analyze the error.

(2) When an error is detected and the sense bit associated with the error is set, the error reason code is set in sense byte 22 and the contents of a related register, if required, are moved to sense byte 23.

Analysis of the FRU code

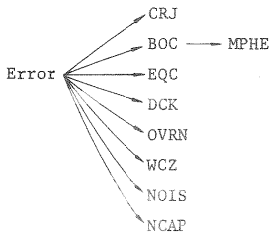
(1) First check the sense bit(s) indicated in the SENSE BIT INDICATION field of this table.

In the SENSE BYTE 22 and 23 fields, 'xx' indicates the error code (in hexadecimal) and (xxxx) indicates the status information.

When the contents of sense byte 22 match one of the error codes of this table, the cause of the error will be found in the DESCRIPTION field of this table. Most error codes are accompanied by status information in the SENSE BYTE 23 field, in which case the user can analyze the current status by referring to the DESCRIPTION field.

When sense byte 22 contains status information, the meaning of the bits of both sense bytes 22 and 23 will be found in the DESCRIPTION field.

(2) When two or more sense bits are set, first check sense byte 0 or 1.



SENSE BIT INDICATION	CONTENT OF SENSE BYTE 22	CONTEN OF SENSE BYTE 23	DESCRIPTION
C R J Command Reject [: byte 0, bit 0]	'01'	(CMD)	An invalid command was received from a channel. (CMD) indicates the command code. Check the CCW.
	'02'	(CMD)	An Unconditional Reserve command ('14'), Tape Unit Reserve command ('B4'), or Tape Unit Release command ('94') was issued to an MTC that is in the I-compatible mode. Or, a Controller Reserve command ('F4') or Controller Release command ('D4') was issued to an MTC that is not equipped with the two-channel switch option. (CMD) indicates the command code. Check the CCW, the MTC operation mode, and present of the two-channel option.
	'03'	(LCMD)	A DSE command ('97') was received from a channel, but it was not chained to an Erase command. (LCMD) indicates the last command code. When (LCMD) = '17', check the command chain flag. When (LCMD) ≠ '17', check the CCW of the command that was entered immediately before the DSE command.
	'04'	(CMD)	A Write ('01'), Write Tape Mark ('1F'), or Erase ('17') command was issued to an MTU that was file-protected. (CMD) indicates the command code.
	'05'	(SDIA1)	The MTU was file-protected but it was directed to perform a diagnostic transfer operation, such as Capstan Transfer Write (SDIA1 = 'AA'), Time Sense Transfer Write (SDIA1 = 'AC'), or Erase Transfer (SDIA1 = 'AD'). (SDIA1) indicates the diagnostic transfer code (diagnostic flag byte 1 of the SDIA command).
	'06'	(SDIA1)	The MTU was directed to perform a diagnostic transfer operation while it was detecting the TWA or BOT. (SDIA1) indicates the diagnostic transfer code (diagnostic flag byte 1 of the SDIA command). When the MTU is in the TWA state, TI (sense byte 4, bit 2) is set. When the MTU is in the BOT state, BOT (sense byte 1, bit 4) is set.
	'07'	(SDIA1)	An invalid diagnostic transfer code was specified. (SDIA1) indicates the accepted diagnostic transfer code (diagnostic flag byte 1 of the SDIA command). The following are valid diagnostic transfer codes. All other codes are considered invalid. '2A': CAP XFR FWD '6A': CAP XFR BWD 'AA': CAP XFR WRT 'EA': CAP XFR CGSP '29': ASYM XFR '2E': IBGL XFR 'AC': TS XFR WRT '2C': TS XFR FWD '6C': TS XFR BWD 'AD': ERS XFR '08': CHBF XFR
	'08'	-	Not used

SENSE BIT INDICATION	CONTENT OF SENSE BYTE 22	CONTENT OF SENSE BYTE 23	DESCRIPTION
C R J [Command Reject : byte 0, bit 0]	'09'	(CMD)	A Sense & Controller Reserve ('F4'), Sense & Controller Release ('D4'), Sense & Tape Unit Reserve ('B4'), or Sense & Tape Unit Release ('94') command was issued midway in a command chain. (CMD) indicates the accepted command code. Check the CCW.
	'OF'	(SDIA1)	The MTU was operating in the 800 rpi mode, but was directed to perform a diagnostic transfer operation. (SDIA1) indicates the accepted diagnostic transfer code (diagnostic flag byte 1 of the SDIA command).

SENSE BIT INDICATION		CONTENT OF SENSE BYTE 22	CONTENT OF SENSE BYTE 23	DESCRIPTION
B O C Bus Out Check [: byte 0, bit 2]		'B0'	(CHBO)	A parity error was detected in a command code that was received from a channel. (CHBO) indicates the received command code (contents of the channel bus out register).
	MPHE [MP Hardware Error : byte 4, bit 0 *1	'00'	'FF'	An error was detected during execution of the microprocessor (MTC) self-test routine.

		'40'
		}
		{
		'67'
			(W5)	An error was detected while conducting an EXR bit ON test in the diagnostic routine when the MTC power was turned on. Sense byte 22 indicates the address of the EXR register where the error was found. (W5) indicates the bit position that failed to turn on (flagged by a '1').

		'70'
		}
		{
		'97'
			(W5)	An error was detected while conducting an EXR bit OFF test in the diagnostic routine when the MTC power was turned on. The contents of sense byte 22 minus '30' equals the address of the EXR register where the error was detected. (W5) indicates the bit position that failed to turn off (flagged by a '1').

		'98'	(MODE)	The MCY bit (bit 0 of the MODE register) failed to turn on during execution of the diagnostic routine when the MTC power was turned on. (MODE) indicates the contents of the MODE register immediately after the error was detected.
		'99'	(MODE)	The MCY bit (bit 0 of the MODE register) failed to turn off during execution of the diagnostic routine when the MTC power was turned on. (MODE) indicates the contents of the MODE register immediately after the error was detected.

*1 : A BOC error is reported with the MPHE bit indication when an error is detected during diagnostics performed when the MTC power is turned on or the MTC is idle, or for the purpose of indicating the cause of an ICC (Interface Control Check) that occurred immediately before the error.

SENSE BIT INDICATION		CONTENT OF SENSE BYTE 22	CONTENT OF SENSE BYTE 23	DESCRIPTION
B O C [Bus Out Check : byte 0, bit 2]	[MP Hardware Error, : byte 4, bit 0]	'D0' ∿ 'D8'	(TMCTL)	An error was detected while conducting a timer circuit test in the diagnostic routine when the MTC power was turned on. (TMCTL) indicates the contents of the TMCTL register immediately after the error was detected.

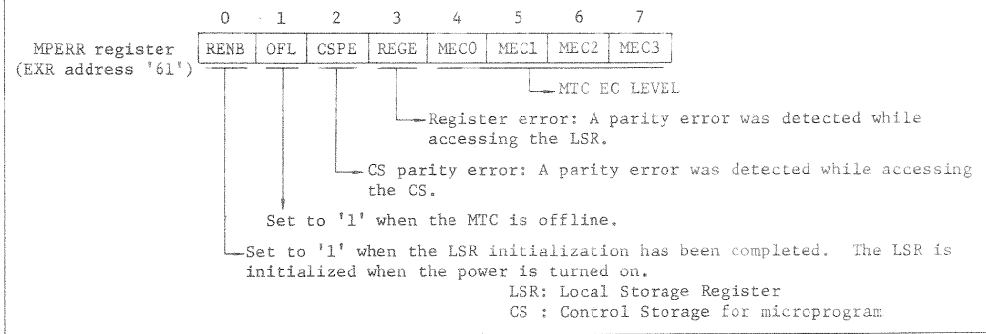
TMCTL register (EXR address '40')

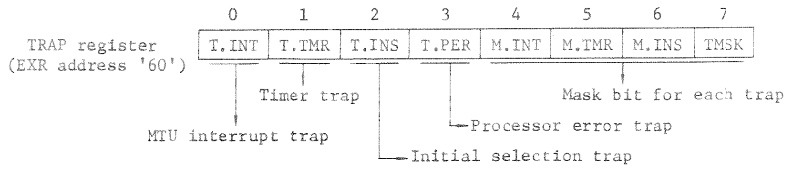
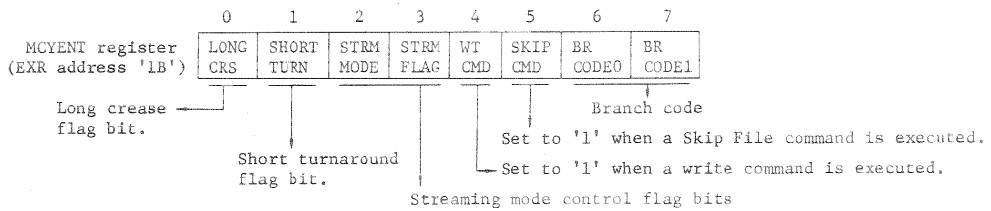
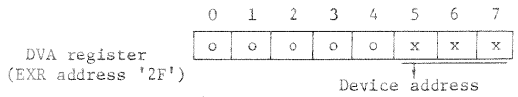
0	1	2	3	4	5	6	7
MCT0	MCT1	CQTP	ERRF	SCNT	CTRU	DFTP	DQTP

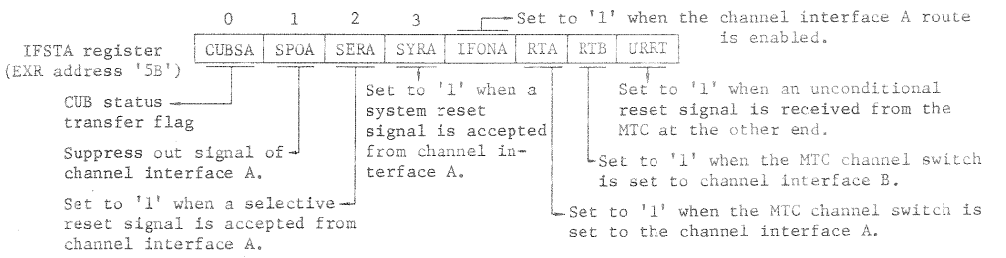
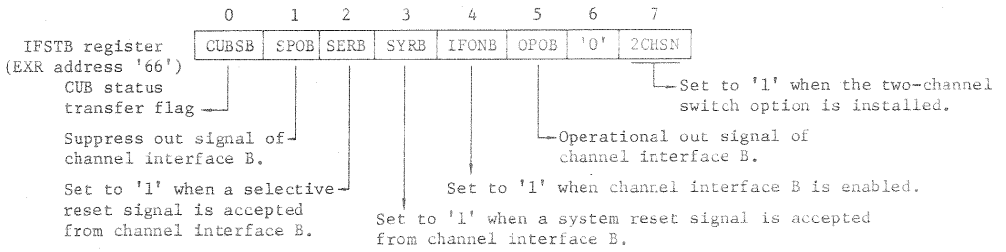
- DQTP: Set to '1' when a QTP (Quarter Tacho Pulse) is detected.
- DFTP: Set to '1' when a FTP (Full Tacho Pulse) is detected.
- CTRU: Set to '1' when the initial value input mode of the counter is the upper mode.
- SCNT: Set to '1' when the counter operation is enabled.
- MCT0, MCT1, CQTP: Count mode

MCT0	MCT1	CQTP	
0	0	x	1.66 µs clock count mode
1	0	0	FTP count mode
1	0	1	QTP count mode
x	1	0	FTP interval count mode
x	1	1	QTP interval count mode

'D0'	(TMCTL)	An attempt was made to reset the timer trap mask bit (M.TMR bit), but the bit was not reset.
'D1'		An attempt was made to reset the CTRU bit, but it failed.
'D2'		The initial value was set in the upper half of the counter, but the counter input mode was not changed to the lower mode (CTRU bit '0').
'D3'		The initial value was set in the lower half of the counter, but the counter input mode was not changed to the upper mode (CTRU bit '1').
'D4' 'D5'		The counter started operation (in the 1.66 µs clock count mode), but did not indicate the expected value after a certain time interval elapsed.
'D6'		No carry signal is detected from the timer circuit after a certain time interval.
'D7'		A carry signal was detected from the timer circuit, but the lower half of the timer value was not 'FF' at that moment.
'D8'		A carry signal was detected from the timer circuit, but the upper half of the timer value was not 'FF' at that moment.

SENSE BIT INDICATION		CONTENT OF SENSE BYTE 22	CONTENT OF SENSE BYTE 23	DESCRIPTION
B O C [Bus Out Check : byte 0, bit 2]		'DA'	(Shift Count)	An error was detected while conducting a serial scan test of all flip-flops of the write circuit LSIs (the LSIs installed in the PCA 512186, namely one 61504 and one 61506) in the diagnostic routine when the MTC power was turned on. (Shift count) indicates the scan shift count.
		'DB'	(Shift Count)	An error was detected while conducting a serial scan test of all flip-flops of the Read circuit LSIs (the LSIs installed in the PCA 512188, namely three 61507s, three 61508s, and one 61509) in the diagnostic routine when the MTC power was turned on. (Shift count) indicates the scan shift count.
	MPHE [MP Hardware Error : byte 4, bit 0]			
		'F0'	(MPERR)	A processor failure was detected when the MTC was idle. (MPERR) indicates the contents of the MPERR register immediately after the error was detected. 
		'F1'	(Check result)	An error was detected during execution of the check-out routine when the MTC was idle. (Check result) indicates the value obtained by the check-out routine. The normal result is '8B'.

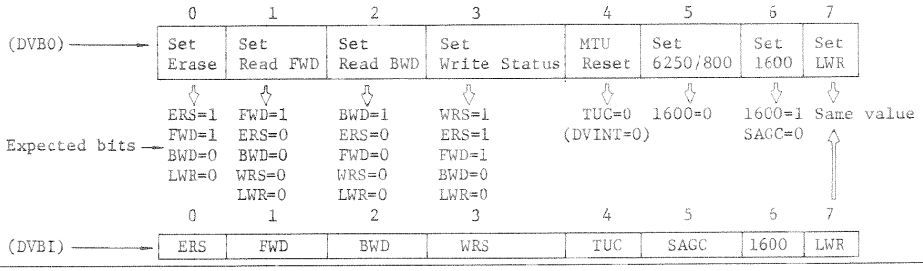
<table>
<tr><th colspan="2">SENSE BIT INDICATION</th><th>CONTENT OF SENSE BYTE 22</th><th>CONTENT OF SENSE BYTE 23</th><th>DESCRIPTION</th></tr>
<tr><td rowspan="5">B O C
[Bus Out Check
: byte 0, bit 2]</td><td rowspan="5">MPHE
[MP Hardware Error
:byte 4, bit 0]</td><td>'F2'</td><td>(TRAP)</td><td>An unaccountable trap was detected in the MTC microprocessor. (TRAP) indicates the contents of the TRAP register immediately after the trap occurred.
 
</td></tr>
<tr><td>'F5'
'F6'</td><td>(MCYENT)</td><td>A processor failure was detected while the MTC was executing a command or during a system reset or selective reset operation.
Sense byte 22 = 'F5' ... When the OPI signal is on (under connection to a channel).
Sense byte 22 = 'F6' ... When the OPI signal is off (control command, etc.).
When a failure is detected, an interface disconnect signal is sent to the channel.
(MCYENT) indicates the contents of the MCYENT register when the failure was detected.
 
</td></tr>
<tr><td>'F7'</td><td>(DVA)</td><td>An error was detected in the contents of the DVA register when the selective reset routine was to be executed. (DVA) indicates the contents of the DVA register immediately after the error was detected.
 
</td></tr>
<tr><td>'F8'</td><td>LSR address</td><td>An error was detected while conducting an LSR read/write test in the diagnostic routine when the MTC power was turned on. (LSR address) indicates the LSR address where the error was found.</td></tr>
<tr><td>'F9'</td><td>(LSR#00)</td><td>When the MTC power was turned on, an LSR read/write test of the diagnostic routine was conducted. In the test, an attempt was made to set 'FF' in the register at LSR address '00', but some of the register bits remained reset. (LSR#00) indicates the date read from the register at LSR address '00' when the error was detected.</td></tr>
</table>

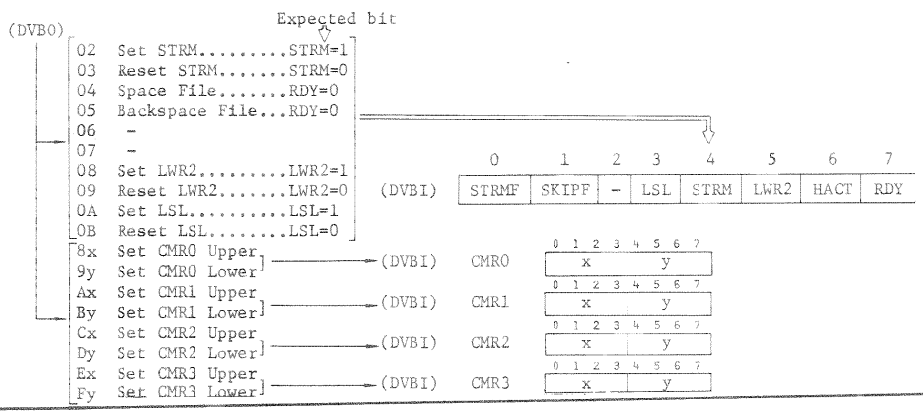
<table>
<tr><th colspan="2">SENSE BIT INDICATION</th><th>CONTENT OF SENSE BYTE 22</th><th>CONTENT OF SENSE BYTE 23</th><th>DESCRIPTION</th></tr>
<tr><td rowspan="5">B O C
[Bus Out Check
: byte 0, bit 2]</td><td rowspan="5">MPHE
[MP Hardware Error
: byte 4, bit 0]</td><td>'FA'</td><td>(IFSTA)</td><td>A system reset or selective reset operation was requested from channel interface A, but the reset operation was not completed normally since the SERA or SYRA signal was not reset. (IFSTA) indicates the contents of the IFSTA register immediately after the error was detected.
 
</td></tr>
<tr><td>'FB'</td><td>(IFSTB)</td><td>A system reset or selective reset operation was requested from channel interface B, but the reset operation was not completed normally since the SERA or SYRA signal was not reset. (IFSTB) indicates the contents of the IFSTB register immediately after the error was detected.
 
</td></tr>
<tr><td>'FC'</td><td>(IFSTA)</td><td>When the MTC power was turned on, the microprocessor was reset although no reset signal was issued from a channel. Or, an attempt was made to execute the reset routine, but the cause of the reset is unaccountable. (IFSTA) indicates the contents of the IFSTA register when the error was detected.</td></tr>
<tr><td>'FE'</td><td>(LSR address)</td><td>An attempt was made to clear a particular LSR register, but it was not cleared even after the clear operation was retried. (LSR address) indicates the address of the LSR register.</td></tr>
<tr><td>'FF'</td><td>XX</td><td>An error was detected in the MTC microprocessor self-test routine that was executed when the MTC power was turned on or when a system reset or selective reset operation was performed.</td></tr>
</table>

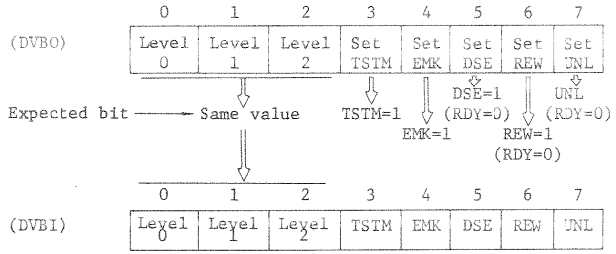
SENSE BIT INDICATION	CONTENT OF SENSE BYTE 22	CONTENT OF SENSE BYTE 23	DESCRIPTION
EQC [Equipment Check : byte 0, bit 3]			
MPHE [MP Hardware Error : byte 4, bit 0]			
	'40' { '67'	(W5)	An error was detected in an EXR bit ON test when the Test MTC operation of the SDIA command was being performed. The contents of sense byte 22 indicate the EXR register address where the error occurred. (W5) indicates the bit position that failed to turn on (flagged by a '1').
	'70' { '97'	(W5)	An error was detected in an EXR bit OFF test when the Test MTC operation of the SDIA command was being performed. The contents of sense byte 22 minus '30' equal the EXR register address where the error occurred. (W5) indicates the bit position that failed to turn off (flagged by a '1').
	'98'	(MODE)	When the Test MTC operation of the SDIA command was being performed, the MCY bit (bit 0 of the MODE register) failed to turn on. (MODE) indicates the contents of the MODE register immediately after the error was detected.
	'99'	(MODE)	When the Test MTC operation of the SDIA command was being performed, the MCY bit failed to turn off. (MODE) indicates the contents of the MODE register immediately after the error was detected.
MPTRP [MP Trap : byte 11, bit 6]	'78'	-	A microprocessor trap took place while a command was being executed (or when the MCY bit is on), but the cause of the trap was not found.

SENSE BIT INDICATION		CONTENT OF SENSE BYTE 22	CONTENT OF SENSE BYTE 23	DESCRIPTION
E Q C [Equipment Check : byte 0, bit 3]	MPHE [MP Hardware Error : byte 4, bit 0]	'CD'	(CMD)	A command was decoded abnormally in the command code decoding routine. (CMD) indicates the contents of the CMD register at that moment, namely the command code that was accepted by the MTC.
		'DE'	(MASK)	An error was found in the phase error pointer circuit during a 6250-rpi-mode phase error test when the Test MTC operation of the SDIA command was being performed. (MASK) has the contents of the MASK register at that moment, in which the bit position that caused the phase error is flagged by a '1'. When (MASK) = '00', bit 8 caused the phase error. When (MASK) = 'FF', the error occurred in the block check circuit (both the DBOB and DIBG signals are set). Sense byte 2 contains the contents of the pointer that was actually detected. Sense byte 2 normally matches the value of (MASK).
		'DF'	(MASK)	An error was detected in the phase error pointer circuit during a 1600-rpi-mode phase error test when the Test MTC operation of the SDIA command was being performed. The contents of (MASK) and sense byte 2 are set in the same way as in the sense byte 22 = 'DE' case.
		'D0' 〃 'D8'	(TMCTL)	An error was detected in a timer circuit test when the Test MTC operation of the SDIA command was being performed. (TMCTL) indicates the contents of the TMCTL register immediately after the error was detected. The bit pattern of the TMCTL register and the meaning of the error codes 'D0' to 'D8' are the same as for the BOC-MPHE errors.

SENSE BIT INDICATION		CONTENT OF SENSE BYTE 22	CONTENT OF SENSE BYTE 23	DESCRIPTION
E Q C [Equipment Check : byte 0, bit 3]	STRJ [Status Tag Reject : byte 10, bit 0]	(DVBO)	(DVBI)	While the MTU was being controlled by a status tag, the MTU status response was interrupted by a timeout. (DVBO) indicates the tag control information received from the MTC, and (DVBI) indicates the MTU response at the timeout.
	CMRJ [Command Tag Reject : byte 10, bit 1]	(DVBO)	(DVBI)	While the MTU was being controlled by a command tag, the MTU command tag response was interrupted by a timeout. (DVBO) indicates the command tag information received from the MTC, and (DVBI) indicates the MTU response at the timeout.



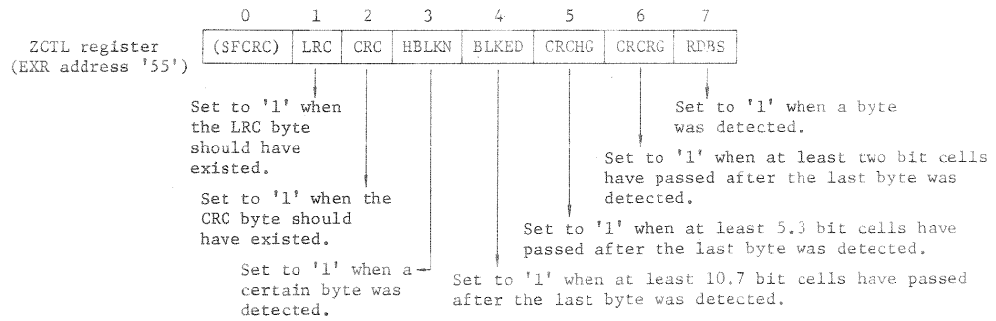


SENSE BIT INDICATION		CONTENT OF SENSE BYTE 22	CONTENT OF SENSE BYTE 23	DESCRIPTION
E Q C [Equipment Check : byte 0, bit 3]	CTRJ [Control Tag Reject : byte 10, bit 2]	(DVBO)	(DVBI)	While the MTU was being controlled by a control tag, the MTU control tag response was interrupted by a timeout. (DVBO) indicates the control tag control information and (DVBI) indicates the MTU response at the timeout. 
	TIRC [Tag in Response Check : byte 11, bit 2]	'E8'	(DVBO)	The MTC accessed an MTU sense byte, but the MTU made no tag-in response. (DVBO) indicates the contents of the DVBO register when the error occurred. (DVBO) = '00' ... when TUSE0 was accessed '01' ... when TUSB0 was accessed '02' ... when TUSB1 was accessed '08' ... when TUSB8 was accessed
	TCSF [Tacho Start Failure : byte 10, bit 5]	(W0)	(W1)	The MTU was started, but the tape was not moved at least as far as specified in the specified direction within the specified time period. (W0) = 108 [QTP] - Total distance the tape moved [QTP] (W1) = 20 [QTP] - Total distance the tape moved in the specified direction [QTP]
		'DD'	-	Note that when the MTU operates in the high-speed mode and (W0) = 'DD' is set, this indicates that no GAPC signal was detected within one second after the GO signal was set. In this case, the contents of sense byte 23 are unpredictable.
	MPTRP [MP Trap : byte 11, bit 6]	'74'	-	A processor trap took place because of an abnormally long tacho pulse cycle time.

SENSE BIT INDICATION		CONTENT OF SENSE BYTE 22	CONTENT OF SENSE BYTE 23	DESCRIPTION
E Q C [Equipment Check : byte 0, bit 3]	DYRV [Dynamic Reversal : byte 10, bit 4]	'CC'	(W1)	The MTU was started by th GO signal, but the tape was moved farther than specified in the opposite direction. (W1) = Distance the tape moved in the specified direction before this error was detected [QTP] 108 - (W1) = Distance the tape moved in the opposite direction before this error was detected [QTP]
		'EE'	(TSNS)	While the tape was moving in the backward direction, the ARA ID Burst was detected but, no BOT marker was detected after that within a certain distance. (TSNS) indicates the time sense output produced when this error was found.
	VLCK [Velocity Check : byte 10, bit 7]	FTP cycle time Upper	FTP cycle time Lower	The MTU was started, but the nominal tape speed was not reached within a certain distance. Sense bytes 22 and 23 indicate the FTP cycle time when this error was detected. SENSE BYTE 22 (0 1 2 3 4 5 6 7) 23 (0 1 2 3 4 5 6 7) MSB ... LSB A FTP cycle time $T = A \times 208$ [ns] Speed $v = \frac{0.00942}{T} \times 10^6$ [inch/s]
	IBGD [IBF detect : byte 8, bit 0]	(TSNS)	(BLFMT)	The IBG was not detected within the specified time. (TSNS) indicates the time sense information obtained when this error was detected, and (BLFMT) gives block check information. (TSNS): 0 1 2 3 4 5 6 7 — TSNS — 0 1 2 3 4 5 6 7 Each bit is set to '1' when data is detected. (BLFMT): 0 (IO2 CR) 1 (DET8) 2 TSNS8 3 DIBG 4 DNIS 5 DBOB 6 DARA 7 DTM Set to '1' when the IBG pattern is detected. Set to '1' when a noise pattern is detected. Set to '1' when the tape mark pattern is detected. Set to '1' when the ARA pattern is detected. Set to '1' when a data block pattern is detected.

SENSE BIT INDICATION	CONTENT OF SENSE BYTE 22	CONTENT OF SENSE BYTE 23	DESCRIPTION
E Q C [Equipment Check] : byte 0, bit 3			
WTMC [Write Tape Mark Check] :byte 5, bit 2			
In the 1600/6250-rpi mode *2	(TSNS)	(BLFMT)	The tape mark was not be written correctly. (TSNS) and (BLFMT) give the time sense information and block check information (respectively) obtained when this error was detected. For the meaning of these information, see the EQC-IBGD error description. If the tape mark is written normally, all TSNS bits of the tape mark except bits 1, 3, and 4 should be set to '1' and the DTM bit should also be set to '1'.
In the 800-rpi mode *2	'31'	(ZCTL)	A tape mark byte that should have been wirtten could not be detected.
	'32'	(ZCTL)	The first byte written was not found to be a tape mark byte.
	'33'	(ZCTL)	A noise byte was detected between two tape mark bytes that had been written.
	'34'	(ZCTL)	Two tape mark bytes should have been written, but the second one could not be detected.
	'35'	(ZCTL)	Two tape mark bytes should have been written, but the second tape mark byte was not found.
	'36'	(ZCTL)	An abnormal noise byte was detected after two tape mark bytes that had been written.

(ZCTL) indicates the hardware timing signal at the time when this error was detected.

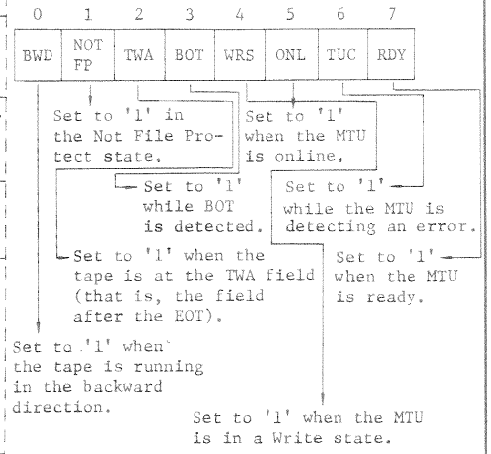


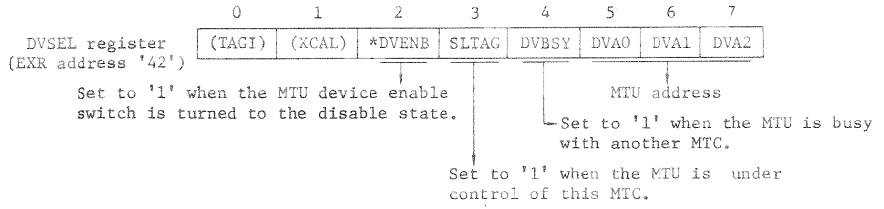
*2: The 1600/6250 rpi mode and 800 rpi mode can be checked by referring to bit 5 of sense byte 3 (1600 rpi), bit 3 of sense byte 6 (Not Set 1600), and bit 4 of sense byte 6 (6250 TU).

6250TU	1600rpi	Not Set 1600	mode
0	1	0	→1600rpi
0	0	1	→ 800rpi
1	1	0	→1600rpi
1	0	1	→6250rpi

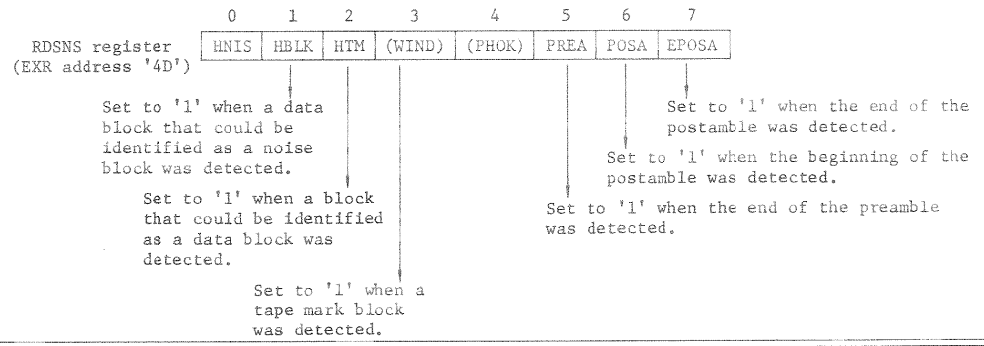
SENSE BIT INDICATION		CONTENT OF SENSE BYTE 22	CONTENT OF SENSE BYTE 23	DESCRIPTION
EQC [Equipment Check " byte 0, bit 3]	MPTRP [MP Trap : byte 11, bit 6]			
	TI [Tape Indicater byte 4, bit 2]	'70'	(DVBI)	While the MTU was operating in the test mode (that is , when the SDIA command was being executed or the MTU was offline from the MTC), the EOT marker was detected and a processor trap took place.
	BOT [BOT :byte 1, bit 4]	'70'	(DVBI)	When the tape of the MTU was running in the backward direction, the BOT marker was detected and a processor trap took place.
	SAGC [SAGC :byte 8, bit 4]	'70'	(DVBI)	A processor trap occurred because the MTU was interrupted by an SAG error.
	FP [File protect :byte 1, bit 6]	'70'	(DVBI)	While data or a tape mark was being written or erased in the MTU, a file protect state was forced and a processor trap occurred.
	TUSTA [TU Status A :byte 1, bit 1] & TUSTB [TU Status B : byte 1, bit 2] (TUST=11)	'70'	(DVBI)	While the MTU was skipping a file, it was interrupted because the tape had run farther than a certain distance (about 20 m) without detecting a tape mark, and a processor trap took place. (Tape overrun)
	RJTU [Reject TU :byte 4, bit 1]			
	IRQ [Intervention Required :byte 0, bit 1]	'70'	(DVBI)	The MTU entered an IRQ state and a processor trap occurred while a command was being executed.
	TCSF [Tacho Start Failure :byte 10, bit 5]	'74'	-	A processor trap occurred because of an abnormally long tacho pulse cycle time.

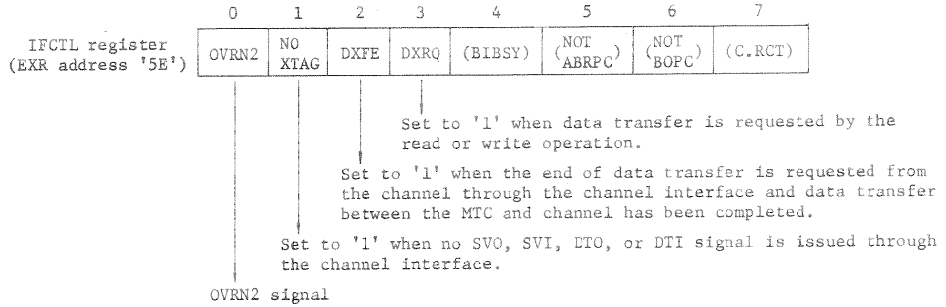
(DVBI) indicates the contents of MTU sense byte 0 when the processor trap occurred.

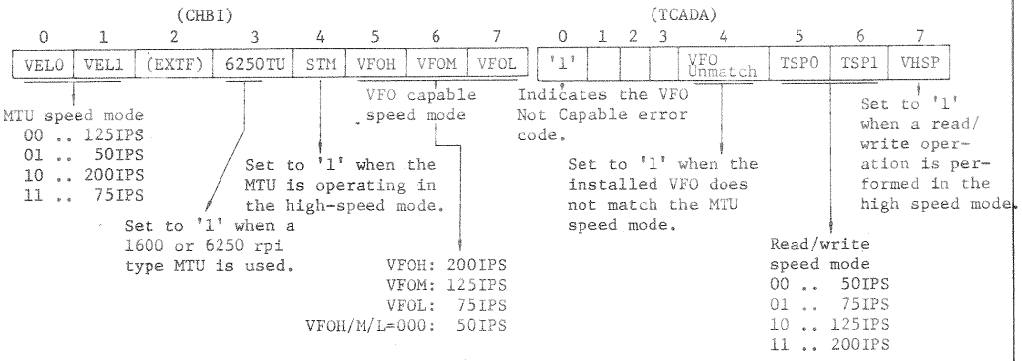
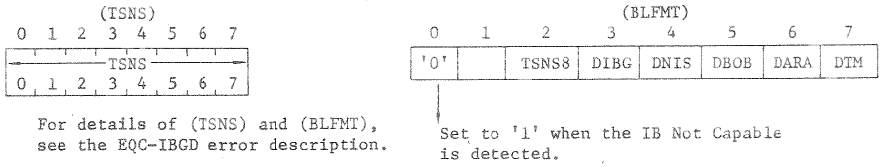


SENSE BIT INDICATION		CONTENT OF SENSE BYTE 22	CONTENT OF SENSE BYTE 23	DESCRIPTION
EQC [Equipment Check : byte 0, bit 3]	MPTRP [MP Trap : byte 11, bit 6]			
	RWOV [R/W overrun :byte 11, bit 0]	'77'	-	An abnormally long block was written or read.
	MPHE [MP Hardware Error :byte 4, bit 0]	'78'	(DVBI)	A processor trap occurred while a command was being executed, but the cause of the trap was not found. (DVBI) indicates the contents of MTU sense byte 0 when the error occurred.
		'7F'	(DVBI)	A processor trap occurred because the MTU was interrupted, but the cause of the interrupt was not found. (DVBI) indicates the contents of MTU sense byte 0 when the error occurred.
	RJTU [Reject Tapu unit :byte 4, bit 1	'E0'	(DVSEL)	The tacho pulse cycle time became abnormally long while performing the Capstan XFR operation of the SDIA command. (DVSEL) indicates the contents of the DVSEL register at that moment. 
		'E2'	(DVBI)	A TU check occurred while the MTU was being controlled by a command chain. (DVBI) indicates the contents of MTU sense byte 0 at that moment.
	WCALM [Write Circuit Alarm :byte 6, bit 1	'OA'	(DVBI)	An error was detected in the MTU write circuit. (DVBI) indicates the contents of MTU sense byte 0 when the error was detected.
	NOIS [Noise :byte 1, bit 0] In the 6250 or 1600-rpi mode	(TSNS)	(BLFMT)	Noise was detected while the erase command was being executed or an additional erase operation was being performed. (TSNS) and (BLFMT) give the time sense information and block check information (respectively) obtained when the error was detected. (See the EQC-IBGD error description).

SENSE BIT INDICATION		CONTENT OF SENSE BYTE 22	CONTENT OF SENSE BYTE 23	DESCRIPTION
D C K [Data Check : byte 0, bit 4]	One of the following bits is set: PCMP [Parity Compare : byte 3, bit 7] XBFC [XFR buffer Check : byte 9, bit 2] ORCE [CRC error : byte 3, bit 3] CRC3 [CRC3 Check : byte 9, bit 3] WVRC [Write VRC : byte 4, bit 3]	'1x'	(CRCST)	SENSE BYTE 22 0 1 2 3 4 5 6 7 0 0 0 1 0 ABRP DBCK WVRC A/B register parity check Deskewing buffer check Set to '1' when a parity error is detected in write data after modulation SENSE BYTE 23 0 1 2 3 4 5 6 7 *MCRC *CRCZ EP≠CR B≠D B≠C *MCRCC A≠B XBIC Set to '1' when a CRC error is detected in read data while reading or writing in the 6250 or 800-rpi mode. Set to '1' unless all CRC bits are '0's. Set to '1' when the CRC bit pattern does not match the contents of the error pattern register. Set to '1' when the CRC pattern (CRCA) generated by XFR buffer input does not match the CRC pattern (CRCB) generated by XFT buffer output. Set to '1' when a parity error is detected in the XFR buffer input data. Set to '1' when the CRCB pattern does not match the CRCD pattern. Set to '1' when the CRCB pattern does not match the CRCC pattern. Set to '1' when the CRCC pattern is incorrect.
	IBGD [IBG detect : byte 8, bit 0] SRDC [Start Read Check : byte 5, bit 4] PREC [Partial record : byte 5, bit 5] POSAE [Postamble error : byte 5, bit 6]	'A8'	(RDSNS)	Excessive drop-outs were detected while data writing, so the data write operation was stopped immediately. When this error occurs, the ENVC bit (Envelop Check: byte 3, bit 4) is also set. (RDSNS) indicates the contents of the RDSNS register set when this error was detected. A drop-out was detected in the preamble. A drop-out was detected in the data area. A drop-out was detected in the postamble.

SENSE BIT INDICATION		CONTENT OF SENSE BYTE 22	CONTENT OF SENSE BYTE 23	DESCRIPTION
D C K [Data Check : byte 0, bit 4]	IBDC (continued)			
	POSAE [Postamble error : byte 5, bit 6]	'DD'	-	A byte having a pattern other than the specified one was read between the beginning and end of the postamble.
	Others	'AA'	-	A tape mark block was detected, but while being read, it changed to a data block pattern. Therefore, the block was processed as a data block rather than a tape mark block.

SENSE BIT INDICATION	CONTENT OF SENSE BYTE 22	CONTENT OF SENSE BYTE 23	DESCRIPTION
O V R N [Overrun : byte 0, bit 5]	'20'	(IFCTL)	The XFR buffer did not become idle after a certain time had elapsed after read operation.
	'21'	(IFCTL)	The XFR buffer became full during a read operation. Or, during a write operation, the XFR buffer became idle (in the 1600 or 800 rpi mode) or it was holding fewer bytes than specified (in the 6250 rpi mode) before the end of data transfer was reported from the channel. (OVRN signal)
	'22'	(IFCTL)	When data was being transferred to or from the channel in the offset interlock mode, an abnormal SVO or DTO signal was detected. (OVRN2 signal) (IFCTL) indicates the contents of the IFCTL register set when the above errors were detected. 
W C Z [Word count zero : byte 0, bit 6]	'FF'	-	The XFR buffer was not idle when data transfer was started to or from the channel for execution of a Write command.
	'00'	-	The interface was disconnected before data transfer was started to or from the channel for execution of a Write command.

SENSE BIT INDICATION	CONTENT OF SENSE BYTE 22	CONTENT OF SENSE BYTE 23	DESCRIPTION
N C A P [Not Capable : byte 1, bit 7] *3	(CHBI)	(TCADA)	The MTU speed mode does not match the VFO readable speed mode. (VFO Not capable) 
	(TSNS)	(BLFMT)	An ID Burst having a recording density unavailable in the MTU was detected. 

*3: VFO Not Capable and IB Not Capable are indicated in bit 0 of sense byte 23.